DATA HANDBOOK

10/100K ECL
Logic/Memory/PLD

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Philips Components

PHILIPS

10/100K ECL Logic/Memory/PLD

Page

Introduction iv
Contents viii
Ordering information xi
Product status xii

Section 1 - Selection Guides

Index 1

Section 2 - Quality and Reliability

Quality and Reliablity 13

Section 3 - Testing

Introduction 23
Chapter 1 - DC Testing 23
Chapter 2 - AC Testing 25

Section 4 - ECL User's Guide

Index 35

Section 5 - Data Sheet Specification Guide

Index 65

Section 6 - 10K Series Data Sheets

Index 79

Section 7 - 100K Series Data Sheets

Index 355

Section 8 - ECL Memory Data Sheets

Index 613

Section 9 - Package Outlines

Index 653

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Preface

Philips Components would like to thank you for your interest in our products. This handbook contains information and specifications on SSI, MSI, and LSI standard products of the 10K and 100K ECL families. Philips Components offers a broad range of Logic Products besides those described in this data handbook. New Random Logic families such as 74HC/HCT and 74F are contained in other data handbooks. TTL, 4000 Series CMOS, PROM/RAM, and Application Specific Product specifications are contained in separate data handbooks.

This new edition also includes:

- specifications for four parts of a new translator/transceiver family
- specifications for ECL PALs and PROMs
- ECL User's Guide
- an expanded chapter on AC test techniques
- updated package information

Philips Components is continually developing new products. As you see new product announcements, you should contact your local Philips Components sales office representative or authorized distributor for the latest technical information.

Introduction

ECL Products

EMITTER–COUPLED LOGIC (ECL)

Emitter–coupled logic is the fastest logic technology available for practical use. Traditionally developed for the high speed elements of mainframe computers, it is being applied wherever ultra–high switching speeds are required. Typical applications include signal generations and processing, digital switching and filtering networks, arithmetic and logic units of computers, optical transmission line interfaces and digital video systems.

This data manual describes the 10K and 100K ECL series. Other ECL products such as ECL Memories, are available from the Bipolar Memory family and ECL semicustom products, such as Advanced Customized ECL (ACE) are available from the Application Specific Group.

GENERAL

The Logic families table compares the propagation delay and power consumption per gate of 10K and 100K to other logic families.

ECL is a current switching logic. In the basic gate of Figure 1, the current from the current source flows continuously through either branch A or B. The exponential change of emitter current with base–emitter voltage results in rapid switching of the current path and allows considerable amount of noise immunity to be built into the circuits. Furthermore, the constant current nature of the circuits minimizes voltage fluctuations (noise) due to switching in the supply lines, eliminating the need of ultra–fast, expensive voltage regulators. The effects of switching output loads are isolated from the inputs by the use of separate V_{CC} supplies for the outputs.

Since there are no internal output load resistors, outputs can be OR–wired, thus saving additional circuitry. Most devices in the family provide complementary outputs, allowing simpler system design and eliminating inverters that would otherwise increase power consumption a circuit cost.

The 100K series is fully compensated for changes in both temperature and voltage, in both the internal bias generator and the output circuitry. Therefore, 100K ECL provides easier thermal management than the 10K or 10KH series, which do not provide full temperature compensation in their output voltage circuitry.

The high current drive capability of the 100K ECL is a valuable feature when switching signals at speeds requiring transmission line techniques. High current drive contributes to the signal–to–noise ratio achieved at the receiving end. It also permits a large fan–out, since all inputs have an internal pull–down resistor of typically 50,000 ohm to V_{EE}.

LOGIC FAMILIES		GATE DELAYS (ns)	POWER CONSUMPTION (mW)
Conventional Logic	TTL	10	10
	LSTTL	9	2
	S TTL	3	20
	10K ECL	2	25
Advanced Logic	FAST	2	4
	ECL	0.75	40

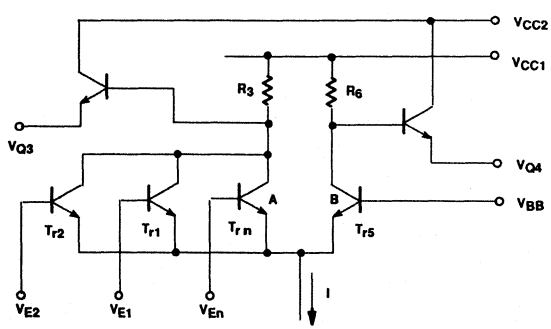


Figure 1. ECL is a Current–Switching Logic. Ther current drawn from the supply voltage (V_{CC1}) is thus independent of the state of the inputs. The use of a separate supply (V_{CC2}) for the output load minimizes the effect of output noise on the inputs.

Introduction

TECHNICAL FEATURES OF ECL

The Technology

A conventional planar process is used for the 10K ECL series with a density of about ten gates per mm^2 and a delay of 2ns per gate. This junction–isolated process achieves a 1.5GHz transition frequency. To achieve the 0.75ns per gate delay and 20 gates per mm^2 density of 100K ECL, an oxide–isolated SUBILO (**SUB**nanosecond Isolation by **L**ateral **O**xidation) process is used. This process achieves a tradition frequency of about 4.5GHz.

What ECL Provides

a) First of all, ECL provides very high speed, enabling high frequency operation.

b) Furthermore, the power consumption required (although high for a simple gate) increases less rapidly than the complexity of the functions in an integrated circuit.

c) Moreover, thanks to ECL, it is possible to process fast phenomena in real time (e.g., monitoring of nuclear phenomena, time bases for oscilloscopes; and, in general, all measurements whose resolution should be less than one nanosecond).

d) ECL also makes it possible to treat very complex phenomena in real–time (e.g., meteorology, the management of power networks, or of very large data bases (in the case of large computers in which processing time is determining factor)).

e) Lastly, ECL makes it possible to optimize the cost of a system by accelerating the subsystems that must respond rapidly (such as an ECL number multiplier in a TTL computer).

When to use ECL

ECL should be used when a gain in speed beyond that achievable with saturating logic families is necessary.

ECL makes it possible to improve the cost of a system. For example, in telecommunications and in data communications, the increase in the line rate makes it possible to use fewer lines, thereby reducing the overall stem cost a system maintenance.

ECL should be used for data rates greater than 100 mega bits per second.

Where to use ECL

a) Large–scale Computation

- Any CPU having a cycle time between 10 and 50ns is partly entirely ECL.
- Likewise, high–speed I/O controllers (access channels to disks, memory blocks, high speed peripherals, or to other processors.)
- Memories having very fast access time are ECL (buffer or "cashe" memories, most of the time; but sometimes central memories too, for the fastest large computers).

b) Small– and Medium–scale Computation

- It is possible to increase the power of a small, microprocessor–based system by adding onto its bus some high–speed hardware functions., such as adders, multipliers, fast Fourier transforms, correlators, etc.
- Likewise, high–speed I/O controllers (acess channels to disks, memory blocks, high speed peripherals, or to tother processors.)

c) Instrumentation

ECL makes it possible to build:

- rapid logic or analog testers for components or boards;
- logic analyzers, for the simultaneous acquisition of the logic state of several channels or signals in a system that is being developed or maintained;
- high–speed oscilloscopes, with acquisition, storage,a and digital processing of signals;
- very high–resolution chronometers and high–speed frequency counters.

d) Telecommunications

- ECL is presently being used in the development of computers that direst telephone switching centers.
- ECL also makes it possible to design new telephone centers that switch wide based signals (from video or from data channels), or even multiplex many audio channels.
- Lastly ECL makes it possible to realize high–rate inter–center connections (for concentration, coding, repeaters and regenerators, decoding, demultiplexing) via coaxial cables, optic cables, or microwaves.

d) Real–time Digital Signal Processing

- ECL is the ideal technology for digital processing of television video signals (filtering, decoding, mixing, special effects, broadcasting).
- ECL also makes it possible to digitize the principal functions of television sets.
- Real-time simulators of complex phenomena (such as flight simulators or artillery simulators) contain large portion in ECL.
- ECL also lends itself to radar–signal processing.

COMPARISON WITH OTHER LOGIC FAMILIES; SELECTION CRITERIA

ECL contains essentially the principal functions of other logic families (gates, flip–flops, complex or MSI circuits).

With a few exceptions, the functions are classified according to the following order of their last three digits (with the prefix of 10XXX or 100 XXX):

100 to 109: Simple gates
110 to 119: Complex gates and line receivers
120 to 129: Interfaces
130 to 139: Flip–flops, counters
140 to 155: Registers, memories, combination of latches and myltiplexers

- 100 to 109: Simple gates
- 110 to 119: Complex gates and line receivers
- 120 to 129: Interfaces
- 130 to 139: Flip–flops, counters
- 140 to 155: Registers, memories, combination of latches and multiplexers
- 156 to 179: Combinatorial MSI (parity, priority, multyiplexers, decoders, delay)
- 180 to 189: Arithmetic circuits (adders, ALUs)
- 190 to 399: Ohter special interfaces
- 400 to 499: High capacity memories
- 500 to 599: Military series
- 700 to 799:
- 800 to 899: Microprocessors and associated circuits
- 900 to 999: circuits

It was not possible to reproduce exactly under the same numbers, the logic functions existing in TTL, for the following reasons:

1. In general, ECL circuits require three power supply pins, as opposed to two for the TTL circuits. Therefore, the number of pins available for the input/output of logic signals is different.

2. The basic ECL gate performs an OR function, whereas the basic TTL gate performs an AND function.

3. ECL gates have built–in complementary outputs(Q and $\overline{Q}$). thus enabling great flexibility in use. The functions that utilize these outputs are special within the family, and often replace two TTL functions at the same time.

4. In the particular case of the ECL 100K series,

Introduction

the standard package contains 24 pins, thus enabling more complex functions, replacing several TTL types. Thus, a 100170 decoder can be configured as a 1 X 8 or a 2 X 4 device with High or Low outputs, thus performing the functions of four TTL decoders.

5. Interface requirements are different for high–speed circuits, which normally only handle data, and for slow logic circuits that can be interfaced to display devices ("display devices") or power devices.

ECL devices can be interfaced in the following ways:

- using short distance transmission lines [for example, twisted –(pair) wires] with line transmitters having differential inputs;
- through ECL–level data buses, by bus drivers that can provide a high current on the bus, or else can be disconnected, loading it as little as possible, thus realizing the the equivalent of three–state TTL circuits;
- to other logic families; ECL 10K to 100K, ECL to CMOS or to TTL. Specifically, to be able to interface ECL processors to MOS central memories at the TTL level, via bidirectional interfaces.

Table 1 summarizes the principal characteristics of the logic families.

Other high–speed circuits exist which, without strictly being part of the ECL logic families, do have inputs or outputs that are compatible with ECL levels, and rely largely on emitter coupled techniques in their internal electrical circuitry. VHF and UHF frequency dividers ("prescalers") utilized in counters and synthesizers are the best known examples; but multivibrators, phase comparators, analog converters, etc., also exist.

PRINCIPAL CHARACTERISTICS	CMOS		TTL–COMPATIBLE				ECL	
	HC	HCT	TTL	LS	S	FAST	10K	100K
Supply Voltage (V)		5	5	5	5	5	–5.2	–4.5
Supply Current per gate (mA)		1.4	2	0.4	4	1	5	8
Logic Swing (V)	3	3	3	3	3	3	0.9	0.7
Maximum Fanout	10	10	10	20	10	30	>30	>30
Typical Propagation Delay (ns)	9	9	10	10	3	2.8	2	0.75
Edge Rate (V/ns)	0.5	0.5	0.35	0.2	2.0	2.0	2	0.75
Maximum Frequency of a D–type Flip–Flop (MHZ)	15	15	15	25	75	100	125	400
Loss of speed due to Output Loading (ns/Load utilized)	1.2	1.2	0.6	0.3	0.3	0.1	0.1	0.07
Figure of Merit per simple gate	20	20	100	20	55	14	50	30
Figure of Merit per complex function							10	5
Principal package (pins)	14, 16	14, 16	14, 16	14, 16	14, 16	14, 16	16	24
Number of Product types	120	120	>100	>150	>100	235	60	40
Operating Range: Commercial	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Operating Range: Military	Yes	Yes	Yes	Yes	Yes	Yes	No	No

NOTE: The sets of data given above are a very simplified representation of existing logic families. The value indicated are only approximate; they depend entirely on utilization conditions(supply voltage, loading conditions, etc.,) and on the supplier.

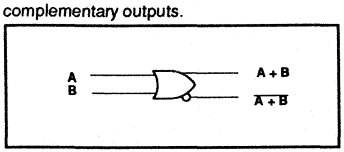
Introduction

DESCRIPTION OF ECL FAMILIES

Two ECL families (the ECL 10K and the ECL 100K series) are presently considered standard (multiple vendors). The former contains more than 60 types, and the latter approximately 40.

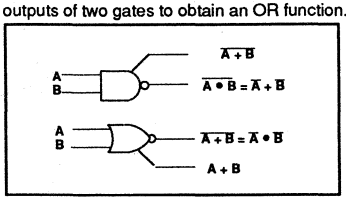
Logic Diagrams

At the elementary–circuit level, the basic gate is an OR/NOR gate with the two inputs and complementary outputs.



The fact that all of these gates have true and complementary (inverting) outputs makes it easier to implement logic diagr ams.

Another worthwhile possibility is the wired–OR-gate which enables the direct connection of the outputs of two gates to obtain an OR function.

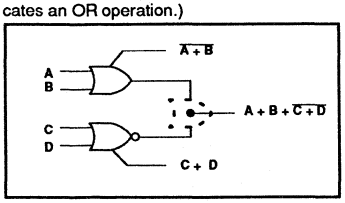


Design of a Logic Diagram

ECL is based on OR/NOR gates. It is easy to transform AND/NAND gates into OR/NOR gates using the Morgan Laws:

$A \bullet B = \overline{A} + \overline{B}$ and $A + B = \overline{\overline{A} \bullet \overline{B}}$

(A B indicates an AND operation, A = B indicates an OR operation.)



Some ECL inputs are non–inverting, as opposed to TTL circuits in which these inputs are inverted; for example, the "clear" and "set to one" inputs (CLEAR and SET). This is due to the difference in design between TTL and ECL, in which the basic gates are AND and OR, respectively. Therefore, to "force" an input signal toward the output, a 0 or a i is applied, respectively. This requirement does not present a problem, because non–inverting and inverting outputs are almost always available on simple circuits.

Other ECL families have been created in the past, but they have not become as widely known as the others. Among them are MECL 1 and MECL 2, which were the original families.

HANDLING

Like MOS circuits, ECL circuits can easily be damaged by electrostatic discharge (ESD). ESD applied to input or an output causes very intense, instantaneous currents. When passing through functions having a small area, these currents can cause a localized fusion of the junction. In the mild case, there will be an increase in the junction leakage current; in the worst case, the junction will be completely short–circuited. The short–circuit can cause a local fusion of the metalizations of the circuit, and the appearance of an open circuit.

The resistance of TTL and MOS circuits to ESD is increased by the addition of diodes or resistor –diode networks. However, this solution has very limited application in ECL, because it introduces parasitic capacitances that impair the speed of the circuits. Protection is instead ensured by simply limiting discharge currents by means of resistors in series.

All insulators can acquire very high charges by rubbing against one another, or due to friction with moving air. Surface potentials of several tens of kilovolts are found on work surfaces (laminate, PVC), on floor covering (plastic flooring, pile carpeting), and on synthetic fabrics (nylon and acrylic). For the sake of prevention, conductive covering are recommended for floors and work surfaces, connected to ground by resistive paths (1M ohm for example). Most risks can be avoided by having operators wear resistive wristbands connected to the work surface. But complete protection must also include a sprayed layer of anti–static varnish on all insulating portions of tools; or also (if applicable) an ionized air blower, to remove charges from untested surfaces.

Signetics' ECL devices are shipped in conducting foam or anti–static tubes and foil–lined boxes to minimize ESD during shipment and unloading.

Before opening the shipment of ECL devices, make sure that the individual is grounded by a wrist–band connected to ground by a 1M Ohm resistor and all handling means (such as tools, fixtures, benches, and chairs) grounded through a 1 M ohm resistor.

After removal from the shipping material, the leads of the ECL devices should always be grounded. In other words, ECL devices should be placed leads–down on a grounded surface, since ungrounded leads will attract static charges.

Before assembly of ECL devices, again make sure the individual is grounded by a wrist–band connected to ground by a 1M Ohm resistor and all handling means (such as tools, fixtures, benches, and chairs) grounded through a 1M ohm resistor.

Do not insert or remove ECL devices in sockets with power applied. Ensure that power transients, such as occur during power turn on–off, do not exceed absolute maximum ratings.

After assembly on PC boards, ensure that ESD is minimized during handling, storage, or maintenance.

ECL inputs should never be left floating on a PC board. As a temporary measure, a resistor greater than 10k ohm should be soldered on the open input. The resistor will limit accidental damage if the PC board is removed and brought into contact with static–generated materials.

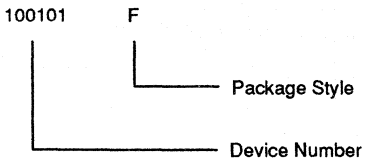
Ordering Information

ECL Products

Signetics ECL products are available in 16–pin plastic and ceramic packages for 10K ECL and 24–pin ceramic, 24–pin flat and 28–pin PLCC packages for 100K ECL with two temperature ranges (–30°C to +85°C for 10K ECL and 0°C to +85°C for 100K ECL). The ordering code for the devices is an alphanumeric sequence as explained below. The ordering codes in the individual data sheets indicate the normal or planned availability of the product. However, the availability of the specific part numbers can be obtained from local Signetics sales office, Signetics representatives or authorized distributors. A complete listing is located in the back of this handbook.

Table 1 provides part number definition for Signetics ECLs. The Signetics part number system allows complete ordering information to specified in the part number. The part number and product description is located on each data sheet.

Signetics ECL Part Numbering System



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
T_A = –30°C to +85°C	10100	N = Plastic DIP F = Ceramic DIP D = Plastic SO
T_A = 0°C to +85°C	100101	F = Ceramic DIP Y = Ceramic Flat Pack A = PLCC (Plastic Leaded Chip Carrier)

Product Status

ECL Products

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	Formative or In Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Section 1
Selection Guides

INDEX

Alphanumeric Index 3
Functional Selection Guide 5

Alphanumeric Index

ECL Products

10H20EV8	ECL Programmable Array Logic	639
10100	Quad 2–Input NOR Gate With Strobe	81
10101	Quad 2–Input OR/NOR Gate With Strobe	85
10102	Quad 2–Input NOR (3 NOR and 1 OR/NOR Gate	89
10103	Quad 2–Input OR (3 NOR and 1 OR/NOR) Gate	93
10104	Quad 2–Input AND Gate	97
10105	Triple 2–3–2 Input OR/NOR Gate	101
10106	Triple 4–3–3 Input NOR Gate	105
10107	Triple 2 Input Exclusive–OR/Exclusive–NOR Gate	109
10108	Dual 4–Input AND/NAND Gate	113
10109	Dual 4–5 Input OR/NOR Gate	118
10110	Dual 3 Input/3–Output OR Gate (Line Driver)	122
10111	Dual 3 Input/3–Output NOR Gate (Line Driver)	126
10113	Quad Exclusive OR Gate With Enable	130
10114	Triple Differential Line Driver	134
10115	Quad Differential Line Driver	140
10116	Triple Differential Line Driver	145
10117	Dual 2–Wide 2–3 Input OR–AND/OR–AND–INVERT Gate	150
10118	Dual 2–Wide 3–Input OR–AND Gate	155
10119	4–Wide 4–3–3 Input OR–AND Gate	159
10121	4–Wide 4–3–3 Input OR–AND/OR–AND–INVERT Gate	164
10123	Triple 4–3–3 Input Bus Driver	169
10124	Quad TTL–to–ECL Translator	175
10125	Quad ECL–to–TTL Translator	181
10129	Quad TTL–to–ECL Translator	188
10130	Dual D–Type Latch	197
10131	Dual D–Type Master–Slave Flip–Flop	203
10132	Dual 2–Input Multiplexer With Clocked D–Type Latches and Common Reset	210
10133	Quad Latch With D–Type Inputs and Enable Outputs	216
10134	Dual 2–Input Multiplexer With Clocked D–Type Latches	222
10135	Dual J–K Master–Slave Flip–Flop	228
10136	Universal Hexadecimal Counter	233
10137	Universal Decade Counter	240
10141	4–Bit Universal Shift Register	247
10149	1K–Bit ECL Bipolar PROM (256 X 4)	615
10149A	1K–Bit ECL Bipolar PROM (256 X 4)	619
10149B	1K–Bit ECL Bipolar PROM (256 X 4)	623
10158	Quad 2–to–1 Multiplexer, Non–Inverting	252
10159	Quad 2–to–1 Multiplexer, Inverting	256
10160	12–Bit Parity Checker/Generator	260
10161	1–of–8 Decoder With Two Enable Inputs (Active Low Outputs)	264
10162	1–0f–8 Decoder With Two Enable Inputs (Active High Outputs)	268
10164	8–Input Multiplexer With Enable Input	272
10165	8–Input Priority Encoder	276
10171	1–of–8 Decoder With One Common and Two Individual Inputs (Active Low Outputs)	281
10172	1–of–8 Decoder With One Common and Two Individual Inputs (Active High Outputs)	285
10173	Quad 2–Input Multiplexer With Latched Outputs	289
10174	Dual 4–to1 Multiplexer With Latched Outputs	294

Alphanumeric Index

10175	Quint D–Latch With Common Reset and 2–Wired–OR Common Clock Inputs	298
10176	Hex D–Type Master–Slave Flip–Flop	303
10179	Look–Ahead Carry Block	307
10180	4–Bit Arithmetic Logic Unit/Function Generator	311
10181	4–Bit Arithmetic Logic Unit/Function Generator	316
10188	Hex Buffer With Enable (Non–Inverting)	323
10189	Hex Buffer With Enable	327
10192	Quad Open Collector Bus Driver	331
10210	High speed Dual 3 Input/3–Output OR Line Driver	336
10211	High speed Dual 3 Input/3–Output NOR Line Driver	340
10216	Triple Differential OR/NOR Line Receiver (High Speed)	344
10231	Dual D–Type Master–Slave Flip–Flop (High Speed)	349
100101	Trple 5–Input OR/NOR Gate	357
100102	Quint 2–Input OR/NOR Gate With Enable	362
100107	Quint Exclusive OR/Exclusive NOR Gate With Compare Output	367
100112	Quad Driver	373
100113	Quad Driver (High speed)	378
100114	Quint Differential Line Receiver	383
100117	Triple 1–2–2 Input OR–AND/OR–AND–INVERT Gate	389
100118	Quint 2–4–4–4–5 Input OR–AND Gate	394
100122	9–Bit Buffer	399
100123	Bus Driver	403
100124	Hex TTL–to–ECL Translator	409
100124A	Hex TTL–to–ECL Translator (low power)	409
100125	Hex ECL–to–TTL Translator	416
100126	9–Bit Backplane Driver	423
100131	Triple D–Type Master–Slave Flip–Flop	427
100136	Counter/Shift Register	436
100141	8–Bit Shift Register	447
100149	1K–Bit ECL Bipolar PROM (256 X 4)	627
100149A	1K–Bit ECL Bipolar PROM (256 X 4)	631
100149B	1K–Bit ECL Bipolar PROM (256 X 4)	635
100150	Hex D–Type Latch	455
100151	Hex D–Type Master–Slave Flip–Flop	462
100155	Quad 2–Way Multiplexer/Latch	469
100158	8–Bit Shift Matrix	476
100160	Dual 9–Bit Parity Checker/Generator/8–Bit Comparator	481
100163	Dual 8–Input Multiplexer	486
100164	16–Input Multiplexer	492
100165	Universal Priority Encoder	498
100166	9–Bit Comparator	505
100170	Universal Demultiplexer/Decoder	510
100171	Triple 4–Input Multiplexer	516
100175	100K–to–10K Translator	522
100179	Carry Look–Ahead Generator	529
100180	High speed 6–Bit Adder	536
100181	4–Bit Binary/BCD ALU	542
10020EV8	ECL Programmable Array Logic	639
100231	Triple D–Type Master–Slave Flip–Flop (High speed version of 100131)	552
100255	Quint Bidirectional 100K–to–10K Translator	561
100790	9–Bit Transceiver	572
100982	Hex ECL–TTL Translating Transceiver with Registers	579
100984	Quad ECL–TTL Translating Transceiver with Registers	593
100990	9–Bit Transceiver	606

Functional Selection Guide

ECL Products

GATES

FUNCTION	DEVICE NUMBER
OR/NOR GATES	
Triple 4–3–3 input NOR	10106
Quad 2–input NOR with strobe	10100
Dual 4–5 input OR/NOR	10109
Triple 2–3–2 input OR/NOR	10105
Triple 5–input OR/NOR	100101
Quad 2–input OR/NOR (one input common)	10101
Quint 2–input OR/NOR with common enable input	100102
Quad 2–input NOR (one input common)	10102
Quad 2–input OR (3 OR and 1 OR/NOR)	10103
EXCLUSIVE–OR/NOR GATES	
Quad Exclusive–OR with enable input	10113
Triple 2–input Exclusive–OR/Exclusive–NOR	10107
Quint Exclusive–OR/Exclusive–NOR with compare output	100107
AND, AND/NAND GATES	
Dual 4–input AND/NAND	10108
Quad 2–input AND	10104
OR–AND–INVERT COMBINATION	
Dual 2–wide 3 input OR–AND	10118
4–wide 4–3–3–3 input OR–AND	10119
Dual 2–wide 2–3 input OR–AND/OR–AND–INVERT	10117
4–wide OR–AND/OR–AND–INVERT	10121
Triple 1–2–2 input OR–AND/OR–AND–INVERT	100117
Quint 2–4–4–4–5 input OR–AND/OR–AND–INVERT	100118

FLIP–FLOPS

FUNCTION	DEVICE NUMBER	COMMON CLOCK	CLOCK ENABLE	SET	RESET
Dual D–type master–slave	10131	Low	Low	Low	Low
Dual D–type master–slave (high–speed)	10231	Low	Low	Low	Low
Triple D–type master–slave	100131	Low	Low	Low	Low
Triple D–type master–slave (high–speed)	100231	Low			
Hex D–type master–slave	10176	Low			
Hex D–type master–slave	100151				Low
Dual J–K master–slave	10135	Low	Low	Low	Low

Functional Selection Guide

LATCHES

FUNCTION	DEVICE NUMBER	COMMON CLOCK	RESET	CLOCK ENABLE	OUTPUT
Dual D–type 2–input multiplexer, clock, and common reset	10132	High	High	Low	True, Comp
Dual D–type 2–input multiplexer, clock, and common reset	10134	Low	High	Low	True, Comp
Triple D–type	100130	Low		Low	True
Quad with D–type inputs and enable outputs	10133	High		Low	Comp
Quint D–type with common reset, and 2 wired–OR common clock inputs	10175	Low	Low		True
Hex D–type	100150		Low	Low	True, Comp

MULTIPLEXER

FUNCTION	DEVICE NUMBER	ENABLE INPUT	SELECT INPUTS	OUTPUT
Quad 2–to–1, non–inverting	10158		S	True
Quad 2–to–1, inverting	10159	Low	S	Comp
8–input with enable input	10164	Low	A_{S0}, A_{S1}, A_{S2}	True
Quad 2–input with latch outputs	10173	Low	D_S	True
Dual 4–to–1 with enable input	10174	Low	A, B	True
Quad multiplexer/latch	100155	Low	S_0, S_1	True & Comp
Dual 8–input	100163		S_0, S_1, S_2	Comp
Triple 4–input with enable input	100171	Low	S_0, S_1	True & Comp
16–input	100164		S_0, S_1, S_2, S_3	Comp

DECODER/DEMULTIPLEXER

FUNCTION	DEVICE NUMBER	ADDRESS INPUT	ENABLE LEVEL	OUTPUT LEVEL
1–of–8 decoder with 2 enable inputs (active Low outputs)	10161	3	2 (Low)	8 (Low)
1–of–8 decoder with 2 enable inputs (active High outputs)	10162	3	2 (Low)	8 (High)
Dual 1–of–4 decoder with one common and two individual inputs (active Low outputs)	10171	2	2 (HIGH), 1 (Low)	1 (Low)
Dual 1–of–4 decoder with one common and two individual inputs (active High outputs)	10172	2	2 (Low), 1 (High)	8 (High)
Universal demultiplexer/decoder	100170	5	4 (Low)	8 (High)

REGISTER/SHIFT REGISTER

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK EDGE
4–bit universal shift register	10141	4	D_n	D_0, D_1, D_2, D_3	↑
8–bit shift register	100141	8	D_n	P_0.....,P_7	↑
8–bit shift matrix	100158	8		D_0,.....,D_7	

Functional Selection Guide

COUNTERS

FUNCTION	DEVICE NUMBER	MODULUS	PARALLEL ENTRY	PRESETTABLE	CLOCK EDGE
Universal hexadecimal	10136	16	Synchronous	X	↑
Universal decade	10137	10	Synchronous	X	↑
4–stage counter/shift register	100136	4	Synchronous	X	↑

BUS AND LINE DRIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Dual 3–input/3–output OR line driver	10110	True
High–speed dual 3–input/3–output OR line driver	10210	True
Dual 3–input/3–output NOR line driver	10111	Complement
High–speed dual 3–input/3–output NOR line driver	10211	Complement
Triple 4–3–3–input bus driver	10123	Complement
Quad current–mode differential bus driver	10192	True & Complement
Quad driver	100112	True & Complement
Quad driver (high–speed)	100113	True & Complement
Hex bus driver	100123	True
9–bit backplane driver	100126	True

RECEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Triple differential line receiver	10114	True & Complement
Quad differential line receiver	10115	True
Triple differential line receiver	10116	True & Complement
Triple differential line receiver (high–speed)	10216	True & Complement
Quint differential line receiver	100114	True & Complement

BUFFERS AND INVERTERS

FUNCTION	DEVICE NUMBER	OUTPUT
Hex buffer with enable input, non–inverting	10188	True
9–gate buffer	100122	Complement
Hex inverter with enable input	10189	Complement

Functional Selection Guide

TRANSLATORS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad TTL–to–ECL translator	10124	True & Complement
Quad TTL–to–ECL translator	10129	True & Complement
Hex TTL–to–ECL translator	100124	True
Quad ECL–to–TTL translator	10125	True
Hex ECL–to–TTL translator	100125	True
100K–to–10K translator	100175	True
TTL–to–100K bidirectional translating Transceiver	100255	Complement
9–Bit Transceiver	100790	True
Hex ECL–TTL Translating Transceiver	100982	True
Quad ECL–TTL Translating Transceiver	100984	True
9–Bit Transceiver	100990	True

PRIORITY ENCODERS

FUNCTION	DEVICE NUMBER	INPUT ENABLE (LEVEL)	INPUT/OUTPUT (LEVEL)
8–Input	10165	Low	Active Low
Universal	100165	Low	Active Low

ARITHMETIC FUNCTIONS

FUNCTION	DEVICE NUMBER
4–bit arithmetic logic unit/function generator	10181
4–bit binary/BCD ALU	100181
High–speed 6–bit adder	100180
Dual 2–bit adder/subtractor	10180
Look–ahead carry block	10179
Carry look–ahead generator	100179

COMPARATORS

FUNCTION	DEVICE NUMBER
9–bit comparator	100166
Dual 9–bit parity generator/8–bit comparator	100160

Functional Selection Guide

PROMS

FUNCTION	DEVICE NUMBER
1K–Bit ECL Bipolar PROM (256 X 4)	10149
1K–Bit ECL Bipolar PROM (256 X 4)	100149
1K–Bit ECL Bipolar PROM (256 X 4)	10149A
1K–Bit ECL Bipolar PROM (256 X 4)	100149A
1K–Bit ECL Bipolar PROM (256 X 4)	10149B
1K–Bit ECL Bipolar PROM (256 X 4)	100149B

PALS

FUNCTION	DEVICE NUMBER
ECL programmable logic array	10H20EV8
ECL programmable logic array	10020EV8

Section 2
Quality and Reliability

Quality and Reliability

ECL Products

AMIC SIGNETICS ASSURANCE PROGRAM

SIGNETICS QUALITY PROGRAM

In 1979, Signetics recognized that quality was becoming a major competitive issue, not only in the semiconductor business but also in other industries. Increases in the volume of products imported from the Far East (steel, automobiles, and consumer products) sent strong signals that new competitive forces were at work.

Signetics quickly began to investigate a variety of quality programs. The company realized that quality improvement would require a contribution from all employees. Management commitment and participation, however, was recognized as the primary prerequisite for this program to work successfully. Resources required for the resolution of defects under management control.

In 1980, Signetics developed a program which focused on quality management. Rearranging previous quality control philosophies, Signetics developed a decentralized, distributed quality organization and simultaneously installed a quality improvement process based on the 14–Step improvement program advocated by Phil Crosby. The process was formally begun company–wide in 1981. Since then substantial progress has been made in every aspect of Signetics' operations. From incoming raw material conformance to improvements in clerical errors — every department and individual is involved and striving for Zero Defects. Zero Accept sampling plans and Zero Defects warranties are evidence of Signetics' ongoing commitment and progress in quality.

Today, Signetics' quality improvement process has had a far–reaching impact on all aspects of our business. Signetics provided its customers with products of refined electrical and mechanical quality. And through continual use and modification of the Crosby program, Signetics is providing itself with well–defined method of managing ongoing improvement efforts.

SIGNETICS' ZERO DEFECTS WARRANTY

In recent years, American industry has demanded increased product quality of its IC suppliers in order to meet growing international competitive pressure. As a result of this quality focus, it is becoming clear that what once thought to be unattainable— Zero Defects— is, in fact achievable.

Signetics offers a Zero Defects Warranty which states that it will take back an entire lot if a single defective part is found. This precedent setting warranty has effectively ended the IC industry's "war of the AQLs" (Acceptable Quality Levels). The ongoing efforts of IC suppliers to reduce PPM (Parts Per Million) defect levels is now a competitive customer service measure. This intense commitment to quality provides an advantage to today's electronics OEM. That advantage can be summed up in four words: ***Reduced Cost of Ownership.***

As IC customers look beyond purchase price to the total cost of doing business with a vendor, it is apparent that a quality–conscious supplier like Signetics, represents a viable cost reduction resource. Consistent high–quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures.

SIGNETICS' STATISTICAL PROCESS CONTROL (SPC)

Although application of statistics in our process development and manufacturing activities goes back to the early 1970's, the corporate–wide emphasis on Statistical Process Control (SPC) did not come until mid–1984.

A natural evolution of our quality process made introduction of SPC and other related programs an inevitable event. SPC was, therefore, introduced under the quality umbrella.

The objective of the SPC programs to introduce a systematic and scientific approach to business and manufacturing activities. This approach utilizes sound statistical theory. Managers are expected to be able to turn data into information, and make decisions solely on data (not perception).

The most critical and challenging aspect of implementing SPC is establishment of a discipline within the operating areas so that decision making is fundamentally based on verifiable data, and actions are documented. The other is realization of the fact that statistical tools merely point out the problems and are not solutions by themselves. The burden of action on the process is still on the implementers' shoulders. In order to implement SPC effectively, three steps are continually followed:

Documenting and understanding the process, using process flow charts and component diagrams.

Establishing data collection systems, and using SPC tools to identify process problems and opportunities for improvement.

Acting on the process, and establishing guidelines to monitor and maintain process control.

Repeating steps 1–3 again.

These fundamentals are the basis of establishing Signetics' specifications and operating philosophy with respect to SPC. Signetics believes a solid foundation creates a permanent system and accelerates our quality improvement process.

SIGNETICS QUALITY PERFORMANCE

Signetics Quality Improvement Program has influenced our entire production cycle – from the purchases of raw materials to the shipment of finished product. The involvement of all areas of the company has resulted in impressive quality improvements. A traditional quality gauge is final product electrical and visual–mechanical defect levels as measured upon first submittal results at Signetics outgoing Quality Assurance gates; Estimated Process Quality (This is the PPM Level at our first outgoing inspection for all accepted and rejected lots.)(Figure 1 and 2). Current product shipments routinely record below 20PPM (Parts Per Million) electrical defect levels and 150PPM visual–mechanical defect levels. Since Signetics utilizes zero accept sampling on all finished production inspection, any lot with one or more rejects is 100 percent rejected.

The most meaningful measure is our product quality is how we measure up to our customer's expectations. Many customers routinely send us incoming inspection data on our products. One major mainframe manufacturer has reported zero defects in electrical, visual–mechanical, and hermeticity and has reported a 100 percent lot acceptance rate on Signetics' Standard Products Group product for over a year. Due to this type of performance, an increasing number of our customers are eliminating expensive incoming inspection testing and have begun implementation of Signetics' Ship–to Stock Program.

Quality and Reliability

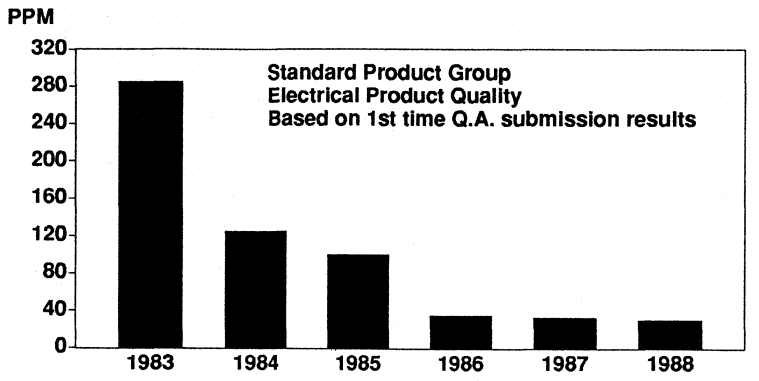


Figure 1

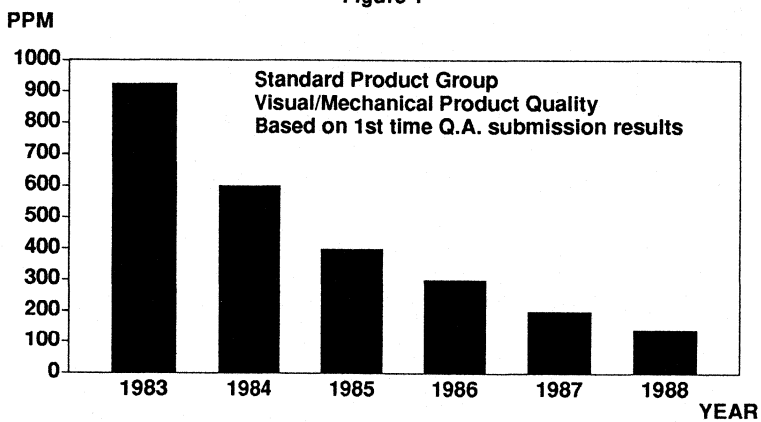


Figure 2

SIGNETICS SHIP–TO–STOCK PROGRAM

Ship–to–Stock is a formal program developed at the request of our customers to help them reduce their costs by eliminating incoming test and inspection. Through close work with these customers in our quality improvement program, they became confident that our defect rates were so low that the redundancy of incoming inspections and testing was not only expensive, but unnecessary. They also saw that added component handling increased the potential of causing defects.

Ship–to–Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into the customer's assembly line or inventory. This program was developed at the request of several major manufacturers after they had worked with us and had a chance to experience the data exchange and joint corrective action occurring as part of our quality improvement program.

Manufacturer using large volumes of ICs, those who are evaluating Just–in–Time delivery programs, or those who want to reduce or avoid high–cost incoming inspection are strongly encouraged to participate in this worthwhile program. Contact your local Signetic's sales representative for further assistance and information on how to participate in this program.

SUMMARY

The Signetics Quality Improvement Program has had a far–reaching impact on all aspects of our business. It has, of course, provided our customers with products of improved electrical and mechanical quality and has provided Signetics with a method of managing product reliability improvement to ensure that Signetics' products continue to perform as specified.

The corrective action teams that work to eliminate the cause of defects in Signetics' products are committed to producing highly reliable integrated circuits and, as demonstrated by our continually improved product reliability

Quality and Reliability

performance, we are well on the way to achieving our objective, **ZERO DEFECTS**.

RELIABILITY ASSURANCE PROGRAMS

FOCUS ON PRODUCT RELIABILITY

During the period from 1981 to 1984, continuing improvements in process and material quality had a significant impact on product reliability. Since 1984, Signetics has intensified its effort to markedly improve product reliability. Corporate Reliability Engineering, Group and Plant Reliability Units, Philips Research Labs–Sunnyvale, and Manufacturing Engineering work jointly on numerous improvement activities. These focused activities enhance the reliability of Signetics future products by providing improved methods for reliability assessment, increased understanding of failure physics, advanced analytical techniques, and aid in the development of material and processes.

RELIABILITY MEASUREMENT PROGRAMS

Signetics has developed comprehensive product and process qualification programs to assure that its customers are receiving highly reliable products for their critical applications. Additionally, ongoing reliability monitoring programs, SURE III and Product Monitor, sample standard production on a regularly established basis (see Table I below).

Table I Reliability Assurance Programs

Reliability Function	Typical Stress	Frequency
New Process Qualification	High Temperature Operating Life Temperature–Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each new wafer fab process
New Product Qualification	High Temperature Operating Life Temperature–Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle Electrostatic Discharge Characterization	Each new product family
SURE III	High Temperature Operating Life Temperature–Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each fab process family, every four weeks
Product Monitor	Pressure Pot	Each package types and technology family at each assembly plant, every week

DESCRIPTION OF STRESSES

SHTL–Static High Temperature Life:
SHTL stressing applies static DC bias to the device. This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive contaminants to the silicon surface. The voltage bias must be maintained until the device are cooled down to room temperature from the elevated life test temperature. DHTL stressing is not as effective in detecting such problems because the bias continuously changes, intermittently generating and healing the problem. For this reason, SHTL has typically been used as the accelerated life stress for Standard Product products.

HTSL–High Temperature Storage Life:
This stress exposes the parts to elevated temperatures (150°C–175°C) with no applied bias. For plastic packages, 175°C is the high end and of its safe temperature region without accelerating untypical failure mechanisms. This test is intended to accelerate mechanical package–related failure mechanism such as Gold–Aluminium bond integrity and other process instabilities.

THBS–Temperature–Humidity, Biased, Static:
The accelerated temperature and humidity bias is performed at 85°C and 85% relative humidity (85°C/ 85% RH). In general, the worst case bias condition is the one which minimizes the device power dissipations and maximizes the applied voltages. Higher power dissipations tend to lower the humidity level at the chip surface and lessen the corrosion susceptibility.

TMCL–Temperature–Cycling, Air to Air:
The device is cycled between the specified upper and lower temperature without power in an air or Nitrogen environment. Normal temperature extremes are –65°C and +150°C with a minimum 10 minute dwell and 5 minute transition per MIL–STD–883C, Method 1010.5, Condition C. This is a good test to measure the overall package to die mechanical compatibility, because the thermal expansion coefficients of the plastic are normally very much higher than those of the die and leadframe. However, for large die the stress may be too severe and induce failures that would not be expected in a real application.

PPOT–Pressure Pot:
This stress exposes the devices to saturated steam at elevated temperature and pressure. The standard condition is 20 PSIG which occurs at a temperature of 127°C and 100% RH. The stress is used to test the moisture resistance of plastic encapsulated devices. The plastic encapsulant is not a moisture barrier and will saturate with moisture within 72 hours. Since the chip is not powered up the chip temperature and relative humidity will be the same as the autoclave once equilibrium is reached. Because the steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, it is effective at detecting corrosion problems, contamination induced leakage problems, and general glassivation stability and integrity. It is also a good test for both package integrity (cracks in the package), and for die cracks (the moisture swells the plastic enough to stress the die–also the moisture causes leakage paths in the crack itself).

PRODUCT AND PROCESS PROGRAMS

Qualification activity is centered around new products and processes and changes in products and processes. The goal is to assure that the products can meet the qualification requirements prior to general release, and on an ongoing basis to demonstrate conformance to those

Quality and Reliability

requirements. The nature and extent of reliability stressing required depends on the type of change and the amount of applicable reliability data available.

A full qualification may include Early Failure Rate (EFR), intrinsic Failure Rate (IFR), and Environmental Endurance Stressing. Such stress plans are reserved for introductions or changes that involve new or untested material or processes and, as such should be subjected to the maximum reliability interrogation. This normally entails a full range of biased and unbiased temperature and humidity stresses along with thermo–mechanical stresses.

For changes that are of limited scope, the full range of qualification stressing may not be warranted. In these instances, the nature and extent of the change is examined and only those stresses which provide a valuable measure of the change, or those which will detect potential weaknesses, are performed.

SIGNETICS'SELF–QUAL PROGRAM (SSQP)

Self–Qual is a joint program between Signetics and a customer which formally communicates Signetics' qualification activities for a new or changed product, process, or material. The Signetics Self Qual process provides our customer's engineering groups an opportunity to participate in the development of the qualification plan. During the qualification process, customers may audit the project, and can receive interim updates of qualification progress. Upon completion, formal detailed engineering reports are provided.

The major impact to the customer comes from the reduced workload on the component engineering and qualification groups. These engineering resources generally divide their time between routine qualification activity and problem resolution on critical components. By eliminating the need to perform qualification for one of the basic vendor changes the customer component engineer can spend more of his time resolving the critical product issues. In addition, the total amount of stress hardware needed to perform qualification life tests and other environmental evaluations can be reduced, saving the customer facility costs and reducing operating expense.

Self–Qual is a no–risk proposition for the customer. Each Self–Qual proposal provides a detailed description of what we are changing and why. It includes a detailed plan of what we intend to do to establish the reliability of the products affected. If the customer wishes to have product added to the plan or select some additional stresses, or prefers alternative stress conditions, Signetics will do everything possible to accommodate those requests. After that, if the customer is still uncomfortable with the recommended change, they are under no obligation to accept our data, and they may perform their own qualification program in addition to Signetics.

Customers who are interested in participating in this program should contact their local Signetics sales representative or Signetics Corporate Reliability Engineering department directly.

SURE III RELIABILITY MONITORING PROGRAM

In order to implement an improvement program, a standard measure of performance was needed. Signetics uses the results from the SURE III Reliability Monitoring Program as its basic ongoing measure of product reliability performance. This program samples all generic families of products manufactured by Signetics, and utilizes standardized stress methods and test procedures. This system is augmented by new product and process qualification activities and infant mortality monitoring programs.

Signetics adopted a measurement philosophy based on the premise of continual improvement toward our performance standard of zero defects.

We also increased our standard Pressure Pot stress conditions from 15 PSIG/121°C to 20 PSIG/127°C. This reduced stress duration from 168 hours to 72 hours, and increased high volume sampling, which increased sensitivity to low defect levels.

Our standard monitoring program, SURE III, includes the stress conditions as described in Table II.

PRODUCT MONITOR

In addition to the SURE III program, each Signetics assembly plant performs Pressure Pot (20PSIG, 127°C, 72hours) reliability monitors on a weekly basis for each molded package type by pin count. The purpose of this program is to monitor the consistency of the assembly operations for such attributes as molding quality and die attach and wire bond integrity. This data is reported back to manufacturing operations and corporate and group reliability and quality assurance departments by electronic mail each week.

RELIABILITY EVALUATIONS

In addition to the product performance monitors encompassed in the SURE III program, Signetics' Corporate and Group Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

Evaluation and qualification of new or changed materials, assembly/wafer–fab processes and equipment, product designs, facilities, and subcontractors.

Devices or generic group failure rate studies.

Advanced environmental stress development.

Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE III program, however, more highly –accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power–temperature cycling, and cycle–biased temperature–humidity, are often included in some evaluation programs.

STRESS FACILITY QUALITY

Signetics quality improvement has reached all functional areas of the company, and the reliability stress laboratories are no exception. Corporate Reliability Laboratory (CRL) is one of the many areas where the benefits of the quality improvement process pays repeated dividends.

Quality and Reliability

Table II SURE III Reliability Monitoring Programs

Reliability Function	Stress Conditions
Static High Temperature Operating Life (SHTL)	Tj ≥ 150°C, T_A = 125°C to 150°C, Biased condition = Static. V_{CC} = MAX, Duration = 1000 hours
High Temperature Storage Life (HTSL)	T_A = 150°C, Biased condition = None, Duration = 1000 hours
Temperature–Humidity, Biased, Static (THBS)	T_A = 85°C ± 3°C, Humidity = 85% RH ± 5%, Biased condition = Static, V_{CC} = MAX, Duration = 1000 hours
Temperature Cycling (TMCL)	T_A = –65°C ⟨ +0°C –10°C) to +150°C ⟨ +10°C –0°C), Air–to–Air, Dwell time = 10 minutes minimum each extreme, Biased condition = None, Duration = 1000 cycles for plastic package, 300 cycles for ceramic package
Pressure Pot	T_A = 127°C ± 2°C, 20 PSIG ±0.5 PSIG (PPOT). 100% saturated steam, Biased condition = None, Duration = 72 hours

NOTE : V_{CC} = MAX is generally equal to V_{CC} = MAX as specified in Data Manual

CRI utilizes stress which accelerate failure rates hundreds to thousands of times, requiring precision and control to make reliability data meaningful. Stress loading schedules are maintained with absolute regularity and chambers are never off–line beyond scheduled loading plans. Board currents are recorded prior to and at each interval on biased stresses, and monitoring of in–oven currents is conducted daily.

Thermal modeling of the Temperature Cycling systems has been accomplished and all loads are carefully weighed to ensure that thermal ramps are consistent.

Pressure Pot and Biased Pressure Pot systems utilize microprocessor controllers, and are accurate to within 0.1 degree centigrade. Saturation is guaranteed via automatic timing circuits, and a host of fail–safe controls ensure that test groups are never damaged.

Electrostatic discharge (ESD) handling precautions are standard procedures in the laboratories, and the occurrences of devices lost, zapped, or overstressed have become almost non–existent.

RELIABILITY IMPROVEMENT PROGRAMS

Currently, Signetics is involved in a number of reliability improvement programs intended to enhance product reliability performance. A series of activities are currently addressing failure rate reduction in thermal cycling stresses, particularly on large die. Other reliability improvement programs involve the use of Silicon Nitride and other technologically advanced passivation systems to increase the high humidity resistance of sensitive products.

Reducing early life failures has become a major focus at Signetics. Numerous corrective action teams are in the process of establishing high volume monitors capable of accurately describing parts per million (PPM) level infant failure rates. From data produces via these monitors, improvement in wafer fabrication process and assembly process technologies are developed to minimize integrated circuits defect levels.

RELIABILITY PUBLICATIONS

Data from from all these activities is made available to all Signetics customers in a variety of publications:

PRODUCT RELIABILITY SUMMARIES AND QUARTERLY UPDATES

Yearly, each Product Group's SURE III monitoring data is summarized and published in a Product Reliabilty Summary.

SSQP – SIGNETICS SELF–QUAL PROGRAM

In addition to the regular publications of reliability monitor results, a special program for the publication of qualification proposals and final engineering reports has been in place since January of 1984.

SMD RELIABILITY

In support of Signetics' leadership in Surface Mount Device (SMD) technology, we have published in–depth studies and evaluations on the reliability of numerous combinations of SMD packages and IC process technologies. These reports cover not only the basic product performance, but also evaluate products after exposure to the unique environments created by the various SMD soldering and cleaning processes.

SPECIAL RELIABILITY REPORTS

In addition to our standard reports, special reliability evaluation results are available on a wide variety of Signetics' products and processes. Custom reports can be generated to meet specific customer needs and the most accurate failure rate estimates can be prepared for your specific system application and environment.

DATA AVAILABILITY

The previously referenced documents are available to all Signetics customers. Many are available in your local Signetics sales office, or:

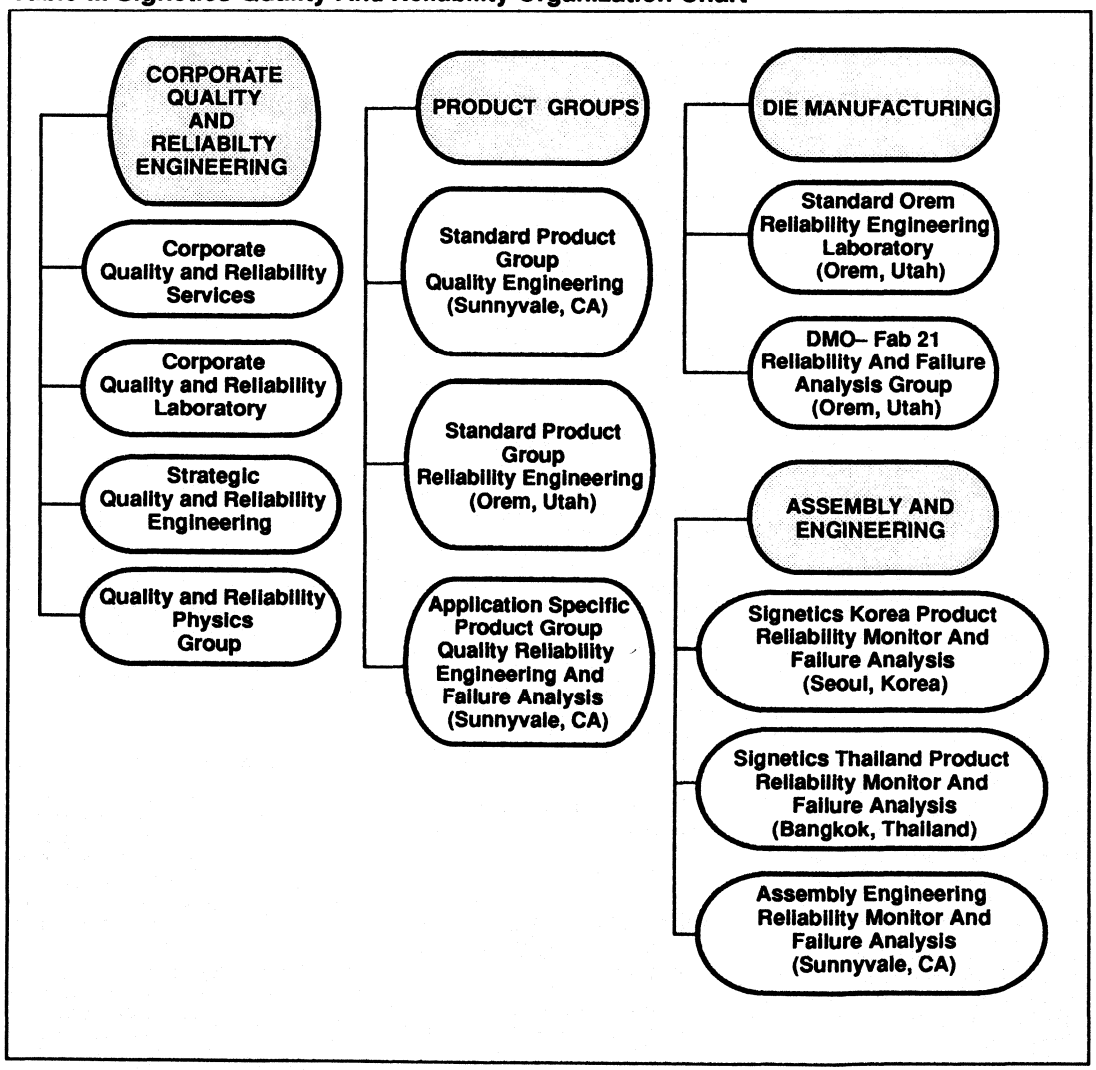
Corporate Reliability Services
Reliability Publications Group
Department 9205, Mail Stop #34
Arques Avenue
P. O. Box 3409
Sunnyvale, CA 94088–3409, USA

where you can be placed on a standard mailing list for all documentation which meet your requirement(s).

Quality and Reliability

The Table III below depicts the current organization for Signetics' Quality and Reliabilty Group.

Table III Signetics Quality And Reliability Organization Chart



Quality and Reliability

SIGNETICS' MANUFACTURING FACILITIES

Signetics, as part of a multinational corporation, utilize manufacturing facilities for wafer fabrication, package assembly, and test in threes states and three overseas countries as shown in Table IV. All wafer fabrication is performed in Signetics operated fabs which report to the Vice President of Die Manufacturing Operations (DMO) in Sunnyvale. Similarly, Signetics Assembly operations in Utah, Korea, and Thailand, report to the Vice President of Assembly Manufacturing Operations (AMO). Assembly subcontractors, Anam, Hyundai, MEC, Peibei, and Team are scheduled and controlled through the AMO organization. Assembly subcontractors process all product to Signetics' specifications and materials. Signetics has on-site quality assurance personnel at each subcontractor to audit assembly processes and procedures.

Table IV Signetics Product Manufacturing

Facilities	Designation	Location	Process or Package Families
Wafer Fabrication	Fab 01	Sunnyvale, California, USA	Bipolar Junction Isolated and Quality Assurance
	Fab 16	Sunnyvale, California, USA	Oxide Isolated, BICMOS and Quality Assurance
	Fab 21	Orem, Utah, USA	Bipolar Gold Doped, Schottky, Oxide Isolated, ECL, and Quality Assurance
	Fab 22	Albuquerque, New Mexico, USA	ACMOS, EPROM and Quality Assurance
Assembly	Anam	Seoul, Korea	SO, PLCC, Metal Can and Quality Assurance
	Hyundai	Ichon, Kyungki, Korea	Ceramic DIP (CERDIP) and Quality Assurance
	MEC	Osaka, Japan	SO EIAJ, QFP 44 and Quality Assurance
	Orem	Orem, Utah, USA	Military Final Test and Quality Assurance
	Pebel	Kaomsiung, Taiwan	PDIP, SO, PLCC, and Quality Assurance
	SigKor	Seoul, Korea	PDIP, SO and PLCC, and Quality Assurance
	Sig Thai	Bangkok, Thailand	PDIP and Ceramic DIP(CERDIP) and Quality Assurance
	Team	Manila, Philippine	PDIP and Quality Assurance
Test	TAO3	Sunnyvale, California, USA	Wafer Sort, Final Test and Quality Assurance
	SigKor	Seoul, Korea	Final Test and Quality Assurance
	SigThai	Bangkok, Thailand	Final Test and Quality Assurance

TYPICAL IC MANUFACTURING FLOW

The manufacturing process for integrated Circuits begins with wafer fabrication. The wafers are then electrically sorted, assembled, and tested prior to customer shipment. Quality assurance inspections are utilized throughout the manufacturing process.

Table V Package Construction

Items	Plastic DIP	SO/PLCC	Ceramic DIP(CERDIP)	Ceramic Flat Pack
Lead Frame	Copper, 194 Alloy	Copper, 194 or PMC102	Alloy–42	Alloy–42
Lead Finish	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40) or Solder Plate (80/20)	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40)
Bond Area Finish	Silver Spot	Silver Spot	Silver Spot	Silver Spot
Die Attach	Silver Filled Polymide or Themoplastic	Silver Filled Polymide or Thermoplastic	Silver Filled Glass	Silver Filled Glass
Bond Wire	Gold, 1.0–1.3 mils in Diameter	Gold, 1.0–1.3 mils in Diameter	Aluminum, 1.0–1.3 mils in Diameter	Aluminum, 1.0–1.3 mils in Diameter
Wire Bonding Die Lead Frame	Thermosonic Ball Stitch	Thermosonic Ball Stitch	Ultrasonic Stitch Stitch	Ultrasonic Stitch Stitch
Package Material	Novolac Epoxy	Novolac Epoxy	Ceramic	Ceramic

Quality and Reliability

Table VI Package Code Definition (For internal use)

Pin count	Plastic DIP	Plastic SO	PLCC	Ceramic DIP	Ceramic Flat Pack
16	NJ1	DJI	–	FJ1	–
24	NN3	–	–	FN1 FN2 FN3	YN1
28	–	–	AQ1	–	–

Section 3
Testing

INDEX

Introduction 23
Chapter 1 DC Testing 23
Chapter 2 AC Testing 25

Chapter 1
DC Testing

ECL Products

INTRODUCTION

The purpose of this section is to assist personnel involved with testing of ECL by discussing various testing methods and techniques needed in testing ECL.

TEST SEQUENCE

ECL testing is usually done in the following sequence: functional testing, DC testing and AC testing.

Functional Testing

The purpose of functional testing is to verify that the device is working. Functional testing is done on the automatic tester by simulating in–circuit condition. The inputs are driven using V_{OH} and V_{OL} limits. The outputs are compared against V_{IH} and V_{IL} values.

DC Testing

It is important to emphasize that the specified limits in the DC Characteristics can be met only after the thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min).

Q_0, Q_1, and Q_3 are the input transistors in this simplified schematic of a 10100. Q_4, D_1, and D_2, and R_9 and R_{10} form the reference voltage supply (V_{BB}). If the voltage at the base of any or all of the input transistors rises above V_{BB}, the transistor will begin to conduct current down through R_6, thus diverting most of the base current away from the output transistor, Q_5. The voltage at the output pin will drop toward V_T via a 50 ohm termination resistor, R_T. If only one input transistor is conducting, all the current that is diverted away from Q_5 will flow through it.

Threshold measurement is the most difficult DC parameter to test on the automatic tester. If all inputs are at threshold simultaneously, the device may tend to oscillate when in a test environment.

In addition, the primary reason for testing input thresholds is for checking noise immunity. Since noise immunity is defined as the difference between the input level at threshold and its associated output level, only one input at a time can be tested in order to achieve accurate results.

Although suggested test conditions are described for V_{OH}, V_{OHT}, V_{OL}, and V_{OLT}, they are not necessary worst case. The following is a recommendation as to what to look for in considering output voltages in the worst case.

V_{OH} and V_{OL} path levels on ECL devices are somewhat current dependent, i.e., the output voltage level can vary depending on how the output is being driven by the internal circuitry. Also, the effect is different for V_{OH} than for V_{OL}. This can be explained by analyzing the circuit Figure 1.

If two input transistors are conducting, that same amount of current will be split evenly by each transistor. Since the saturation resistance (R_{SAT}) of any transistor is not zero, a smaller voltage drop will result causing a slightly lower voltage at the output.

If all three input transistors are conducting, that same amount of current will be split three ways and a still lower voltage will result. Since the most negative output voltage is V_{OLMIN}, the above condition would represent the worst case of that test. Therefore, if the most positive Low state is V_{OLMAX}, the worst–case condition for that would be with only one input transistor conducting. It is advisable to test V_{OLMAX} with each input High, one at a time.

In the case of V_{OH}, there is only one possibility– all inputs Low– so it is not necessary (or possible) to test anything but that one condition.

It is fairly simple to see from the above example what the worst cases are for most gates (provided a schematic is available). As the circuitry advances into flip–flops and beyond into the even more advanced functions, the worst–case conditions become a little more difficult to determine, although the philosophy remains the same.

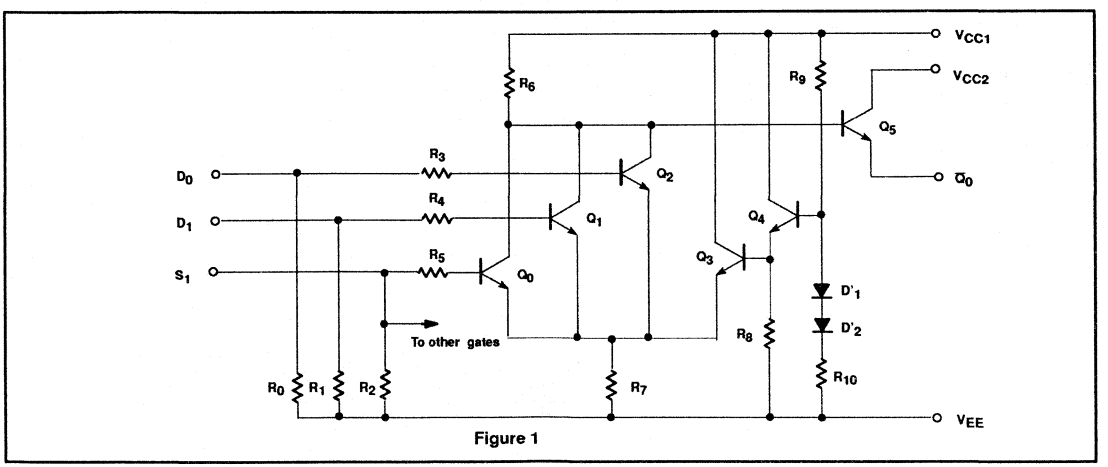


Figure 1

DC Testing

The easiest way to determine how the output is affected is to start at the base of the output transistor to see what components directly drive it, then determine all of the possible combinations from all of the available inputs. Of course, only the worst possible combinations need to be tested.

When testing inverting circuits, the parameter that is usually affected is V_{OL}; but in non–inverting circuits, V_{OH} is path dependent. Referring to the simplified schematic of a 10101 in Figure 2, the inverting output is affected the same as in the previous example but this device also has a non–inverting output from the emitter of Q_3. With both inputs Low Q_4 diverts most of the base current away from the base of Q_3, thus the output is Low and that is the only Low state condition that can exist.

If one input goes High, most of the current from R_5 can now flow into the base of Q_3 pulling the emitter High. If the other input transistor goes High also, the voltage drop will be shared equally between Q_1 and Q_2 and the voltage at their emitters could rise a few millivolts. In turn, the emitter of Q_4 will rise along with the collector of Q_4, the base of Q_3 and therefore the output emitter. So the base of the worst–case V_{OHMAX} test of this device would be with both inputs High for the worst–case V_{OHMIN} would be with only one input High at a time.

Every effort has been made to include simplified circuit schematics for all devices in the limited space of this databook to aid the intesting and circuit design with Signetics' ECL devices.

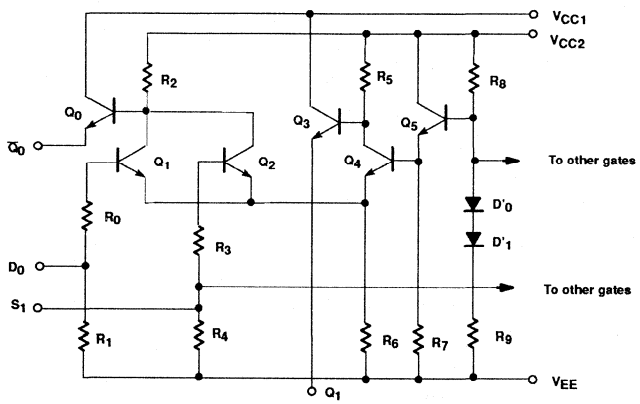


Figure 2

Power Supply	Current capability	Since ECL is noted for high current requirements, power supplies fo V_{EE} should be capable of supplying current with a 25% reserve over the highest powered part. The power supply must provide well over 1 Ampere.
Power Supply	Noise–free power supply current	Since the voltage swing on ECL input and output level is only about 800mV, it is important that the power supplies be extremely clean and free of spikes, hum, or other types of noise.
Pulse Generator	DC resolution	Since the threshold measurements require that input voltage be extremely accurate and repeatable, the driver and the output comparator should have an accuracy of ±1mV.
Pulse Generator	Edge rates	It is important that the rise and fall time of the clock pulses be fast, clean, and free from overshoot.
Sampling Scope	Rise time	The sampling scope should be able to handle rise time of 100ps and preferably should have a digital display for easier readout.
Test Fixture	Contact resistance	Contact resistance between the device pins and test pins should be kept to less than 50 milliohm to avoid oscillation. Free length of contact (portion not matched to 50 ohm terminating resistor) should be kept to less than 6 mm.
Test Fixture	Input	All inputs must be terminated through a 50 ohm resistor to ground or through a built–in 50 ohm resistor of the sampling scope.
Test Fixture	Output termination	To minimize reflection, all outputs must be terminated through a 50 ohm resistor to ground, or through a built–in 50 ohm resistor of the sampling scope.
Test Fixture	Jig delay	Effort should be made to cut down propagation delay due to the fixture (jig) itself.
Test Fixtue	Decoupling	To avoid oscillations, great care should be taken to decouple the V_{CC1}, V_{CC2}, V_{CC3}, and V_{EE} to ground.

Chapter 2
AC Testing

ECL Products

TEST PHILOSOPHY

As Integrated Circuits become increasingly faster, the job of making and verifying AC measurements becomes increasingly more difficult. The primary concern, therefore, when testing the AC characteristics of ECL devices is the accuracy and repeatability of measurements. The two largest contributing factors in this accuracy and repeatability are: the integrity of the test fixtures and the ability of the operator to precisely duplicate the AC setup conditions from bench to bench, machine to machine or test session to test session.

The information provided in this section is intended to establish guidelines that eliminate as many variables as possible to ensure that setup conditions remain consistent regardless of when or where the measurements are made.

Digitally–controlled pulse generators, power supplies, scopes, and even switching matrices are available for bench work which provide very repeatable setup and measurement conditions and are in use in varying degrees at many test locations. Information is provided for users of both the newer digital equipment as well as the older analog adjustment–type equipment.

Consideration is also given to test fixtures which applies to both bench and ATE environments. Setup conditions given in the tables of individual data sheets apply to both environments and help to maintain consistency between measurement methods.

TEST FIXTURES

When testing ECL, or any other devices whose outputs switch large amounts of current in a very short period of time, it is important to keep several factors in mind. Even though this discussion centers around bench testing, many of the principles are also applicable to automatic testing.

One major variable in AC testing is the fixture itself. Most test engineers have their own idea of what the ideal test jig should be, and it is difficult to say which method is better than the other. The thing to keep in mind, however, is to eliminate variables. For instance, it is important to maintain a continuous 50 ohm environment to reduce waveform anomalies. This includes eliminating any unterminated stubs that are longer than 1/4 inch, since at ECL speeds a reflection can be generated with sufficient amplitude and phase characteristics to distort the wavefront and reduce measurement accuracy. Also, supplying adequate power for the nanosecond and sub–nanosecond switching of high load currents is of the utmost importance.

POWER DISTRIBUTION

Switching large amounts of current at ECL speeds requires serious consideration of power supply lines (V_{CC}, V_{EE}, V_T). Things such as their physical size, shape, etc., need to be designed to reduce inductance and provide the reservoir of current required to prevent the sagging of potentials which causes the system to operate at less than optimum performance.

The easiest solution to the problem is to simply over–design so that every supply line is large enough to handle the maximum amount of current that will flow anywhere in the system. This scheme will fulfill the needed requirements but will consume a large amount of space. Since cost is also a consideration and, on the IC level, cost is directly proportional to space, the optimum design would require the supply lines to be as small as possible while still maintaining the absolute minimum required flow of current.

On the test fixture level, space is less of a concern, except at the Device Under Test (DUT) socket itself where traces run very close together.

Universality is another concern since the lack of it is the major contributor to the cost of fixtures for the various pinouts of the devices within a family. This means that some compromises must be made but, if done correctly, they will not adversely affect the performance of the DUT.

In the standard 100K family, the 100123 represents a worst–case scenario because of its six outputs, each capable of driving a 25 ohm load. It also has a different pinout from the other devices in the family.

The designers of this part provided a ground (V_{CC2}) reference pin for each output in order to prevent supply drooping that results from inductive reactance in the supply leads when attempting to source massive amounts of current through six 25 ohm loads in less than 2 nanoseconds. This case presents some interesting challenges as far as designing the test fixture. The best (but most expensive) solution is to design a dedicated fixture where each V_{CC2} pin is connected to the V_{CC} plane of the fixture (see Figure 1). To do so precludes the possibility of using the fixture for any other device in the family.

Another, less desirable, solution is to use a universal fixture in which only the standard V_{CC1} and V_{CC2} pins are connected to the V_{CC} plane and to daisy–chain all the additional V_{CC2} pins together via the input–output traces (see Figure 2). The problem with this scheme is that there is insufficient volume in the PC traces to be able to supply all of the required current. Thus the supply line droops and anomalies are created on the output waveform invalidating the measurements. This is further complicated under multiple–output–switching conditions.

A reasonable compromise would be to design a universal fixture where the V_{CC} plane of the board is located on the bottom, next to the DUT socket pins such that small solder bridges can be made from the V_{CC} plane to the appropriate pins. The V_{CC} plane is large enough (and therefore the inductance and resistance low enough) to handle the current distribution to the various V_{CC2} pins; yet the solder bridges can be removed when using the fixture for other devices in the family.

If test conditions require changing back and forth very often, other compromises will need to be made but the general idea is to draw the most equitable line between fixture cost and measurement integrity.

AC Testing

JIG DELAY VS. UNIVERSALITY

Another variable is jig delay or the delay that is added by the test fixture itself. A jig that cancels the effects of its own internal delay is quite simple to design and build.

Figure 3 shows an example of such a test fixture. The PC board consists of four layers and incorporates composite micro–strip techniques to achieve a consistent 50 ohm environment. Jig delay cancellation is accomplished by returning the input signal reference to the sampling scope directly from the DUT input pin. Since the length of the PCB trace from the DUT input pin to the reference output connector is the same length as the trace from the DUT output pin to the measured output connector (see Figure 4), and the length of each coaxial cable from the jig to the sampling scope inputs are also equal, the jig delay is virtually transparent.

However, there is an unterminated stub connected to the DUT output pin which is two or more inches long. This will cause aberrations on the output waveform which may or may not be visible on the scope display, depending on their amplitude and phase relationship to the actual output signal. These aberrations may appear as a slight overshoot or undershoot or a subtle roll–off of the rising or falling edge. The signal may be grossly distorted or no distortion may be apparent at all, except that measured propagation delay may vary from its true value by a few hundred picoseconds.

This stub could be removed by cutting the trace, but this would prevent the jig from being used for any other device in the family whose input pin is in that particular location. Therefore, a compromise will need to be made. In Figure 5, the input traces have been designed so that a jumper may be installed or removed as needed for a given part. With the jumper removed (as in the case of an output pin), the unterminated stub is less than 1/4 inches long. Even at 100K ECL speeds this length does not create enough delay in the reflected signal to significantly distort the waveform, i.e., the roundtrip delay in the stub is considerably shorter than the transition time of the output signal.

With the jumper installed (as in the case of an input pin), the line is now terminated via the scope input, and although the jumper causes a short length (less than 1/4 inches) of discontinuity in the 50 ohm microstrip, it will not significantly impact the measurement accuracy.

BYPASSING AND DECOUPLING

One matter that often seems to be ignored is power supply bypassing and decoupling. However, it is extremely important and should be given the same attention as any other factor in the test fixture.

Because the supply lines (V_{EE} and V_T) cannot always be made as a PC board plane (due to limited space at the DUT socket), they create a parasitic inductance to the high speed AC signals, and bypassing and local energy storage are required to prevent measurement anomalies. The smaller value capacitors, 0.001μF to 0.1μF provide an adequate path for the extremely high frequency signals to bypass the power supplies and associated leads. The larger value capacitors, 1.0 to 47μF, provide a local storage buffer for the instantaneous current required to switch the heavy loads. Both types of capacitors must be located as close to the DUT as physically possible in order to be effective since even very short lead lengths become significant inductors at high switching speeds.

The type of capacitor material is also critical to the effectiveness of the bypassing and energy storage. Capacitors that are specifically designed for high frequency duty into the gigahertz range are essential and should be carefully screened for their integrity prior to board installation.

PULSE SOURCE ADJUSTMENTS

The repeatability of the input signals to the DUT are a primary source of inaccuracy in ECL AC measurements and also the most difficult to control, especially when using manually adjusted equipment because of the inability of the operator to accurately repeat exactly the same setup at each test session. The procedure outlined below is suggested in order to eliminate as many of the human and mechanical variables as possible.

THE HUMAN FACTOR

The information contained under this heading is provided for those with less sophisticated equipment.

In many of today's test labs, some of the older digital sampling scopes can still be found. These include built–in digital readout capability that can display the precise value of a signal's amplitude, transition times, and propagation delay, but do not have a provision for digitizing its DC offset from ground. Because of the CRT display size, the graticule resolution, and parallel error, the human eye is incapable of consistently resolving the offset measurement to any better than 20 to 30mV. But a difference of even 2 or 3 mV in the signal offset will alter the propagation delay measurement of an ECL device by several tens of picoseconds.

The repeatability of this offset measurement can be increased significantly with the use of a few other pieces of standard laboratory equipment, including a high–quality DVM with resolution down to at least 1mV.

DC OFFSET MEASUREMENT

To accurately measure the input signal's DC offset using a DVM, a few assumptions have to be made. First, it is assumed that a square wave of amplitude A and exactly 50% duty cycle will generate a display of A/2 on a DVM that is set to measure DC volts, provided that there is no DC offset on the signal. Second, it is assumed that any DC offset added to signal will merely add to the A/2 value. And third, it is assumed that the bandwidth of the DVM is wide enough to prevent significant roll–off of the square wave signal which could introduce non–linearities into the measurement, although such non–linearities will probably be present on both the positive and negative transitions of the signal in equal amounts and therefore will tend to balance in the meter reading. Such non–linearities will decrease the accuracy of the measurement but not the repeatability of it as long as the same DVM is used each time.

Keeping these assumptions in mind, the DC offset adjustment is made as follows:

1. Set the pulse generator output signal to a repetition rate of approximately 1MHz and exactly 50% duty cycle (a frequency counter should be used for this).

2. Using a sampling scope with a digital readout set to measure volts, adjust the signal amplitude of the pulse generator to 800mV (for 10K ECL).

3. Adjust t_R and t_F to 2ns, 20% to 80% (for 10K ECL).

4. Recheck steps 2 and 3 until satisfied with the adjustment accuracy (the amplitude and transition time adjustments may interact with each other).

5. Disconnect the 50 ohm coax cable from the input of the sampling scope and connect it to the input of a DVM whose input is terminated in 50 ohms. A BNC–Banana adaptor can be used for this with either a 50 ohm precision resistor attached or 50 ohm BNC feedthrough termination in line with the coax. The termination should be as close to the DVM input connector as possible. With the DC offset of the pulse generator set at 0V, i.e., the negative swing of the signal is at 0V and the positive swing is at 500mV, the DVM should read 800mV divided by 2, or 400mV.

6. The standard DC offset for a 10K ECL input signal is 310mV. (See Figure 6.) Therefore, the

AC Testing

DC offset control of the pulse generator should be adjusted so that the DVM reads 710mV, which is one half of the signal amplitude (400mV) plus 310mV of offset.

The input signal is now set and may be connected to the test fixture but it should be checked periodically during a test session to make sure it has not drifted. Variation of this method will need to be developed to suit individual test requirements, but if the basic principle is followed, one of the major variables in ECL AC testing will be brought under control.

AC MEASUREMENTS OVER TEMPERATURE AND POWER SUPPLY RANGES

In 10K ECL devices, V_{BB} drifts with temperature. The amount of drift varies between part types due to internal power dissipation and various other characteristics but it is approximately equal to 1.1mV/°C. This affects the amount of DC offset to be used when measuring AC parameters at other than room temperature. For example: At room temperature (25°C), a part would normally require a 310mV offset. If the part were to be tested at 85°C, the offset would have to be increased by 1.1mV/°C times 60°C (ΔT) or 66mV. A total offset of 376mV would be required. Using the formula from step 6 above, one–half the signal amplitude (400mV) plus 376mV of offset would produce a reading on the ΔVM of 776mV. When testing at –30°C, the offset must be decreased from the room temperature figure by applying the same formula.

100K ECL devices are designed with internal compensation which virtually eliminates any drift due to operating temperature. Therefore, the same offset value may be used over the entire temperature range. The input signal conditions for 100K devices differ slightly from those used for 10K, but the same principles apply to either family and the same procedures and precautions should be used (refer to Table 1 for input pulse parameters).

ECL devices also drift with power supply (V_{EE}) variations. These variations are given as $\Delta V_{OH}/\Delta V_{EE}$, $\Delta V_{OL}/\Delta V_{EE}$, and $\Delta V_{BB}/\Delta V_{EE}$ in chapter 5, section 4 of this handbook and should also be taken into account in determining input signal levels for AC measurements.

3–STATE CONSIDERATIONS

Many new ECL devices have been added into the handbook that have 3–state outputs which present a whole new set of parameters to consider when making AC measurements. Basically, everything remains the same as far as test philosophy and fixture is concerned but there are some subtle differences that need to be pointed out.

The main purpose of having 3–state capability is for use in bus applications where it is desirable to totally remove all drivers except the one that is actively driving the bus. This is done in order to maintain the precise bus impedance that was designed into the system to prevent signal anomalies resulting from bus impedance mismatches. The more active drivers attached to the bus, the greater the mismatch and the worse the signal distortion.

It is important for the bus designer to know how much time it takes for a given driver to actually become removed from the bus after having been disabled. It is also important to know how long after a driver has been enablod that it can actively begin transmitting data. Parameters such as t_{PHZ}, t_{PLZ}, and t_{PZH}, t_{PZL} specify this information.

Testing for these parameters proves to be a little more difficult than testing for ordinary propagation delays. Certain kinds of ATE, however, may create new and interesting challenges for the test engineer. Because ECL devices are terminated through a load resistor to the –2.0V supply, the 3–state condition is difficult to detect, especially with ATE. The difference between a normal ECL logic Low level and the 3–state level (virtually V_T) is as little as 150mV. In an ATE environment, with its inherent noise, ground bounce, AC measurement system resolution limitations, etc., it is very difficult to accurately and repeatedly distinguish between the two levels.

25 OHM LOADS

Providing a clean 25 ohm environment for line drivers is relatively simple, especially on a bench. Using a test jig such as the one described earlier in this section, creating a 25 ohm environment is accomplished by inserting the jumper into the input line of the jig on each output pin of the DUT, then terminating both of the lines connected to that pin in 50 ohms (see Figure 7). One of the terminations for the output under test is the one built into the scope input which is connected to the output line of the test jig. The other can be a standard termination plug installed in the input line of the jig. This is a standard configuration for a 25 ohm bus which is nothing more than a 50 ohm transmission line that is terminated at each end in 50 ohms. The unused DUT outputs are terminated in the same manner by a standard termination plug.

A serious limitation on some ATEs is the inability to provide a convenient method of applying a 25 ohm load to the DUT that can be switched in and out at will. This is especially important with transceivers since, in one direction, the loads must be connected to the output side and not connected to the input side; then; during measurements in the opposite direction, the loads must be exchanged. There are several ways of getting around this limitation and individual solutions will be the option of the test engineer, but it must be remembered that impedance matching is of prime importance in order to maintain signal integrity. Unterminated stubs and unmatched lines that are longer than 1/4 inch must be avoided.

TTL OUTPUTS

TTL outputs create various problems in the ECL world. TTL typically operates outside of a characteristic impedance environment. At high AC speeds, this creates noise due to signal reflections. Progress has been made in the newer TTL technologies (FAST, ALS, etc.,) by specifying loads with a characteristic impedance of about 500 ohms.

Older TTL technologies (Schottky, Low power Schottky, and Gold Doped), each with their own AC loading techniques, do not lend themselves easily to testing in anything that resembles a characteristic impedance environment. Attempting to make repeatable, high speed AC measurements outside of such an environment is not useful.

One of the ECL–to–TTL translators that set the pace for making repeatable AC measurements by its hybrid loading scheme was the 10125. As it turns out, this has proven to be the most reliable and easiest–to–implement method developed to date. (Refer to Figure 8.)

It is hybrid in the way that it uses the old TTL loading scheme of simulating a standard TTL input structure (D_1–D_4, R_1, and C_L), but then adds a 500 ohm voltage dividing circuit to match the 50 ohm input termination impedance of the measurement scope. This method also attenuates the output signal by a factor of 10:1 but this does not significantly degrade the accuracy of the measurements. The major drawback to this load is the use of the diodes. Before TTL AC speeds reached much higher than 25 MHz., this method proved very reliable. With TTL AC speeds now reaching well over 100 MHz, most of the measurement accuracy is heavily dependent upon the recovery time of the diodes.

With the advent of Advanced Schottky technology, the diodes were eliminated, leaving only

AC Testing

the 500 ohm voltage divider and the shunt capacitor, C_L. (See Figure 9.) The 10125, 100125, and 100255 AC Characteristics are specified using the former loading method, while the newest additions to the ECL family (e.g, 100982 and 100984) use the latter method. 3–state AC measurements are more easily implemented using the latter method.

TTL AND ATE

The above discussion on TTL loading schemes pertains only to bench testing. ATE testing, on the other hand, is somewhat more challenging, simply because of the combination of the two technologies. Separately, each one's unique set of test problems can be overcome in their own ways. But combine the two technologies onto one type of automatic test system and the solution to the individual problems are sometimes in direct opposition to one another. The selection of the "right" ATE system, then, becomes a primary concern. The number of ATE vendors and the specific tester models available that are capable of doing the job are very few.

The first concern is to ensure that the test system can provide a clean, continuous 50 ohm environment from pulse source to DUT pin to measurement system. The next concern is to ensure that power supplies and measurement systems can provide the required amount of current, with DC Kelvin connections all the way to the DUT pins without compromising AC integrity. The next concern is whether the signal drivers, power supplies and measurement systems are all capable of both TTL and ECL voltage levels at the same time (–5.5 to +5.5V, at least). The pulse sources must be capable of driving at least a 3.0V (for the TTL side) and a –2.0V (for the ECL side) AC signal into a 50 ohm terminated line. There must be sufficient auxiliary power supplies to cover such things as the termination voltage (V_T), the 3–state termination voltage (as high as 5.0V), and any external relays that may be necessary for loading or isolation. There must also be auxiliary signals available under software command in order to control any such relays. The method used to load the TTL outputs is also critical. Loading schemes such as described for bench work may not be practical in the ATE environment and loading schemes provided internally on ATE vary in design, applicability, reliability, and integrity.

LEVEL SHIFTING

ECL devices are normally terminated through a 50 ohm resistor to –2.0V (V_T). When measurements are taken on a bench using sampling scopes with internal termination resistors that are referenced to ground, it is necessary to shift all of the supply voltages and pulse generator signals up by +2.0V. This is not a desirable solution but since it cannot be avoided, there are a few points that should be kept in mind.

The primary disadvantage is that the ground reference to the DUT V_{CC} pins is lost when +2.0V power supply is substituted. This now requires bypassing as discussed earlier. The best bypassing scheme, located in the closest proximity to the DUT is still not as good as a large ground plane, so power supply drooping and output anomalies will result. The degree of drooping can only be decreased but not eliminated.

Additionally, all signal and power supply voltages must be readjusted to the appropriate levels. Since bench testing is still considered to be "the standard", this information has been provided in the AC diagrams and tables in each data sheet. If ATE testing is desired, however, the 2.0V shift is not necessary.

Further complications arise when testing Translating Transceivers (ECL–TTL, TTL–ECL) such as the 100982 or the 100255. When making AC measurements in the TTL to ECL direction, level shifting is required. When measuring in the ECL to TTL direction, no level shifting is needed since the TTL output loads are normally reference to system ground.

AC Testing

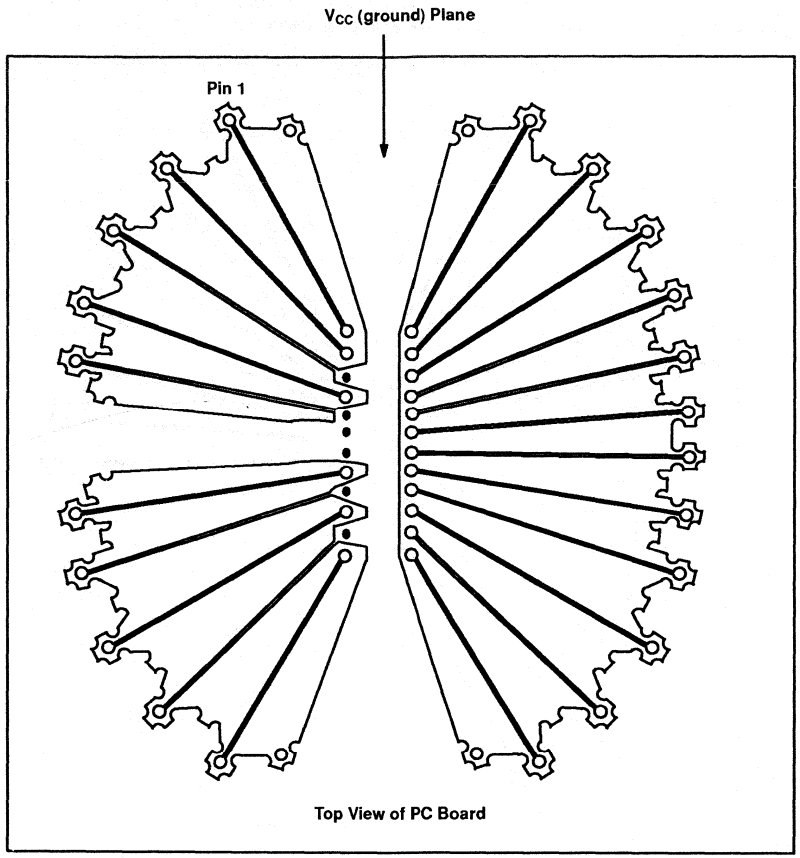


Figure 1. Fixture for 100123 with V_{CC2} pins permanently connected to V_{CC} plane provides excellent grounding but dedicated to one part type.

AC Testing

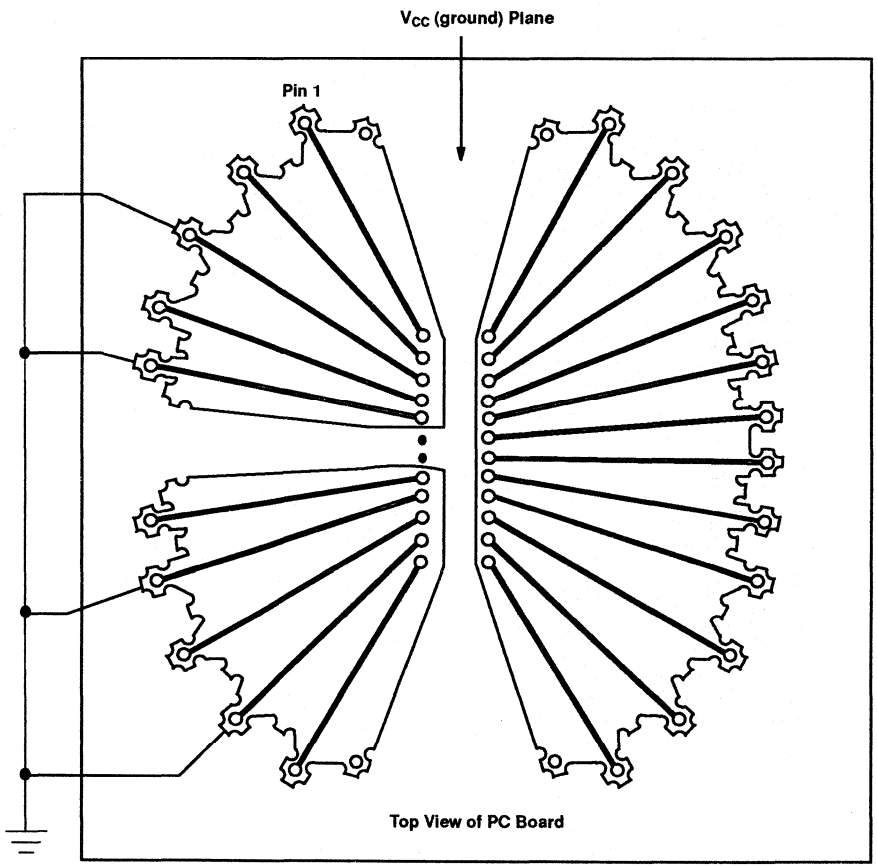


Figure 2. Fixture for 100123 with V_{CC2} pins connected to ground via I/O traces provides very poor grounding method, although very simple to change for another product pinout.

AC Testing

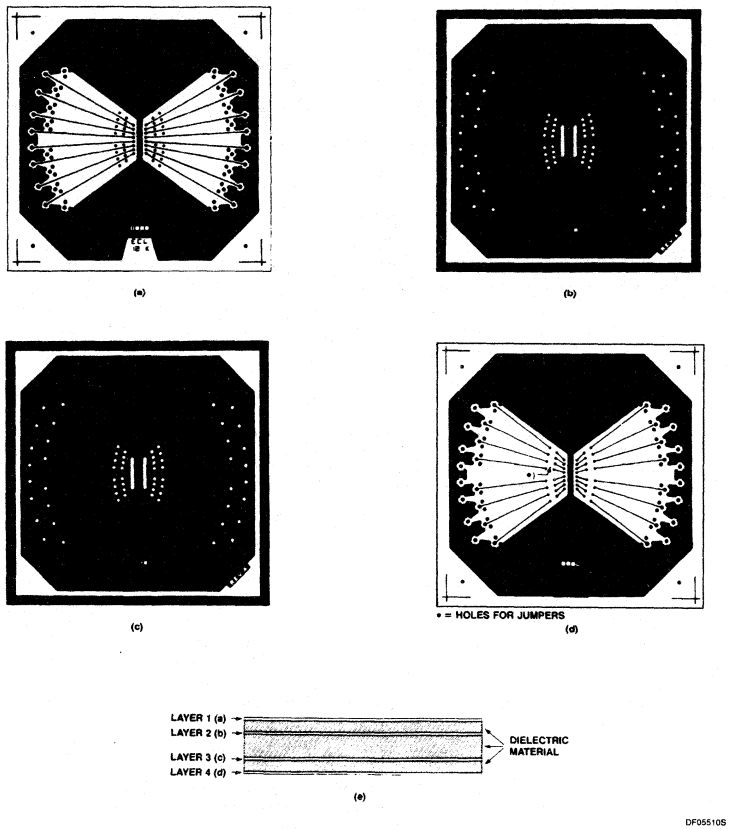


Figure 3. Sample AC test fixture fabricated as a 4–layer PC board to produce a 50 ohm environment.
Top traces of layer 1 (a) produce a 50 ohm micro–stripline with layer 2 (b), the ground plane, and are used as output lines from the DUT.
Layer 3 (c) is the ground plane for the bottom traces of layer 4 (d) which are used as inputs to the DUT. (Notice the holes for the jumpers.) In the cross–sectional view (e), the space between layers 2 and 3 is non–functional except to provide rigidity to the overall fixture.

AC Testing

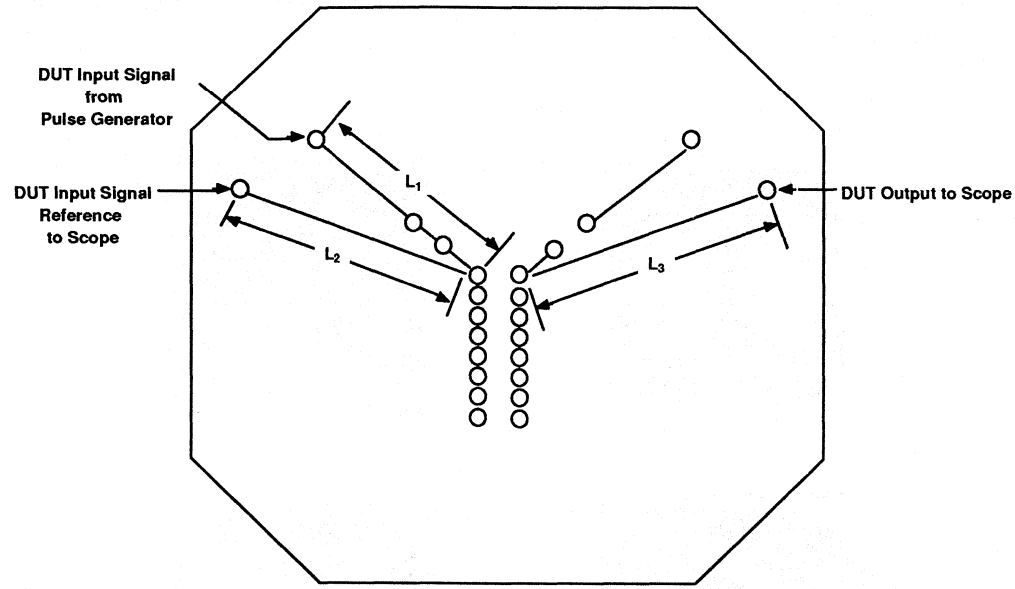


Figure 4. The reference for the input signal is taken at the DUT pin after length L_1. Since the length of the two output traces (L_1 and L_2) are equal, fixture delay cancels out leaving only the delay through the DUT package and circuitry.

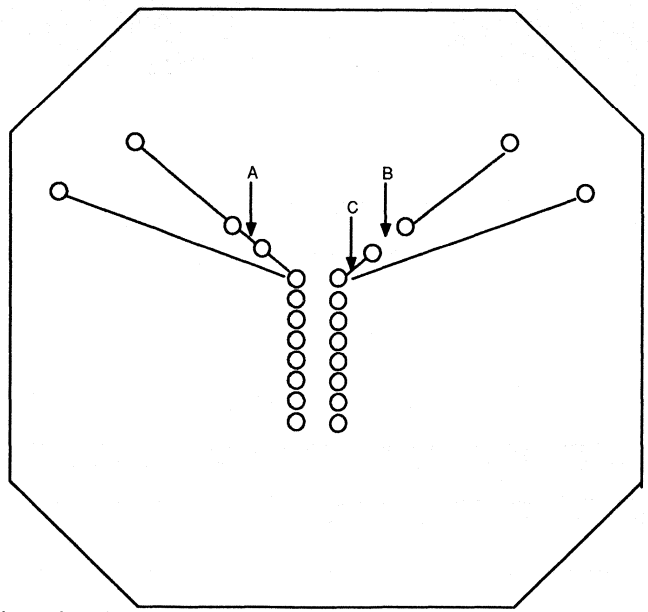


Figure 5. Trace used as an input has jumper (A) installed but trace used as an output has no jumper (B), leaving a stub(C) of less than 1/4" long.

AC Testing

Table 1. Input Parameters for Manual AC Measurement of ECL Devices at Room Temperature (25°C)

PARAMETER	FAMILY	
	10K	100K
Amplitude	800mV	740mV
Offset	310mV	310mV
t_R, t_F	2ns	700ps
Repetition Rate	1MHz	1MHz
Duty cycle	50%	50%

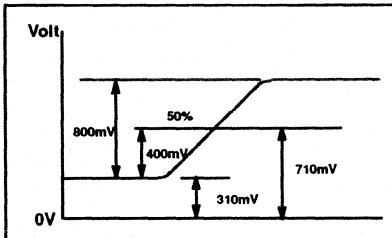


Figure 6 800mV/2 + 310mV = 710mV

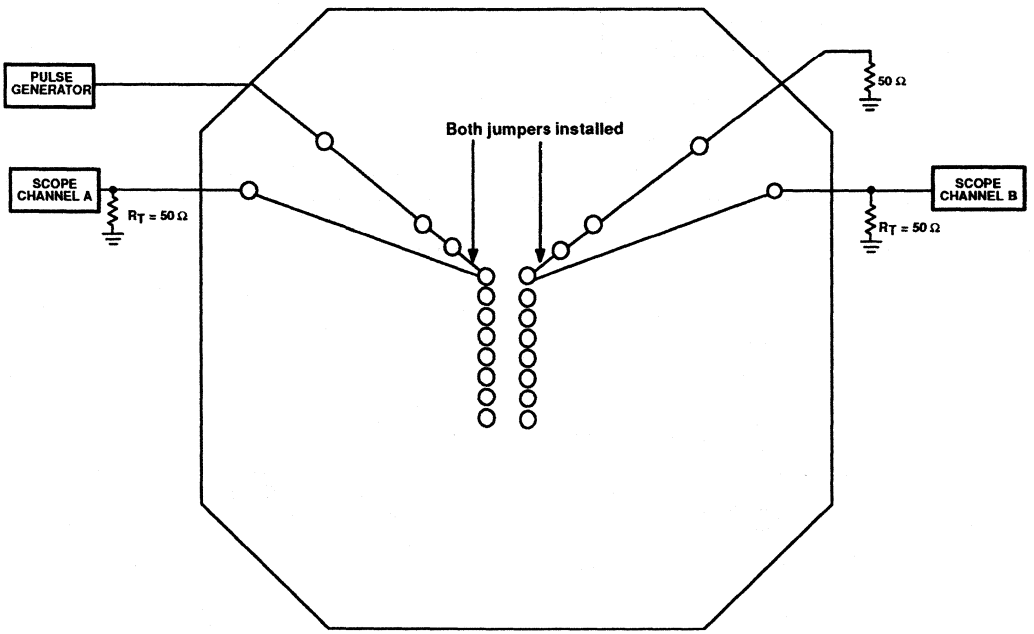


Figure 7. A 25 ohm load is established by terminating both 50 ohm traces connected to the output of the DUT. R_T is the 50 ohm termination built into the scope.

AC Testing

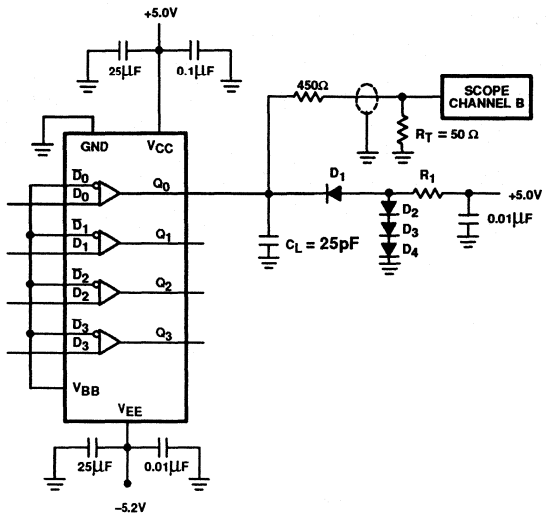


Figure 8. 10125 TTL output loading scheme provides interface to a 50 ohm environment.

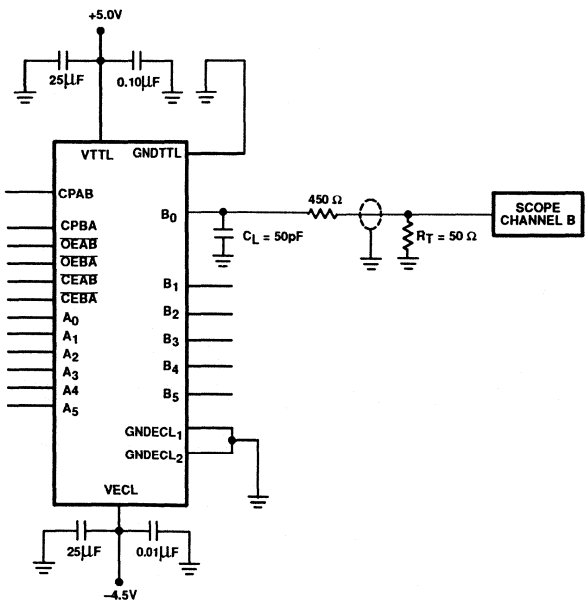


Figure 9. 100982 TTL output loading scheme eliminates the diodes that decrease testing accuracy.

Section 4
ECL User's Guide

INDEX

Chapter 1	ECL Circuit Basics	37
Chapter 2	Logic Function Operation	41
Chapter 3	ECL Gate—Static Characteristics	43
Chapter 4	ECL Gate—Dynamic Characteristics	45
Chapter 5	100K ECL	46
Chapter 6	Transmission Lines	48
Chapter 7	Interconnection	53
Chapter 8	Power Supplies	57
Chapter 9	Packages and Thermal Constraints	59
Chapter 10	Interfacing ECL Families	61
Chapter 11	Circuit Boards	64

Chapter 1
ECL Circuit Basics

ECL Products

THE ECL GATE

Figure 1.1 shows a basic ECL 10K OR/NOR gate having two inputs and two complementary outputs. The gate's current switching stage is shown in Figure 1.2. The input voltage, V_{IN}, controls the current, I. When V_{IN} changes logic levels, I is switched between Q_2 and Q_5. V_{BB}, the reference voltage, is held at a fixed voltage by an internal voltage driver, with the fixed voltage being midway between the input voltage threshold region. As the current is switched, the output voltages V_{OUT1} and V_{OUT2} also change, giving a NOR and an OR logical output, respectively.

The net output voltage swing is determined by R_3 and R_6 and the magnitude of 1.1 can be determined from:

$$I = \frac{Max(V_{IN}, V_{BB}) - V_{BE} - V_{EE}}{R_7} \qquad \text{Eq. 1.1}$$

where V_{BE} is the base–emitter voltage drop of Q_2 or Q_5 (on the order of 0.8V).

If $Max(V_{IN}) > Max(V_{BB})$, then

$$I = \frac{Max(V_{IN}) - V_{BE} - V_{EE}}{R_7} \qquad \text{Eq. 1.2}$$

If $Max(V_{IN}) < Max(V_{BB})$, then

$$I = \frac{Max(V_{BB}) - V_{BE} - V_{EE}}{R_7} \qquad \text{Eq. 1.3}$$

I is on the order of several milliamperes (4mA for a 10K gate).

Figure 1.3 gives the switching characteristics of the circuit in Figure 1.2, with the output voltage given as a function of the input voltage. Four operating zones are shown labeled A, B, C, and D.

In Zone A, V_{IN} is below V_{BB} enough to turn Q_2 off. V_{OUT1} is

$$V_{CC} - (I \text{ leakage } Q_2)(R_3)$$

The current I, passes almost entirely through R_6 creating a voltage drop across R_6 of about 1V (the value of R_6 is selected specifically to achieve this). V_{BB} is designed to be slightly lower than $V_{CC} - (1)\ (R_6)$ to avoid saturation of Q_5 while maintaining a collector-base voltage > 0. For this purpose, V_{CC}–V_{BB} is selected to be on the order of 1.3V.

In Zone B, the transition region, the V_{IN} is nearly V_{BB}. Both transistors, Q_2 and Q_5 are on and conducting current. In this region the switching stage behaves like a differential amplifier. Q_2 and Q_5 are designed to be as nearly identical as possible so that when $V_{IN} = V_{BB}$, the current I, is divided equally between the two, making the voltage drop across both R_3 and R_6 approximately 0.5V. The width of this zone is approximately 100mV at 25°C. The width varies with temperature by (4kT)/q (where k is the Boltzman constant, q is the charge of an electron, and T is the absolute temperature of the V_{BE} junction due to the temperature dependence of the emitter–base junctions of Q_2 and Q_5.

In Zone C, V_{IN} is enough above V_{BB} to turn off Q_5. As V_{IN} rises, the emitter voltage V_E, increases (since $V_E - V_{IN} - V_{BE}$ (Q_2) and $V_{BE}(Q_2)$ is approximately constant) while V_{BB} remains constant until the base–emitter voltage drop of Q_5 is sufficient to keep Q_5 on. In this zone V_{OUT2} becomes equal to $V_{CC} - (I \text{ leakage } Q_5)\ (R_6)$ and $V_{OUT1} = V_{CC} - (R_3)\ (I)$. R_3 is designed to make V_{OUT1} close to V_{CC}–1V. I varies in Zone C due to its dependence on V_E. Because of this, R_7 is replaced by a current source in many circuits to produce better matched output characteristics, as well as other advantages that will be discussed in a later section.

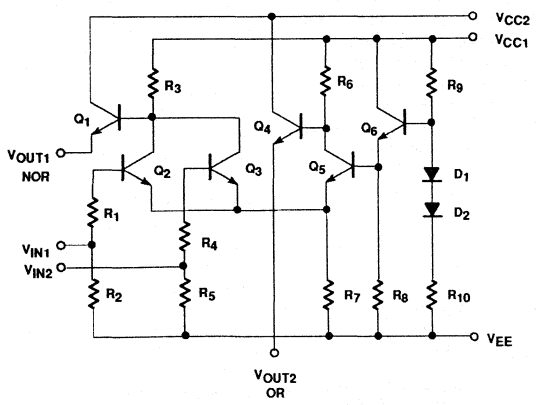
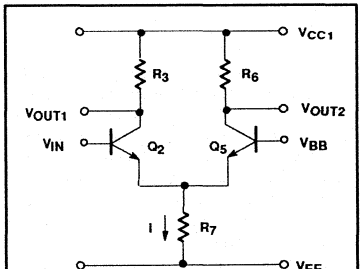


Figure 1.1 Basic 10K ECL OR/NOR Gate



If $Max(V_{IN}) > Max(V_{BB})$, then

$$I = \frac{Max(V_{IN}) - V_{BE} - V_{EE}}{R_7}$$

If $Max(V_{IN}) < Max(V_{BB})$, then

$$I = \frac{Max(V_{BB}) - V_{BE} - V_{EE}}{R_7}$$

Figure 1.2 ECL Current Switch

User's Guide

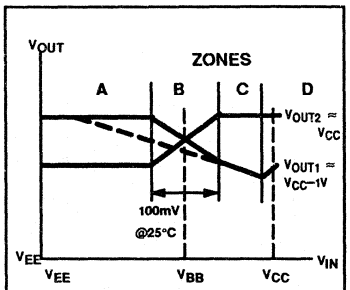


Figure 1.3 Switching Characteristics of ECL Current Switch

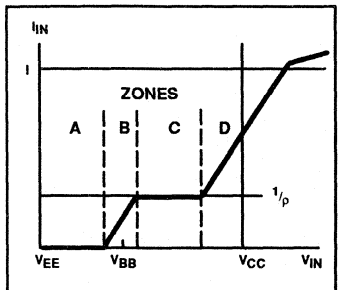


Figure 1.4 Change in Base Current as a Function of V_{IN}

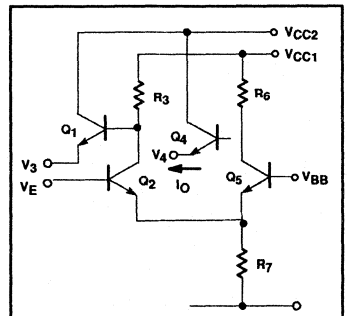


Figure 1.5 Emitter Follower Outputs

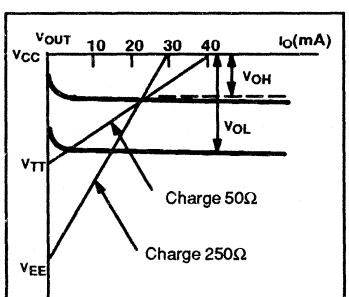


Figure 1.6 V_O as a Function of I_O

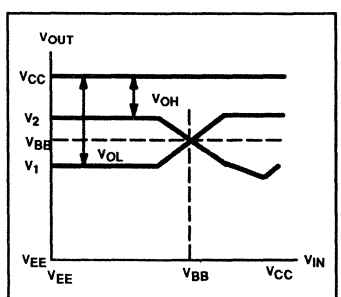


Figure 1.7 V_{OUT} as a Function of V_E (50Ω Load)

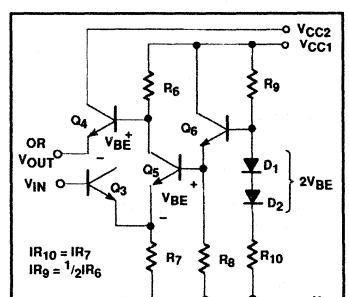


Figure 1.8 Internal Voltage Generator – 10K

In Zone D, V_E is high enough to allow Q_2 to saturate. Under this circumstance, the base–collector junction of Q_2 is forward–biased and the collector voltage begins to follow the input voltage, creating the upturn in the characteristic curve for V_1 in Figure 1.3. Because the current I can no longer be provided completely by the collector of the transistor, the difference is supplied by the base current of Q_2, which increases considerably. The change in base current with increased input voltage is shown in Figure 1.4. This current is the input current of the simplified gate. The input voltage of an ECL gate is usually limited to prevent operation in Zone D.

EMITTER-FOLLOWER BUFFERS —OUTPUT AND TRANSFER CHARACTERISTICS

The V_1 and V_2 signals of Figure 1.2 could be used directly as the output signals of the gate. However, there are two disadvantages in doing so. First, the voltage values of the logic levels generated by these nodes are not compatible with an input threshold voltage equal to V_{BB}, so a downward shift of V_1 and V_2 is required. Second, V_1 and V_2 would have a high impedance for values of I in the several milliampere range. The addition of transistors Q_1 and Q_4, shown in Figure 1.5, eliminates both of these problems. The output voltage level is shifted down by V_{BE}(on). And, because these transistors are configured as emitter–followers, they provide a low output impedance allowing the circuit to drive transmission lines with characteristic impedances of 50 ohms or greater.

Figure 1.6 shows the output characteristic, V_O ($=V_3$ or V_4), as a function of the output current, I_O, for Zone A or Zone C. Two load lines are shown: 50Ω and 250Ω. The 50Ω load is connected to an intermediate voltage, V_{TT}, to limit the output current of the gate. Larger loads can be connected directly to V_{EE}.

Figure 1.7 gives the transfer characteristic, V_O ($=V_3$ or V_4) as a function of V_E. Note that the logic swing is now almost symmetrical about the reference voltage, V_{BB}, due to the voltage–level shifting by the V_{BE} of the emitter–follower transistors, Q_1 and Q_4.

INTERNAL THRESHOLD VOLTAGE GENERATOR

In 10K ECL circuits, the threshold voltage, V_{BB}, is provided by the internal voltage generator shown in Figure 1.8. (The NOR output circuitry has been excluded for simplicity.) As with other device technologies, the transfer and other characteristics of ECL gates are temperature–dependent. This is mainly due to the temperature dependence of V_{BE}.

As stated earlier, the logic High and logic Low noise margins of ECL gates should be symmetrical about V_{BB}. Due to the temperature dependence of V_{BE}, this is possible at only a single temperature when the reference voltage, V_{BB}, is kept fixed. However, it is possible to maintain the symmetry of the noise margins over a wide temperature range if the reference voltage itself is made to be temperature-dependent. The voltage generator of Figure 1.8 accomplishes this. The reference voltage for the current switch is taken from an emitter–follower, Q_6. D_1 and D_2 help to stabilize the current in the emitters of Q_3 and Q_5 against variations in temperature in that any change with temperature of the

User's Guide

V_{BE} of Q_6 and Q_5 is compensated by a similar change across D_1 and D_2.

Assume a temperature change, ΔT. This temperature change will produce a voltage change in each forward-biased V_{BE} junction, the amount of voltage change being $\Delta V_{BE} = -kT$, where k = 2mV/°C. Assuming the gain through Q_6 is unity, the change in the reference voltage, V_{BB}, due to ΔT is given by

$$\Delta V_{BB} = \frac{2\Delta V_{BE} R_9}{R_9 + R_{10}} - \Delta V_{BE} = \Delta V_{BE}\left[\frac{2}{\left(1 + \frac{R_{10}}{R_9}\right)} - 1\right] \quad \text{Eq. 1.4}$$

When Q_5 conducts, V_{OUT} is at logic level 0. The change in V_{OUT} due to ΔT is given by

$$\Delta V_{OUT}(\theta) = -\Delta V_{BB}\left(\frac{R_6}{R_7}\right) + \Delta V_{BE}\left(\frac{R_6}{R_7}\right) - \Delta V_{BE} = \left(\frac{R_6}{R_7}\right)(-\Delta V_{BB} + \Delta V_{BE}) - \Delta V_{BE} \quad \text{Eq. 1.5}$$

Note that in the equations for ΔV_{BB} and ΔV_{OUT} only resistor ratios appear. This result is important because it is possible to hold resistor ratios to much tighter tolerance than absolute values of resistors during device fabrication.

When Q_5 is off and V_{OUT} is at logic 1,

$$V_{OUT}(1) = -\Delta V_{BE} \quad \text{Eq. 1.6}$$

Resistor values are chosen so that the "average" ΔV_{BE} of the two logic levels will equal ΔV_{BB}. Therefore, if the ΔV_{BE} of Q_4 and Q_6 are equal, then V_{BB} will remain centered between V_{OH} and V_{OL}.

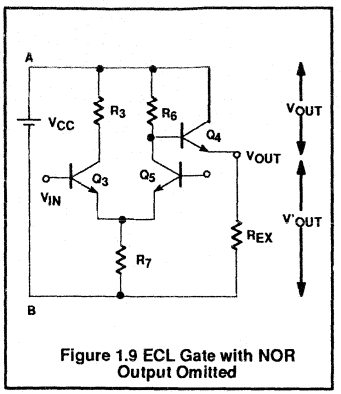


Figure 1.9 ECL Gate with NOR Output Omitted

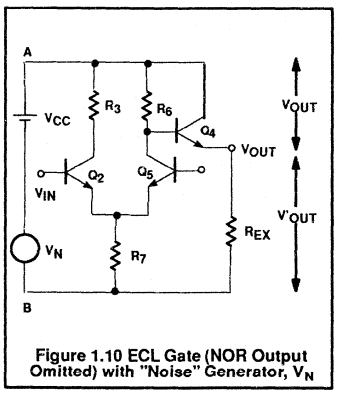


Figure 1.10 ECL Gate (NOR Output Omitted) with "Noise" Generator, V_N

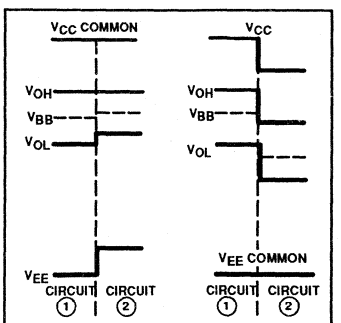


Figure 1.11 Difference in Output Voltage of ECL Gate When Powered by V_{CC} vs. Powered by V_{EE}

SELECTION OF V_{CC} AS REFERENCE VOLTAGE (GROUND)

Unlike TTL gates, with ECL gates it is common practice to ground the positive end of the voltage supply. One advantage of using this arrangement with ECL gates is that it minimizes external noise transfer.

Figure 1.9 shows our ECL gate with the NOR output omitted for simplification. Usually the output voltage of the gate is the voltage between the emitter of Q_4 and V_{CC} (V_{OUT}), but we could just as easily consider the output voltage to be that between the emitter of Q_4 and V_{EE} (V'_{OUT}). As far as the output signal is concerned, the positive and negative sides of the supply are the same electrical point. As Figure 1.9 shows, closed-circuit loops are formed by the connection to V_{CC}. A varying magnetic flux can be produced in these loops by the currents in the gate, or by currents in neighboring gates, which produces an electromagnetic field in the loops and in V_{CC}. This electromagnetic field, or induced voltage, is referred to as "noise" because it is random and unpredictable. It is represented in Figure 1.10 by the voltage source V_N.

With the inclusion of V_N, the two sides of the power supply, A and B, are no longer equivalent and V_{OUT} and V'_{OUT} are also no longer equivalent. Assume Q_5 is cut off. Then V_N can be considered across R_6, Q_4 and R_{EX} only. The impedance between the collector and emitter of Q_4 is

$$Z_{CE} = \frac{R_6}{(h_{FE} + 1)} \quad \text{Eq. 1.7}$$

For h_{FE} = 99 and R_6 = 300Ω, Z_{CE}=3Ω. Then, $V_{OUT} = (3/1{,}500)V_N = 0.002V_N$ while $V'_{OUT} = (1{,}500/1{,}503)V_N \equiv V_N$. The advantage lies clearly with using V_{OUT} rather than V'_{OUT}.

It is also common practice to have the output terminal of a signal source and the input terminal of a signal measuring device use ground as one signal terminal. This practice is convenient since ground is usually the chassis on the relay rack on which the circuit is built, including the cabinet that houses the unit, if any, and has the advantage that when units are interconnected, the chassis, cabinets, etc., are all joined electrically.

Thus, since it is advantageous to use the positive side of V_{CC} as one of the output terminals, and also advantageous to use ground as one such terminal, the positive side of V_{CC} is grounded.

User's Guide

Another advantage to the grounding arrangement employed with ECL is shown in Figure 1.11 where the output voltages of two gates, one powered by V_{CC} and one powered by V_{EE}, is shown. When V_{CC} is common to both gates, V_{OH} varies very little and the V_{OL} of each gate remains compatible with the threshold voltage, V_{BB}, of the other. However, when V_{EE} is common to both gates, the output voltages V_{OH} and V_{OL} of both gates can become so different that the threshold of the second gate is no longer compatible with the output voltage of the first gate.

ECL LOGIC IMPLEMENTATION

An ECL gate incorporating the basic structure of Figure 1.1 is shown in Figure 1.12. The input transistors Q_2 and Q_3 are shown here in parallel. Additional transistors can be added in parallel to provide for multiple gate inputs.

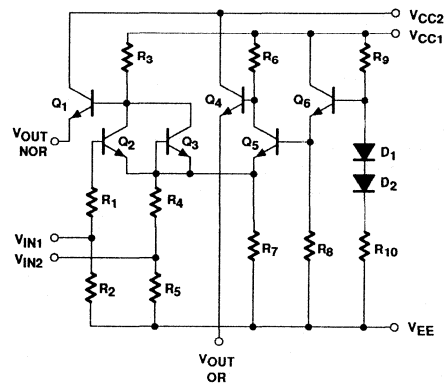
When the input voltages V_{IN1} and V_{IN2} are in the LOW state (i.e. < V_{BB}), the input transistors Q_2 and Q_3 are cut off and Q_5 is conducting. This creates a LOW level at the V_{OUT2} output and a HIGH level at the V_{OUT1} output. If either of the input voltages goes to the HIGH state (i.e. > V_{BB}), the current will switch to the corresponding input transistor and cut Q_5 off. Consequently, the V_{OUT2} output will go to HIGH and the V_{OUT1} output will go LOW. Thus, the circuit performs an OR function

$$V_{O4} = A + B \qquad \text{Eq. 1.8}$$

at the V_{OUT2} output and performs a NOR function:

$$V_{O1} = \overline{A + B} \qquad \text{Eq. 1.9}$$

at the V_{OUT1} output.



V_{IN1}	V_{IN2}	V_{OUT1}
0	0	1
0	1	0
1	0	0
1	1	0

V_{IN1}	V_{IN2}	V_{OUT2}
0	0	0
0	1	1
1	0	1
1	1	1

Figure 1.12. ECL Logic Implementation

Chapter 2
Logic Function Operation

ECL Products

SERIES GATING

The switching stage described in the previous section behaves like an inverting relay contact and, as with relays where contacts can be cascaded, ECL differential stages can also be cascaded. An example is shown in Figure 2.1. Input transistors A and B have been placed in series to share a common current source, Q_{10}, and implement an AND function. It is important to avoid saturating the lower transistors so that the complete benefits of non-saturating logic can be maintained. This can be accomplished by shifting the thresholds of the two differential stages by a voltage comparable to the logic swing on input A. Therefore, a second reference voltage, V_{B2}, is added to shift from 1V to 1.6V with respect to V_{B1}. An equal shift is implemented for input A by the emitter-follower, Q_{12}, shown in Figure 2.2.

This logic block, called "series gating," adds the NAND and AND logic functions to the OR and NOR capability of the basic ECL gate. This technique is so powerful, consumes so little power, and requires so few components that it has become the standard building block for complex circuits in ECL families having two or three levels of current–switching. (The voltage of the 10K family was set at –5.2V to allow three levels of current-switching — two voltage shifts. For a simple gate with only one level of current switching, 2.6V to 3V would certainly have been sufficient.)

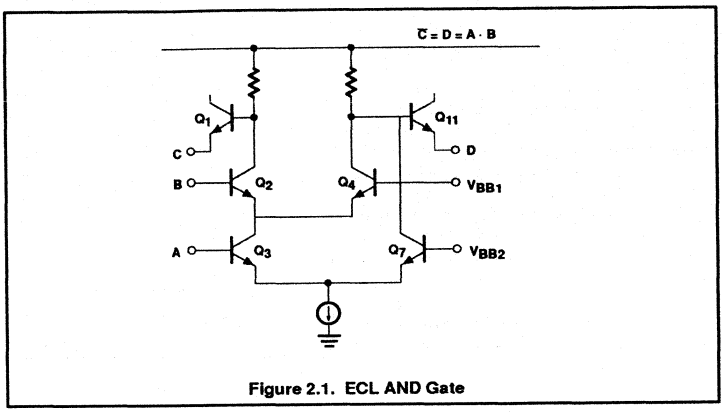


Figure 2.1. ECL AND Gate

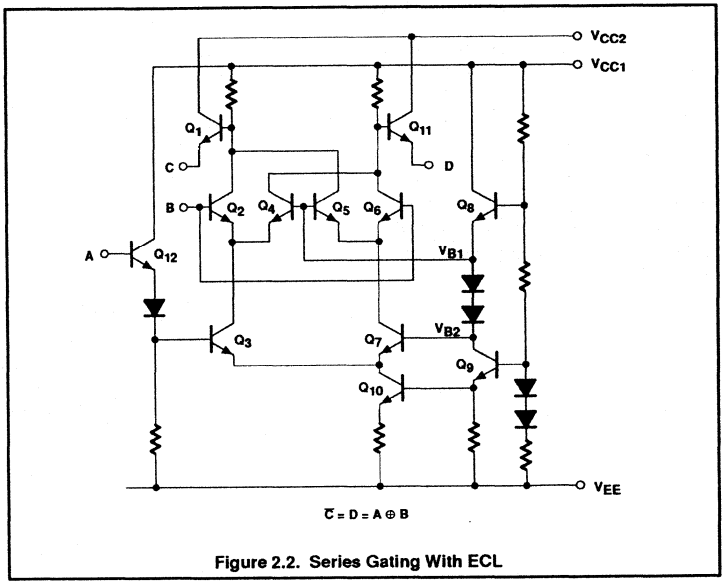


Figure 2.2. Series Gating With ECL

User's Guide

FLIP-FLOPS

Flip-flop functions make extensive use of series gating. Figure 2.3 shows a simple flip-flop that, under the control of a clock signal, latches a "data" bit. When the clock is in the LOW state, current from the source transistor, Q_9, is switched by Q_{12} to the differential "data" stage formed by Q_5 and Q_{13}, and from there to the outputs V_{OUT} and $\overline{V_{OUT}}$. During the transition, this current controls the logic state of the "internal outputs," Q_8 and Q_{10}, which reproduce the state of the data input. When the clock goes HIGH, the current is switched by Q_7 to the differential pair formed by Q_6 and Q_{11}, which is itself controlled by the internal outputs. The circuit is then latched on the data state that preceded the rise in the clock signal, regardless of the subsequent state of the data input.

In this latched state, the data in the flip-flop can be changed by applying a LOW logic state to transistor Q_4 or Q_{14}, which then forces the output HIGH or LOW, thereby accomplishing a "set-reset" function.

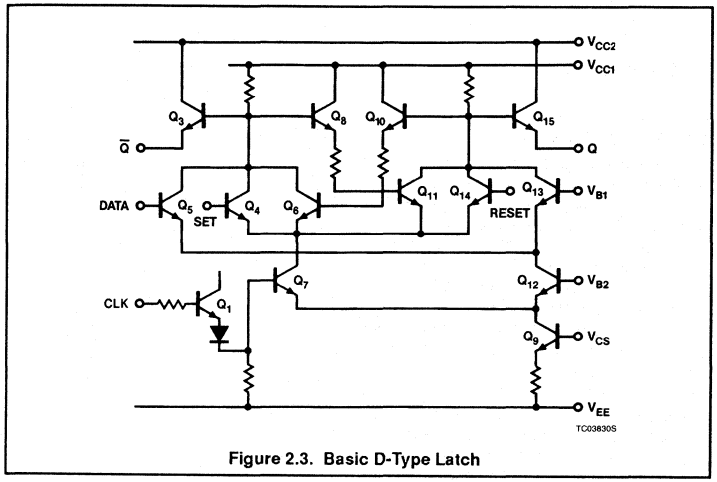


Figure 2.3. Basic D-Type Latch

WIRED-OR FUNCTIONS

Figure 2.4 shows another technique for implementing complex ECL functions: the ability to control several output emitter-followers with the same gate. This makes it very easy to generate supplementary signals.

In Figure 2.4, four independent logic functions are implemented via only two differential stages by combining outputs. Note that for the internal outputs, which need only drive internal inputs having relatively high impedance rather than 50Ω lines, fairly large internal resistors (R_T=1k to 5kΩ) can be used for V_{EE} connections.

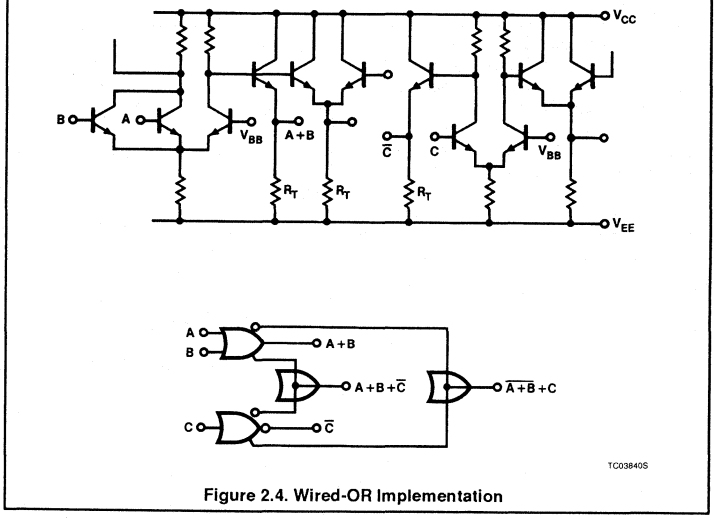


Figure 2.4. Wired-OR Implementation

Chapter 3
ECL Gate – Static Characteristics

ECL Products

OUTPUT CHARACTERISTICS

Figure 3.1 shows transfer curve and DC specification test points for a 10K ECL OR gate. Note the two sets of min/max logic level parameters. The first set, V_{ILmin}/V_{IHmax}, should cause the output to take a level somewhere within the V_{OLmax}/V_{OHmin} specification. The second set of logic level parameters relates to the switching thresholds. When a voltage V_{ILT} is applied to the input, the OR output should be below the V_{OLT} level; and, when a voltage V_{IHT} is applied to the input, the output should be above the V_{OHT} level.

Since variations in wafer fabrication process parameters can affect a gate's transfer characteristics, device performance is tested at the indicated test points to ensure that:

1. the switching threshold falls within the rectangle defined at the lower left by the V_{ILT}/V_{OLT} corner point and at the upper right by the V_{IHT}/V_{OHT} corner point; i.e. that switching does not begin outside this rectangle;
2. quiescent logic levels fall within the specified min/max ranges.

In 10K ECL, this curve varies with temperature and supply voltage changes. This is explained in detail in a later section.

NOISE MARGIN

Noise margin is a measure of a circuit's immunity to adverse DC operating conditions. Noise margin is defined for the HIGH state as

$$V_{NH} = V_{OHT} - V_{IHT} \qquad \text{Eq. 3.1}$$

and for the LOW state as

$$V_{NL} = V_{ILT} - V_{OLT} \qquad \text{Eq. 3.2}$$

Where "T" is used to denote the threshold value for V_{OH}, V_{OL}, V_{IH} and V_{IL}. Figure 3.2a gives noise margins vs. temperature variations for 10K ECL and 3.2b gives noise margins vs. power supply variations for 10K ECL.

"Noise immunity measures the minimum input noise that will propagate through cascaded gates. This measurement, indicative of a device's immunity to noise during actual AC system operation, is difficult to measure and, therefore, is not specified on datasheets. However, noise immunity of 10K devices is typically at lease 40mV greater that the DC noise margin.

Both 10K and 100K device specifications dictate that only one input at a time should be connected to a threshold level (V_{IHT} or V_{ILT}) and that all other inputs should be at V_{IHmax} or V_{ILmin} during testing.

INPUT CHARACTERISTICS

As shown in Figure 1.1, gate inputs are not connected directly to the base of their input transistors, but instead are connected through a network of two resistors, R_1 and R_2 (or R_4 and R_5). The resistor R_1 (R_4) guarantees a positive (real) input impedance at all frequencies. High frequency capacitive effects could cause the input current to be put out of phase by more than 90° with regard to the input voltage, causing the appearance of a negative resistance on the base of Q_2, if R_1 (R_4) was not included. The resistor R_2 (R_5) pulls any unused inputs LOW, eliminating the need for external wiring on these inputs. However, because of large switching transients associated with fast rise and fall times and the sensitivity of clocked devices (flip-flops, counters, etc.), it is advisable to use external components with clocked devices to assure that the unused inputs of such devices are securely tied to a low logic level.

Figure 3.3 shows the input characteristics of an ECL gate. I_{IHmax} is the guaranteed maximum static load that is represented by the gate input. I_{ILmin} guarantees the internal pull-down resistance.

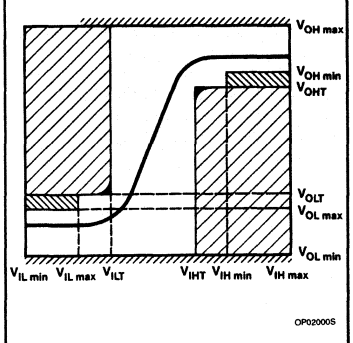


Figure 3.1. ECL OR Gate Transfer Curve with DC Specification Test Points

PARAMETER		-30°C	+25°C	+85°C
V_{IHmin} to V_{OHTmin}	V_{NH} (mV)	125	125	125
V_{ILmax} to V_{OLTmax}	V_{NL} (mV)	155	155	155

a. 10K to 10K
Minimum Noise Margin vs. Temperature Variations

PARAMETER		V_{EE} – 10%	V_{EE} – 5%	V_{EE} + 5%
V_{IHmin} to V_{OHmin}	V_{NH} (mV)	127	166	241
V_{ILmax} to V_{OLmax}	V_{NL} (mV)	223	249	301

b. 10K to 10K
Minimum Noise Margin vs. V_{EE} Variations

Figure 3.2. 10K ECL Minimum Noise Margins

User's Guide

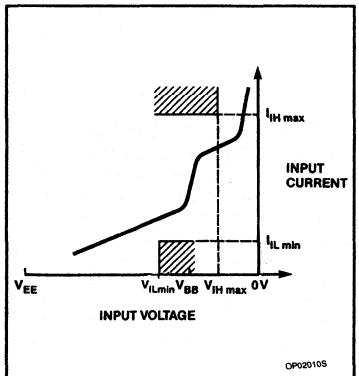


Figure 3.3. ECL Gate Input Characteristics

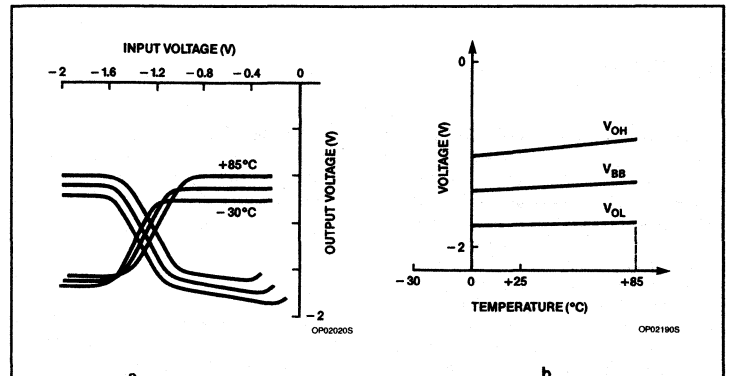


Figure 3.4. Effect of Temperature on Output Voltage

CURRENT CONSUMPTION

Current consumption is specified as the Power Supply Drain Current, I_{EE}, and is the current that is drawn through the supply pin, V_{EE}. I_{EEmax} is measured with V_{CC} at 0V and V_{EE} at −5.2V since maximum circuit speed is achieved at this power supply value.

The magnitude of I_{EE} is affected by three separate portions of the ECL gate: the current switch, the reference voltage supply, and the output emitter–followers. I_{EE} limits specified for a particular device reflect the power requirements of the current switch (or switches) and reference voltage supply. However, ECL devices can support a broad range of output termination resistor values, with the particular value chosen depending on individual system performance requirements. Therefore, it is necessary to add power requirements due to input current drain and output loading to the specified power supply drain current limit given in the device's datasheet.

EFFECT OF TEMPERATURE

10K ECL outputs rise with increasing temperature. This is mainly due to the dependence of V_{BE} on temperature.

When designing with ECL devices, the following should be kept in mind:

1. Maximum noise immunity is obtained when two connected circuits are at the same temperature;
2. When a circuit is tested, thermal equilibrium must be obtained before any measurements are made.

EFFECT OF SUPPLY VOLTAGE ON 10K ECL

As explained in Chapter 1, 10K ECL devices are specified with V_{CC} at ground and V_{EE} at −5.2V because maximum noise immunity is achieved with this supply configuration. This convention is not mandatory; and, while not recommended because of loss of noise immunity, it is possible to operate ECL devices from a TTL +5V power supply.

10K ECL devices are specified for V_{EE}=−5.2 ±10%. However, the best circuit speed is achieved with V_{EE}=−5.2V. As V_{EE} becomes more negative, both noise margin and power dissipation increases. As V_{EE} becomes more positive, power dissipation decreases, but at the expense of a decrease in noise margin.

Most 10K ECL devices have two power supply pins, V_{CC1} and V_{CC2}, to reduce cross-coupling between internal device components when the outputs are driving heavy loads. V_{CC1} supplies current to the output transistors and V_{CC2} supplies current to the circuit logic transistors.

Chapter 4
ECL Gate – Dynamic Characteristics

TRANSITION TIME AND PROPAGATION DELAY

The dynamic characteristics of a device are those that define its effect on a specified input signal as that signal travels through the device. They include the time required to change the output from one logic state to another, specified as the output transition time, and the time required for the output of the device to respond to an input signal, specified as the propagation delay.

To accurately measure a device's dynamic performance, an environment very similar to the system environment in which the device will be used should be created. Input voltages applied should represent signals the device will see in the system; i.e., pulses having HIGH and LOW levels that are typical of V_{OH} and V_{OL} and having edges that are representative of the edges generated by the outputs of an interfacing device. An example is shown in Figure 4.1.

The output transition time (t_{TLH} and t_{THL}) also gives an indication of the maximum operating frequency and of any high–frequency parasitic effects. For ECL devices, both t_{TLH} and t_{THL} are measured between 20% and 80% of the signal amplitude; i.e., in the transition region. Because ECL utilizes current–mode switching to eliminate transistor saturation storage delays and permits the use of differential comparison techniques, transition rise times can, by design, be slowed via internal time constants without sacrificing throughput delays. This is an important advantage of ECL because slower rise times minimize ringing and reflections and, therefore, simplify board design. The typical edge rate for 100K ECL is 1V/ns, 80% of the Schottky TTL edge rate.

Propagation delay (t_{PD}) defines the time it takes for a signal to travel internally from the input terminal and the output terminal of a device. Test equipment limitations make it necessary to measure the propagation time of ECL devices at 50% of the amplitude of both signals rather than at V_{BB}.

INTERNAL SWITCHING

Internal switching of the gate takes place in two stages (see Figure 1.10):

1. In the first stage, the input voltage rises to V_{IH}. The voltage change at the input of transistor Q_2 is delayed, however, because of its input capacitance. When its input voltage enters Zone B in Figure 1.3, Q_2 begins to conduct after a given time delay dependent on its cut–off frequency, f_T.
2. In the second stage Q_2 delivers current into resistor R_3. The collector voltage, followed by the output voltage, begins to change. The rate of change of the output voltage depends on the total capacitance on the collector of Q_2, and varies inversely with the load resistance of the emitter of Q_1.

The tranistion time is dependent on the second stage, whereas the propagation delay depends on both stages.

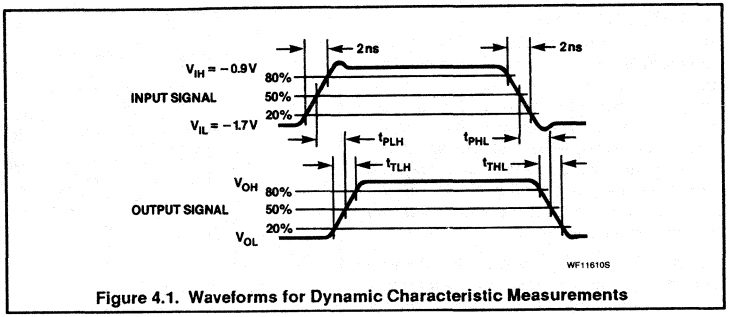


Figure 4.1. Waveforms for Dynamic Characteristic Measurements

EFFECT OF CAPACITIVE LOAD

The speed of an ECL gate is adversely affected by capacitive loading due to the emitter–followers used at the outputs. When the base voltage of an emitter–follower increases, the emitter follows. Any capacitance across the output charges rapidly through the low output impedance of the emitter–follower. But, when the base voltage decreases, the emitter voltage remains fixed momentarily due to the coupled capacitor. Since the base voltage has dropped, the emitter–follower cuts off and any capacitance must discharge through a relatively large emitter resistance. The voltage difference between logic levels is small in comparison to the difference between the supply voltage and the logic level voltages, however, so the discharge time will not be excessively large with moderate capacitive loads.

As with all extremely fast logic gates, the upper limit on fanout of an ECL gate is not due to the DC loading factor, but rather due to the total capacitive load that a gate can drive in a given time.

SETUP AND HOLD TIMES

Two additional dynamic characteristics are often important: the setup time (t_S) and the hold time (t_H). The setup time is the time interval between the active transition of a timing pulse or control input during which the data must be maintained at the input to insure its accurate recognition. A minimum value is specified that is the shortest interval for which correct operation of the device is guaranteed. The setup time can sometimes be a negative value, in which case the minimum limit defines the longest interval between the active transition and the application of the other input signal for which correct operation of the device is guaranteed.

The hold time is the interval during which the data must be retained at a specified input terminal after an active transition of a timing pulse or control input. A minimum value is specified that is the shortest interval for which correct operation of the device is guaranteed. Again, the hold time may have a negative value. In this case the minimum limit then defines the longest interval between the release of data and the active transition for which correct operation of the device is guaranteed.

Chapter 5
100K ECL

ECL Products

ADVANTAGES OF 100K ECL

The 100K family provides a 0.75ns typical internal gate delay, higher on–chip integration, and improved immunity to voltage and temperature variations. Subnanosecond speeds are achieved via an oxide lateral isolation process that allows very small transistors with reduced parasitic capacitance (less than 0.2pF) and very high switching speed (f_T=5GHz). An increased current through the output gates also contributes to faster speed.

A new, smaller flat package with improved propagation and high–frequency characteristics has been developed to support the increased performance offered by the 100K family.

100K ECL devices have better immunity to temperature variations than do 10KH devices. While both 100K and 10KH have internal bias voltage generators that compensate internal thresholds for variations in supply and temperature, only 100K devices offer temperature compensation at device outputs.

THE BASIC 100K GATE

Figure 5.1 shows a standard 100K gate. Note that the 100K gate is similar to a 10K gate, the essential differences occurring in the voltage and temperature compensation networks.

TEMPERATURE COMPENSATION OF A 100K GATE OUTPUT

Additional temperature compensation at the gate outputs is achieved by adding a current–controlling network (R_8, D_1, D_2) between the collectors of Q_2 and Q_3 and by a regulator that generates a constant 1.3V control voltage for the current source, V_{CS}, regardless of variations in V_{EE} or temperature. R_7 and the V_{BE} of Q_5 (Figure 5.1) are designed so that when current, I, is passing through the gate, (R_7) (I)+V_{BE} Q_5 will be equal to 1.3V. When V_{IN} = V_{BB} = +1.3V, current is divided equally between the differential pair formed by Q_2 and Q_3, R_8 is cut off, and the two output voltages are equal: $V_3 = V_4 = (R_3 (I/2) + V_{BE} Q_1$. By design $V_{BE} Q_1$ = $V_{BE} Q_5$, R_7 = $R_3/2$, and $V_3 = V_4 = -V_{CS} = -1.3V$. The switching threshold (central crossover point in the transfer characteristic) is, therefore, stabilized at $V_{IN} = V_{OUT} = -1.3V$, regardless of supply voltage and temperature.

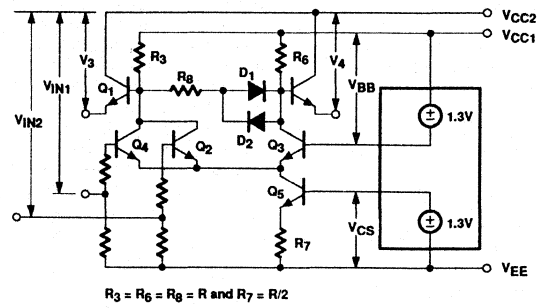


Figure 5.1. Standard Signetics 100K ECL Gate

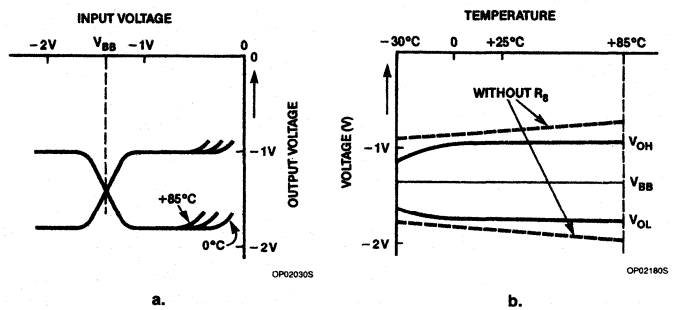


Figure 5.2. Effect of Temperature on 100K ECL Gate with and without Compensation

The V_{BE} of Q_5 decreases with increasing temperature; therefore, for a constant V_{CS}, the current in R_7 increases with increasing temperature. The network (R_8, D_1, D_2) keeps this increase in current stable during variations in the output levels when the gate is fully switched. It also absorbs an increasingly large portion of the current as temperature increases.

Figure 5.2 shows the behavior of the output voltage levels when the stabilization network is not functioning. Below 0°C, practically no current remains in R_8 and the stabilization network ceases to function. Devices can still be utilized below this temperature, but with reduced noise immunity; therefore, 100K ECL device characteristics are not specified below 0°C.

User's Guide

THRESHOLD REGULATOR

The threshold regulator used in 100K ECL devices is shown in Figure 5.3. V_{BB} is regulated to hold the input voltage threshold constant with temperature. V_{CS} is regulated to hold internal thresholds constant over temperature to help keep the output voltage constant.

Since

$$I_{R9} = \frac{(V_{CS} - V_{BE}\ Q_9)}{R_9} \qquad \text{Eq. 5.1}$$

and

$$I_{R11} = \frac{(V_5 - V_{BE}\ Q_{11})}{R_{11}} \qquad \text{Eq. 5.2}$$

the current density, J_9, through Q_9 is determined by R_9 and (V_{CS}–V_{BE} Q_9) and the current density, J_{10}, through Q_{10} is determined by R_{11} and (V_{BE} Q_5–V_{BE} Q_{11}). Also, since V_{CS} and V_5 are connected to V_6 by V_{BE} Q_7 and V_{BE} Q_8, V_{CS} and V_5 are almost equal. Therefore, the ratio between J_9 and J_{10} is fixed by the ratio between R_{11} and R_9.

Due to the physics of semiconductor junctions, (V_{BE} Q_9–V_{BE} Q_{10}) is proportional to the temperature, resulting in a high positive temperature tracking coefficient across R_{10}. The current through R_{10} is the same as that through R_{11} and R_{13}; therefore, they also have a high positive temperature tracking coefficient. R_{11} and R_{13} are designed so that the positive temperature coefficient across them exactly cancels the negative diode tracking coefficient of V_{BE} Q_{11} and V_{BE} Q_6. Thus, the voltages V_5 and V_{BB} are temperature-independent.

Q_{11} is a shunt regulator, with Q_8 and R_{11} in negative feedback between its collector and base. In the absence of current from Q_{10}, Q_{11} sets V_5 at 1 V_{BE} and V_6 at 2 V_{BE}, independent of V_{CC} and any current through R_{12}. Additional current from Q_{10} compensates the negative temperature coefficient of Q_{11}, and makes it possible to maintain V_5 independent of variations in supply voltage and temperature.

The capacitor, C, stabilizes the feedback loop, Q_{11}–Q_8–R_{11}, and prevents oscillations in the regulator when fluctuations occur in current or supply voltage.

This regulator is designed to function across a V_{EE} range of –4.2V to –5.7V.

Figure 5.4 compares the effects of temperature and supply variations on the various ECL logic families.

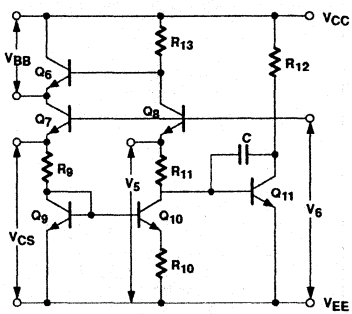


Figure 5.3. 100K ECL Threshold Regulator

PARAMETER	10K	10KH	100K
t_{PD} Variation vs. Temp (ps/°C)	7.0	4.0	0.2
t_{PD} Variation vs. Supply (ps/V)	80	0	0
$\Delta V_{OH}/\Delta T$ (mV/°C)	1.80	1.50	0.06
$\Delta V_{OL}/\Delta T$ (mV/°C)	0.75	0.60	0.10
$\Delta V_{BB}/\Delta T$ (mV/°C)	1.30	1.20	0.08
$\Delta V_{OH}/\Delta V_{EE}$ (mV/V)	16	8	25
$\Delta V_{OL}/\Delta V_{EE}$ (mV/V)	250	20	30
$\Delta V_{BB}/\Delta V_{EE}$ (mV/V)	148	10	25

Figure 5.4. Effects of Temperature and Supply Variations; DC Tracking Rates for 10K, 10KH and 100K Circuits (Maximum Values)

Chapter 6
Transmission Lines

ECL Products

LIMITATIONS OF THE REAL WORLD

Logic functions implemented in the real world must take into account that interconnection wires do not transmit a perfect replica of a theoretical signal, but instead add signal reflections and noise that can cause a system to malfunction. The degree to which noise and reflections will affect a system depends on the speed of the signal being transmitted and the distance the signal has to travel.

The maximum duration of noise or reflections that can be produced on a piece of wire is related to its length, varying between 3 to 4ns/ft of length, depending on the type of insulation used. Therefore, a flip-flop with a minimum set-up time of 10ns can be used with interconnections of up to $^{10}/_{4}$ = 2.4 ft. long without much worry while a flip-flop with a minimum setup time of 2ns may experience problems with wires greater than $^{2}/_{4} = {}^{1}/_{2}$ ft. long.

Simple transmission line concepts allow waveform reflections to be predicted with great accuracy and provides an easy way to look at high-speed system wiring.

SIGNAL TRANSMISSION

Figure 6.1 shows a fixed voltage source, V, connected to a load, R, through a switch and a pair of wires of length x. When the switch is closed, the voltage does not immediately appear across the load. Instead, the voltage propagates from source to load with a finite velocity. Assuming the lines connecting the source to the load have a uniform cross section, the propagation velocity is given by

$$v = \frac{1}{\sqrt{\left(\frac{dL}{dx}\right)\left(\frac{dC}{dx}\right)}} \qquad \text{Eq. 6.1}$$

where L and C are the inductance and capacitance, respectively, of both lines. It turns out that even though L and C each depend on geometry, the propagation velocity itself is not dependent on geometry. When a geometry is reduced, L decreases and C increases such that the product, LC, is relatively independent of geometry. Therefore, the propagation velocity of a wave is determined more by the dielectric constant of the material and less by the geometry.

The reciprocal of the propagation velocity is the "delay per unit length," usually referred to as the "propagation delay."

$$t_{PD} = \sqrt{\left(\frac{dL}{dx}\right)\left(\frac{dC}{dx}\right)} \qquad \text{Eq. 6.2}$$

Figures 6.2a and b show the distribution of the voltage along the line at times $t_1 = x_1/v$ and $t_2 = x_2/v$. At t_1, the line voltage is V from x = 0 to $x = x_1$ and is zero for $x > x_1$. The voltage travels to the right with a velocity v so that at time $t_2 > t_1$ the voltage has propagated to $x - x_2$. As the voltage travels down the line, it is accompanied by a current which charges the capacitance of the line to voltage V. As the current moves a distance dx, the additional capacitance that is charged to voltage V is C_{dx}. The charge required to accomplish this is $dQ=VC_{dx}$. Therefore,

$$I = \frac{dQ}{dt} = VC\frac{dx}{dt} = VCv = VC\frac{1}{\sqrt{LC}} \qquad \text{Eq. 6.3}$$

$$= V\sqrt{\frac{C}{L}} = \frac{V}{Z_O}$$

The parameter $Z_O = \sqrt{(L/C)}$ is called the "characteristic impedance" of the line.

The current, I, in Equation 6.3 above is the magnitude of current flowing from x = 0 up to the point where the voltage front is located. To the right of the voltage front the current is 0. I is positive when current flows to the right on the upper wire of Figure 6.1 and to the left on the lower wire of Figure 6.1.

Let I_X and V_X represent the current and voltage as a function of line distance, x. When the switch closes, a front of voltage, V_X moves to the right on the line with a velocity, v. A current front, I_X, accompanies V_X. The distribution of current on the line at the times t_1 and t_2 is shown in Figure 6.2c and d. The voltage and current on the line, up to their respective fronts, is given by

$$\frac{V_X}{I_X} = \frac{V}{I} = Z_O = \sqrt{\frac{L}{C}} \qquad \text{Eq. 6.4}$$

If the locations of source and load in Figure 6.1 were interchanged, then at the closing of the switch a voltage and current front would start moving toward the left. Using the same sign convention as above, this voltage and current is given by

$$\frac{V_X}{I_X} = \frac{V}{I} = Z_O = -\sqrt{\frac{L}{C}} \qquad \text{Eq. 6.5}$$

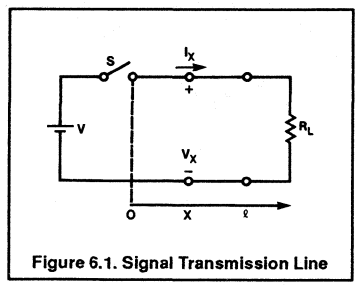


Figure 6.1. Signal Transmission Line

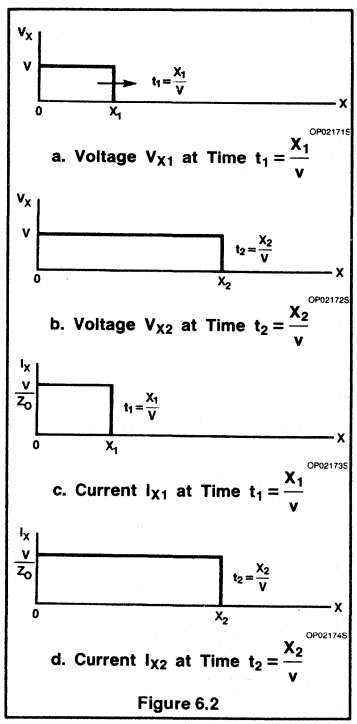


Figure 6.2

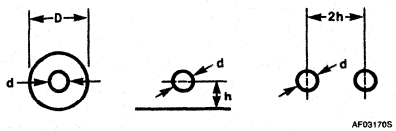
The inductance and capacitance of a line can be determined from Equations 6.2 and 6.4 when the propagation delay, line length and line impedance are known. For a length i and delay T, d=T/i. And

$$L = d(Z_O) \qquad C = \frac{d}{Z_O}$$

User's Guide

THE CHARACTERISTIC IMPEDANCE

The characteristic impedance $Z_O = \sqrt{L/C}$ is a function of the geometry of the cross section of the line. The cross sections of three common lines are shown in Figure 6.3, with the expression for their respective capacitances given below each diagram. Since C increases and L decreases with reduced spacing, Z_O will decrease if the spacing between the two parallel wires in Figure 6.3c is reduced. A dielectric introduced between the wires will increase C while L remains unchanged, again decreasing Z_O. (However, the propagation velocity is also reduced.)



a. Coaxial Cable	b. Wire Over Ground	c. Parallel Wires
$C = \frac{\pi\epsilon}{\ln D/d}$	$C \approx \frac{2\pi\epsilon}{\ln 4h/d}$	$C \approx \frac{\pi\epsilon}{\ln 4h/d}$

Figure 6.3. Three Common Types of Transmission Lines, With Expressions for Capacitance per Meter for Each Type

While the impedance of the coaxial cable in Figure 6.3a depends on the logarithm of the dimension ratio, the logarithm function varies so slowly with changes of its argument that it is generally not feasible to make very large changes in Z_O by changes in dimension. When attenuation of the line results principally from ohmic losses in the conductors, the loss for a fixed D is a minimum for D/d = 3.6. With D/d = 3.6, using a relative dielectric constant of 2.3, $Z_O = 51\Omega$. Most commercially available coaxial lines have impedances under 100Ω. Parallel-wire lines may have impedances up to several hundred ohms.

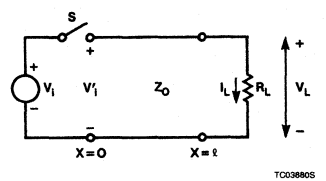


Figure 6.4. Transmission Line Model

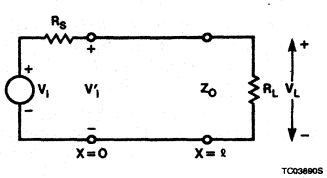


Figure 6.5. Transmission Line With Source Impedance, R_S and $Z_O \neq R_L$

REFLECTIONS

Usually a wave incident on a discontinuity is partly reflected and partly transmitted. Any change in characteristic impedance encountered along a transmission line behaves like a discontinuity. This is due to the fact that Ohm's Law, V = IR, must be satisfied at all times at all points along the line. Rearranging Ohm's Law to R = V/I, if $R_1 = R_2$ then $V_1/I_1 = V_2/I_2$, where R is the impedance encountered along the line and V and I are the voltage and current fronts travelling down the line. Therefore, a reflected voltage and current front will develop such that V_1/I_1 will equal V_2/I_2.

At the moment the switch in Figure 6.4 closes, the voltage source (assumed to have zero internal impedance) applies a voltage V to the line and delivers a current V/Z_O (since the impedance seen by the source looking into the line is the characteristic impedance Z_O). If the line is infinitely long so that the fronts of voltage and current never encounter a discontinuity, the fronts would continue indefinitely and there would be a constant impedance Z_O looking into the line.

If the line is not infinitely long, and a resistor $R_L = Z_O$ is bridged across the line to ground, the bridge would look like an infinite extension of the line. Then, when the switch closes, a front of voltage V and current V/Z_O would travel down the line to the right. After a time, $t = \ell/v$, the fronts will have reached the bridge and from that time on the voltage across the line at any position, as well as the voltage across the bridge, will be V while the current at all points on the line and in the bridge will be V/Z_O. In other words, the fronts reach termination and nothing further happens.

If the bridge resistor R_L does not equal Z_O, a discontinuity exists. When the fronts arrive at $x = \ell$ they will be related by $V_i/I_i = Z_O$. At $x = \ell$ the impedance is now R_L, and the ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current required by R_L. Therefore another voltage and current wave is created at $x = \ell$ in order to satisfy Ohm's law at this point; i.e. a reflection will develop and start moving to the left. The amplitude and polarity of the reflected fronts will be such that the sum of the incident and reflected voltage and current will be

$$V_i + V_r = V_L \qquad \text{Eq. 6.6}$$

$$I_i + I_r = I_L \qquad \text{Eq. 6.7}$$

Thus,

$$I_L = \frac{V_L}{R_L} = \frac{V_i + V_r}{R_L} \qquad \text{Eq. 6.8}$$

Also,

$$I_i = \frac{V_i}{Z_O} \quad \text{and} \quad I_r = \frac{-V_r}{Z_O} \qquad \text{Eq. 6.9 \& 6.10}$$

Solving for V_r,

$$\frac{V_i}{Z_O} - \frac{V_r}{Z_O} = \frac{V_i + V_r}{R_L} = \frac{V_i}{R_L} + \frac{V_r}{R_L}$$

$$= V_i \left(\frac{1}{Z_O} - \frac{1}{R_L}\right)$$

$$= V_r \left(\frac{1}{R_L} + \frac{1}{Z_O}\right)$$

so,

$$V_r = V_i \left(\frac{R_L - Z_O}{R_L + Z_O}\right) = \rho V_i \qquad \text{Eq. 6.11}$$

and,

$$I_r = \frac{-V_r}{Z_O} = \frac{-\rho_L V_i}{Z_O} \qquad \text{Eq. 6.12}$$

Where the parameter ρ_L is the "reflection coefficient" at the load end of the line.

Since

$$V_L = V_i + V_r \qquad \text{Eq. 6.13}$$

then

$$V_L = V_i (1 + \rho_L) \qquad \text{Eq. 6.14}$$

V_L can also be determined without ρ. Using Equation 6.11 above,

$$1 + \rho_L = 1 + \frac{R_L - Z_O}{R_L + Z_O} = 2\left(\frac{R_L}{R_L + Z_O}\right)$$

so

$$V_L = 2\left(\frac{R_L}{R_L + Z_O}\right) V_i \qquad \text{Eq. 6.15}$$

The reflection coefficient lies in the range –1 to +1. When $R = Z_O$, $\rho = 0$; when the end of the line is open, $\rho = 1$; when the end of the line is short–circuited, $\rho = -1$.

A typical situation, where the load is not equal to Z_O, is shown in Figure 6.5. A line with impedance Z_O is terminated at the receiving end by $R_L = Z_O$. The source has an impedance $R_S = Z_O$. Let a voltage, V_L, of amplitude V be applied at t = 0. The input to the line appears to be a resistance Z_O, so at t = 0 + the voltage step at x = 0 is

$$V'_i = \left(\frac{Z_O}{R_S + Z_O}\right)V_i \qquad \text{Eq. 6.16}$$

V'_i travels down the line to the receiving end, where the load would dissipate the entire front and no reflections would occur if $R_L = Z_O$. However, a reflection will develop in this example since $R_L \neq Z_O$. This reflection will again be reflected at the line input, with reflections continuing back and forth. Each time a reflection arrives at the source or receiving ends of the line, its front will be smaller than the incident front so that eventually a steady–state will be established. In the special cases where the reflection coefficients are +1 or –1, excluding the effect of attenuation, a steady–state will theoretically never be attained.

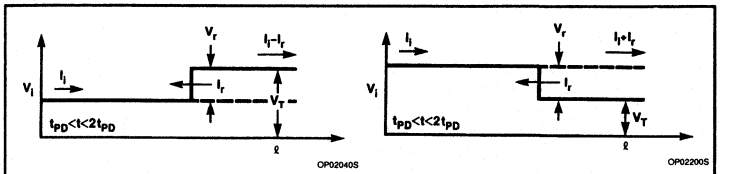
Figure 6.6 shows the effect of the ratio of R_L to Z_O. In Figure 6.6a, $R_L > Z_O$ and a positive voltage is reflected back to the source. To the left of V_r the current flowing to the right is I_i. To the right of V_r the net current flowing to the right is $I_i – I_r$, a net decrease in current. In Figure 6.6b, $R_L < Z_O$ and a negative voltage is reflected back to the source. To the left of V_r the current flowing to the right is again I_i. But to the right of V_r the net current flowing to the right is $I_i + I_r$, a net increase in current.

MULTIPLE REFLECTIONS

The reflection coefficient at the source determines the response to a voltage front reflected back to the source. From Equation 6.11, the reflection coefficient is

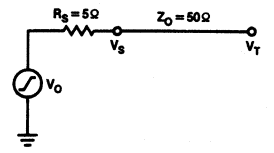
$$\rho = \frac{R - Z_O}{R + Z_O} \qquad \text{Eq. 6.17}$$

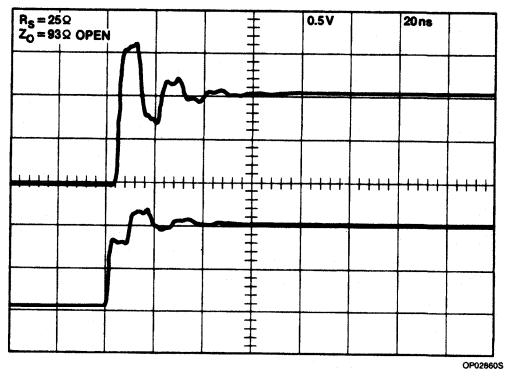
If the source impedance and line impedance match, the reflected wave will not be reflected back to the load and the voltage and current on the line will be stable with the values given in Equations 6.6 and 6.7. But, if neither the source or load impedance matches the line impedance, multiple reflections will occur.



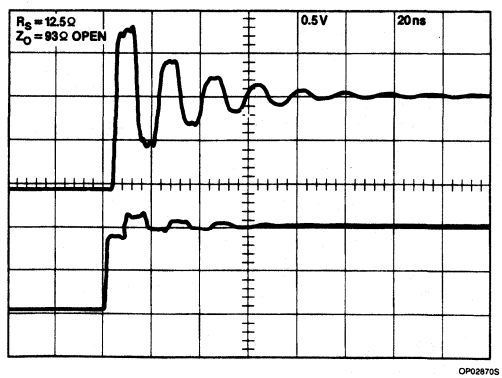
a. $R_L > Z_O$ b. $R_L < Z_O$

Figure 6.6. Effect of the Ratio $\frac{R_L}{Z_O}$





a.



b.

Figure 6.7. Multiple Reflections Due to Mismatch at Load and Source

User's Guide

In the presence of multiple reflections, keeping track of the waves on the line and the net voltages and currents at the ends can be very tedious. A systematic method has been developed to make the job much more convenient. This method combines magnitude, polarity and time into a graph called a lattice diagram. A lattice diagram for the line conditions of Figure 6.7a is shown in Figure 6.8. The vertical lines represent the discontinuities at the ends of the line. A time scale is marked off on each line in increments of 2T, starting at t(o) for V_S and T for V_T. The diagonal lines indicate the voltages and currents travelling between the ends of the line.

The reflection coefficient of the unterminated end of the line is +1. Successive reflections tend toward steady–state of zero line current and a line voltage equal to the source voltage. (If the unterminated end of the line were shorted to ground, the reflection coefficient would be –1 and successive reflections would tend toward steady–state of zero voltage and a line current determined by the source voltage and resistance.) A negative coefficient of reflection always reflects voltage in the opposite polarity. A positive coefficient of reflection reflects voltage in the same polarity.

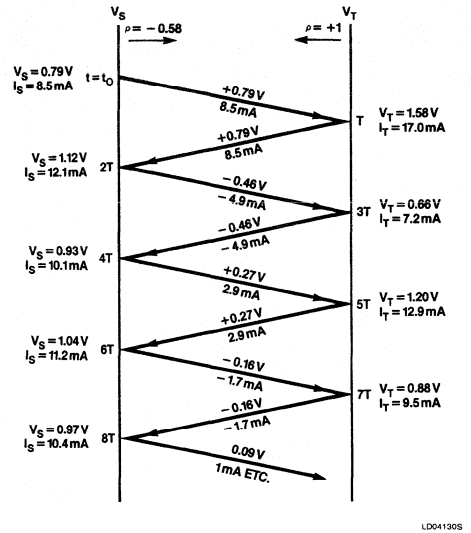
At t = 0, the voltage source switches from 0V to 0.9V. Due to the voltage divider action of R_S and Z_O, the voltage at V_S is:

$$V_S = V_{STEP}\left(\frac{Z_O}{Z_O + R_S}\right) = 1V$$

$$= \left(\frac{93}{118}\right) = 0.79V \qquad \text{Eq. 6.18}$$

The voltages and currents at each point on the lattice diagram are determined by summing all the voltages and currents arriving at and leaving from the point. The process continues until the voltage at the end of the line approaches the new steady–state voltage, i.e., 1.0V in this example. Figure 6.7b illustrates the extended ringing when the source, R_S, is reduced to 13Ω from 25Ω.

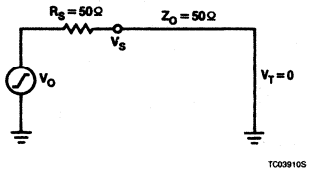
A shorted line, with the reflection coefficient at the source end of the line negative also, is shown in Figure 6.9. Graph 6.9a shows the result when the input step function has a pulse width much longer than the line delay. In this circumstance the reflections constitute a train of positive pulses. Graph 6.9b shows the result when the input step function has a pulse width shorter than the line delay. In this circumstance the reflections constitute a train of positive pulses. Figure 6.9c shows a shorted line for an input pulse duration >> line delay when the source, R_S, and the load, Z_O, are equal (50Ω in this case).

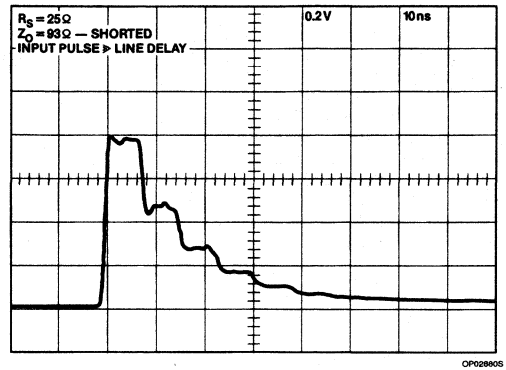


NOTES:
$V_T = 0.79V + 0.79V = 1.58V$
$I_T = 8.5mA + 8.5mA = 17mA$
$V_{2T} = 0.79V + 0.79V - 0.46V = 1.12V$
$I_{2T} = 8.5mA + 8.5mA - 4.9mA = 12.1mA$
$V_{3T} = 1.58V - 0.46V - 0.46V = 0.66V$
$I_{3T} = 17mA - 4.9mA - 4.9mA = 7.2mA$
$V_{4T} = 1.12V - 0.46V + 0.27V = 0.93V$
$I_{4T} = 12.1mA - 4.9mA + 2.9mA = 10.1mA$

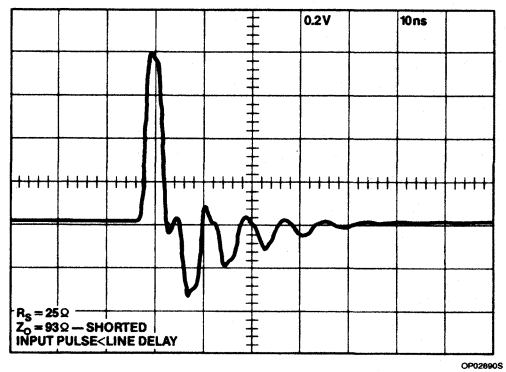
Figure 6.8. Lattice Diagram for Circuit of Figure 7.7

User's Guide

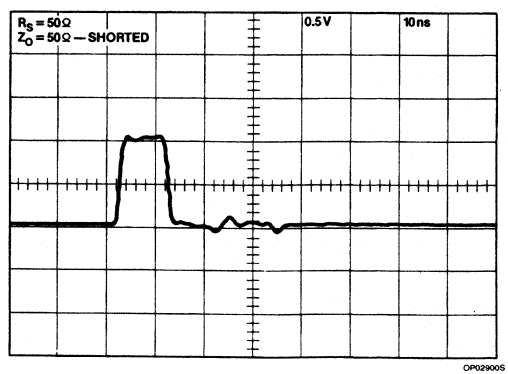




a.



b.



c.

Figure 6.9. Reflections on a Shorted-Line

Chapter 7
Interconnections

ECL Products

PC BOARD INTERCONNECTIONS

Often multilayer PC boards, as shown in Figure 7.1, are used. Interconnections are implemented on one or more layers, with a separate layer (often more) utilized as a ground "plane". The ground plane is a continuous sheet of copper, and the impedance of the ground connection thus becomes so low that the signal appears almost entirely on the signal wire. Therefore, this is a very effective way to reduce ground noise.

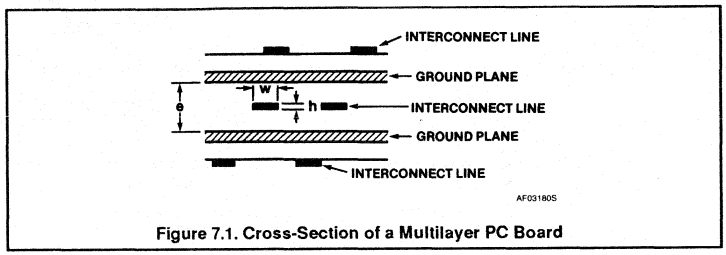


Figure 7.1. Cross-Section of a Multilayer PC Board

The characteristic impedance of a wire over a ground plane is:

$$Z_C = \left(\frac{60}{\sqrt{E_r}}\right) \ln \left(\frac{4h}{d}\right) \qquad \text{Eq. 7.1}$$

where d = wire diameter
h = distance from ground to wire center.

Two common types of PC boards are Microstrip, shown in Figure 7.2, and Stripline, shown in Figure 7.3. Of the two, Microstrip offers easier fabrication and faster signal transmission but complex designs with high packing density will require more design effort. Stripline, providing more interconnect layers, more easily facilitates a high packing density by providing shorter signal paths.

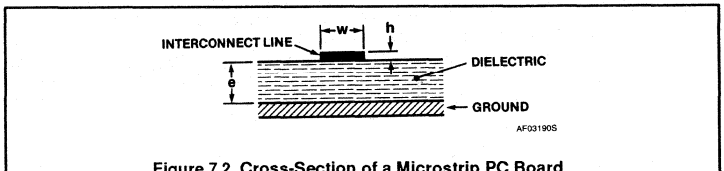


Figure 7.2. Cross-Section of a Microstrip PC Board

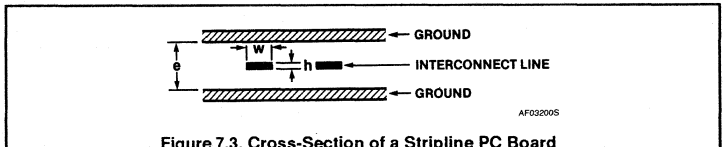


Figure 7.3. Cross-Section of a Stripline PC Board

The characteristic impedance of Microstrip, derived from Equation 7.1 above, is given by the following equation:

$$Z_C = \frac{87\Omega}{\sqrt{E_r + 1.41}} \ln \left(\frac{5.98e}{h + 0.8w}\right) \qquad \text{Eq. 7.2}$$

The parameters e, h, and w are defined in Figure 7.2. E_r is the relative dielectric constant of the insulating material.

From Equation 6.2, the propagation delay is a property of the dielectric material rather than line width or spacing, and

$$t_{PD} = 1.016\sqrt{E_r} \text{ ns/ft.} \qquad \text{Eq. 7.3}$$

where 1.016 is the reciprocal of the velocity of light in free space. The effective dielectric constant can be determined by measuring the propagation delay per unit of length and using Equation 7.3 above.

The characteristic impedance of a Microstrip line, printed in copper on glass–epoxy, is given as a function of dielectric thickness and trace width in Figure 7.4.

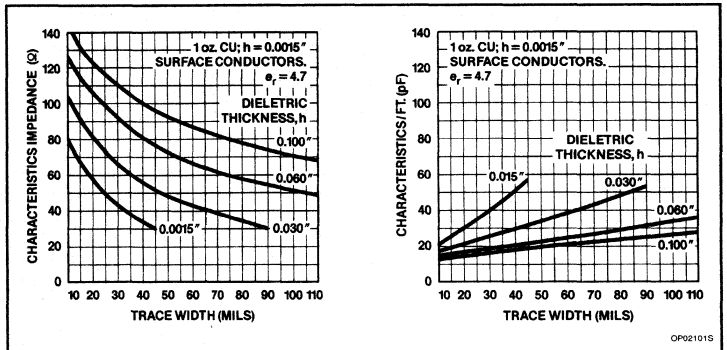


Figure 7.4. Impedance and Capacitance of Microstrip for Various Trace Widths, Printed in Copper on G-10 Epoxy

User's Guide

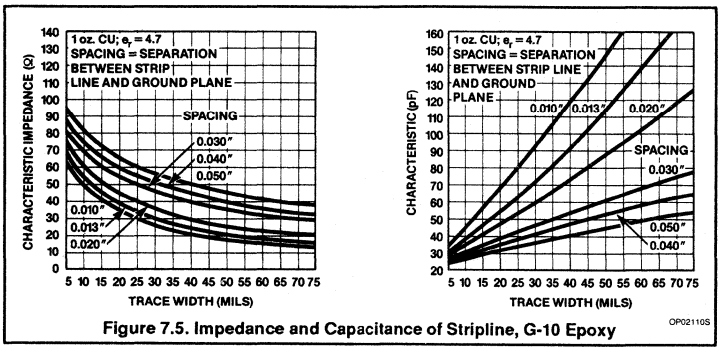


Figure 7.5. Impedance and Capacitance of Stripline, G-10 Epoxy

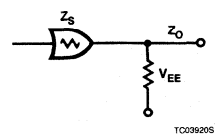


Figure 7.6. Unterminated Transmission Line

When the signal line is enclosed between two ground planes, as in Figure 7.3, the board material determines the dielectric constant. G–10 epoxy Stripline boards have a typical propagation delay of 2.26ns/ft. Using Equation 7.3, the characteristic impedance of Stripline is

Eq. 7.4

$$Z_C = \left(\frac{60}{\sqrt{E_r}}\right) \ln\left[\frac{4e}{0.67\pi(0.8w + h)}\right]$$

The characteristic impedance of Stripline, printed in copper on glass–filled epoxy, is given as a function of dielectric thickness and trace width in Figure 7.5.

ECL CIRCUIT INTERCONNECTIONS

Consider the connection of the output of a driving ECL gate to the input of a driven gate. The emitter-follower driver acts like a source. It has a low output impedance (< 10Ω including the package pin and internal connection). The characteristic impedance of high-speed PC board interconnections is usually in the range of 40 to 60Ω, depending on line width and insulating material used. The line load consists of the input impedance of the gates connected on the line, and any termination resistors that may be present. The input resistance (several kΩ) of gates connected on the line can be ignored because input capacitance, usually several pF, outweighs the effects of input resistance.

A model for the interconnection between ECL gates can be represented by a line of one-way delay, t_D, with characteristic impedance, Z_O. The sending end termination is $R_S << Z_O$ and the receiving end termination is $R_L >> Z_O$.

As discussed in the previous chapter on transmission line theory, any change in characteristic impedance encountered along a transmission line behaves like a discontinuity and causes reflections to occur.

LINE TERMINATION

Let's consider the case where a transmission line has no termination (an "open line"). At t = 0, a voltage front, V, starts at x = 0 and travels down the line (Figure 7.6). At $t=t_D$, the front reaches x = 1 and is reflected with a reflection coefficient of

$$\rho_L = \frac{R_L - Z_O}{R_L + Z_O} = 1 \qquad \text{Eq. 7.5}$$

since the inpedance of the load is very hgih with respect to Z_O. At $t = 2t_D$, the reflected front will reach x = 0 and be reflected by with a a reflection coefficient of

$$\rho_L = \frac{R_S - Z_O}{R_S + Z_O} = 1 \qquad \text{Eq. 7.6}$$

because R_S is very low with respect to Z_O. The negative reflection results in a front at x = 1 at time $t = 3t_D$ that travels in the opposite direction to the initial front. Positive reflections cause the signal to "overshoot" the initial voltage level, and negative reflections cause the signal to "undershoot" the initial voltage level. When occuring together, these reflections cause a condition known as "ringing."

If the signal line is short, the initial signal will still be rising at $t = t_D$ and the reflection will become part of the rising edge. If the signal line is long, the rise of the signal will be completed before $t - t_D$ and the reflections will act like overshoot and undershoot. Therefore, unterminated lines have a maximum recommended length

$$l_{max} \leq \frac{t_R}{2\ t_{PD}} \qquad \text{Eq. 7.7}$$

where t_R = rise time
t_{PD} = propagation delay/unit length.

There are two configurations generally used to terminate transmission lines: (1) terminating the line at the receiving end, which is called "parallel termination;" and (2) driving the line through a resistor inserted at the output of the gate, which is called "series termination." These are shown in Figure 7.7.

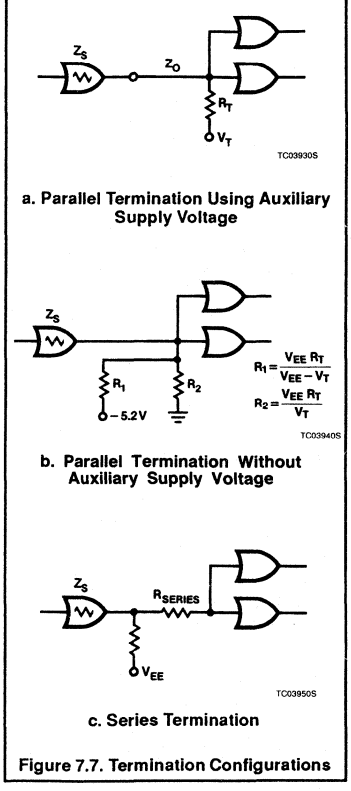


Figure 7.7. Termination Configurations

Parallel termination is used for highest speed and for driving distributed loads. Since Philips Components–Signetics' ECL devices do not have internal pull–down resistors on the outputs, the terminating resistor must be returned to a voltage more negative than V_{OL}, commonly –2V. No additional pull-down resistors are required at the output of the driving gate.

User's Guide

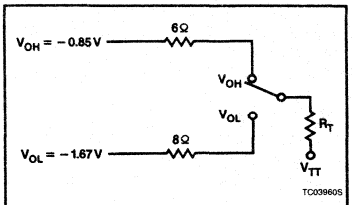


Figure 7.8. Termination Load Model Circuit

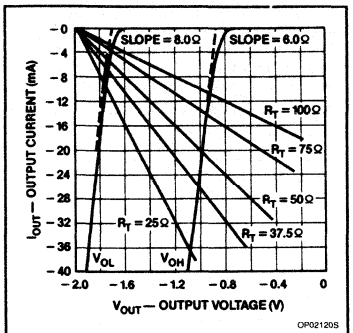


Figure 7.9. Output Characteristics With Terminating Resistor Returned to V_{TT} = −2.0V

The configuration shown in Figure 7.7b allows parallel termination without the use of a separate termination supply. In this configuration, a pair of resistors is connected in series between V_{CC} and the V_{EE} supply. The values of R_1 and R_2 are chosen to provide the Thevenin equivalent of the single resistor to −2V shown in Figure 7.7a.

There is a trade-off between the two parallel termination configurations. While the latter eliminates the need for a separate V_T supply, its average power dissipation is close to 10 times the power dissipation of the former configuration. Decoupling capacitors are required between the supply and ground for both configurations.

Philips Components–Signetics' ECL output transistors are designed to drive low impedance loads with a maximum output current of 50mA. Using a 50Ω load returned to −2V gives nominal output levels of −0.955V at 20.9mA and −1.705V at 5.9mA. These output levels will vary with load current due to the fact that the transistor's output resistance is nonlinear with load current (the V_{BE} of the emitter-follower is logarithmic with output current). The effective source resistance, using a 50Ω load, is approximately 6Ω in the HIGH state and 8Ω in the LOW state.

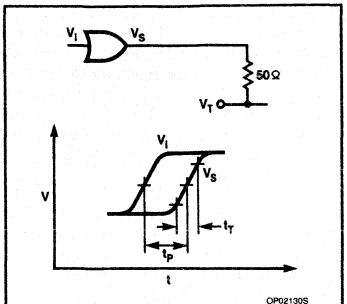


Figure 7.10. ECL Gate Output Characteristic With 50Ω Load

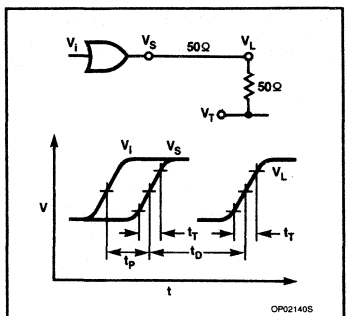


Figure 7.11. ECL Gate Output Characteristic With Matched Long Line

The circuit shown in Figure 7.8 can be used to estimate quiescent output levels at various loads. The linearized portion of the output characteristic is given by

V_{OH}: V_{OUT}=−850mV−(6Ω) (I_{OUT} mA)

V_{OL}: V_{OUT}=−1670mV−(8Ω) (I_{OUT} mA)

Results are given in Figure 7.9.

Since ECL outputs can drive two or more lines in parallel (provided the load does not cause the maximum rated current to be exceeded), the effect of load configurations on noise margin should be considered. Using Figure 7.8, two parallel 75Ω terminations provide V_{OH}= −1.00V and V_{OL} = −1.72V, approximately. A single 50Ω termination provides V_{OH} = −0.96V and V_{OL} = −1.73V, approximately. The single 50Ω termination, therefore, provides 35mV less margin for V_{OH} and 10mV more margin for V_{OL}. Two parallel 50Ω terminations provide V_{OH} = −1.07V and V_{OL} = −1.75V, 110mV less margin for V_{OH} and 10mV more margin for V_{OL}.

When using series termination, a resistor value should be selected such that the driver source resistance plus the series resistor equals the line impedance. The net series resistance and the line impedance act like a voltage divider and cause an incident wave of half amplitude to travel down the line. The coefficient of reflection of an open line is +1, so when the incident signal arrives at the unterminated end of the line it will double and be restored to its full amplitude. If the combination of the series resistor and drive source resistance equals the line impedance, the reflected wave will be absorbed without further reflection, eliminating any possibility of ringing. The ability to absorb reflected waves makes series termination good for interconnection configurations having impedance discontinuities, such as backplane wiring.

A disadvantage of series termination is that driven inputs must be near the end of the line to avoid receiving a 2–step signal. An input will receive a full amplitude signal with a continuous edge provided the distance, l, to the open end of the line is within the recommended length for unterminated lines (Equation 7.7).

MATCHED LONG LINES

The output signal of an ECL gate with a 50W load is shown in Figure 7.10. An applied input voltage, V_{IN}, has a corresponding output voltage, V_S, characterized by a propagation time, t_P, and a transition time t_T.

A line having characteristic impedance of 50Ω, terminated by a resistor having the same value, behaves like a pure 50Ω resistor and, therefore, can be used to load the gate without affecting its behavior (Figure 7.11). The output voltage V_S of the gate has the same t_P and t_T as in Figure 7.10. V_S propagates along the line until it reaches the load resistor. The voltage across the 50W load resistor will be identical to V_S after a time equal to the propagation delay of the line.

MISMATCHED LONG LINES

If the load terminating the line is not a 50Ω resistor, as shown in Figure 7.12, the output voltage remains the same as it was in the preceding case and is transmitted over the line in the same manner. However, the voltage will be deformed by the load voltage, V_L, when it arrives at the load and will not have the same form as V_S. If the load is capacitive, then the edge t_{T2} will be slower than the edge at the gate output t_{T1}, and an additional delay will be added to t_D. Also, because the resistive portion of the load differs from 50Ω, the amplitude of V_L will be different.

The effect of a load can be calculated from the diagram shown in Figure 7.13. The difference between V_L and the incident wave, V_S, will be reflected toward the gate causing a perturbation in the voltage at time $2t_D$.

User's Guide

SHORT LINES

If the line is short; i.e., if t_D is less than or equal to t_T, then it is difficult to separate V_S and V_L at the line terminals. Therefore, it is preferable in this case to discard the transmission line concept and work instead from the equivalent diagram shown in Figure 7.14.

MULTIPLE LINES

Figure 7.15 shows an ECL circuit driving multiple lines. The signal from gate G_1 is distributed successively to gates G_2, G_3 and to the group of gates, G_4 through G_6. A matching resistor, R_T, is placed as far as possible down the line to minimize the length, L_1, of "non–terminated" line.

The effect of the capacitance of this non–terminated, and therefore unmatched, portion is reduced by giving it a high characteristic impedance, Z_1. The reflections generated by the input capacitances of gates G_4 through G_6, and the unmatched line segments that connect them to the main line, should be limited to 15% or 20% of the amplitude of the signal to maintain proper noise immunity between the gates. This factor is usually the main limitation to fanout.

The product ($Z_C \times C_T$), where C_T is the sum of the capacitances loading the line, should not exceed the transition time, t_T, of the signal driving the line. Therefore, it is the input capacitance of the other gates that causes the limitation to fanout. Fanout is typically 3 gates, but can exceed 8 gates if the system is well designed.

It is possible to branch a 50Ω line into two 100Ω lines, or three 150Ω lines, as shown in Figure 7.16. In this configuration, each line is terminated by a load corresponding to its characteristic impedance.

BUS LINES

Bidirectional buses for ECL can be constructed by interconnecting gate outputs and inputs along a matched line terminated at both ends. Each gate output will then appear to be loaded by two lines in parallel; i.e., by $Z_C/2$. In this configuration, a signal can be propagated from one gate to another gate only if the outputs of the non–active gates are in the LOW state.

Bus drivers are available to provide optimum results under these conditions. These devices can generally provide more current and voltage that ordinary gates, and with less sharp edges, to minimize reflections.

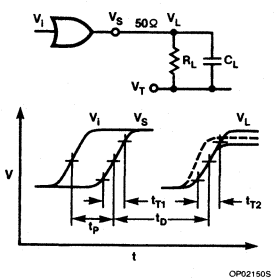


Figure 7.12. ECL Gate Output Characteristic With Mismatched Long Line

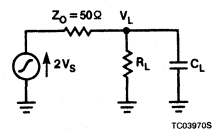


Figure 7.13. Equivalent Load Circuit

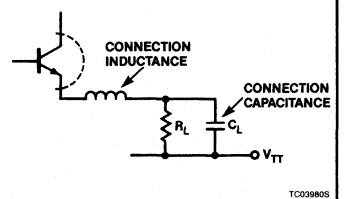


Figure 7.14. Equivalent Circuit for Short Line

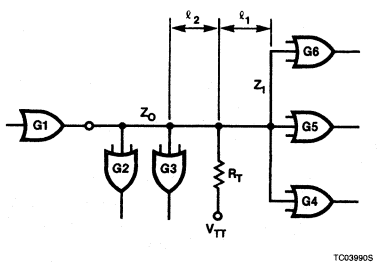


Figure 7.15. ECL Gate Driving Multiple Lines

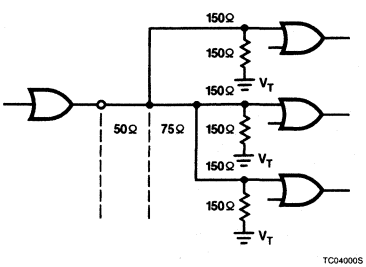


Figure 7.16. 50Ω Line Branched Into Three 150Ω Lines

Chapter 8
Power Supplies

POWER SUPPLY CONFIGURATIONS

The most common power supply network used in ECL systems consists of three distribution lines (Figure 8.1):

1. the overall V_{CC} line;
2. the termination voltage, V_T, line; and
3. the switching-state voltage, V_{EE}, line.

Two different voltage sources are used to supply V_T and V_{EE}. V_T is on the order of –2V, and V_{EE} is on the order of –4.5V to –5.2V, depending on the family. Thus, the network consists of two interleaved current loops, each with different functions.

The V_{EE} loop supplies the current for the biasing networks, the switching stages, and for some of the internal circuit loads. These currents are relatively constant. As explained in the preceding chapter, gate function is insensitive to the value of V_{EE}. The V_{EE} power supply receives almost no high-frequency current components when the gates switch.

The V_T loop supplies the current for the gate output loads. This current is affected by sudden transients. Using a 50W output resistor, this current changes from 8mA to 22mA within one or two nanoseconds whenever the gate output switches.

The V_{CC} connection, which serves as a reference potential for the logic signals, receives the sum total of these two currents simultaneously (one with a strong continuous component and the other with a strong alternating component).

STATIC PARASITIC EFFECTS

The power density distributed on boards implemented in ECL can exceed 10W/cm^2. This means that currents passing through the board can reach 2A/cm^2. These currents can cause ohmic voltage drops in the distribution lines, in connectors, in printed circuit traces, and even in the package pins themselves. Therefore, all circuits do not receive exactly the same V_{CC} voltage.

A difference between supply voltages can cause a reduction in noise immunity. For example, if a 20mV loss of noise immunity is acceptable, then the line must represent less than 0.02V/2A=0.01Ω. A resistance this low requires a large cross-section for V_{CC} connections.

The effect of V_{CC} on noise immunity is four times larger than that of V_{EE} for 10K ECL, and approximately twenty times larger (due to the bias regulator) for 100K ECL. Consequently, a larger distribution resistance is tolerated by V_{EE}.

The effect of V_T on output levels and noise immunity depends on the relationship between the load resistances (50Ω) and the gate output resistance (6 to 12Ω). It turns out, therefore, that V_T is just as tolerant of voltage drops as V_{EE} is.

Depending on whether a system consists primarily of simple circuits (with many outputs per gate) or of complex circuits (with many gates per output), either the V_T line or the V_{EE} line will be the more critical from the point of view of static voltage drops. Power supplies that provide both V_T and V_{EE} also reduce static noise immunity as a function of loading. This should be kept in mind when designing a system.

In small systems using one power supply it is advisable that the power supply and its regulator be connected by four separate lines: two to carry the input current, and two for remote voltage sensing. This technique, known as a "Kelvin connection," is shown in Figure 8.2.

When several sub–systems have independent power supplies, a power supply connection, as shown in Figure 8.3b, prevents current passing through the link between the V_{CC} lines and guarantees the supplies will provide equal voltages.

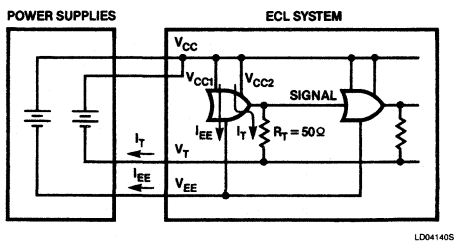


Figure 8.1. ECL Power Supply Network

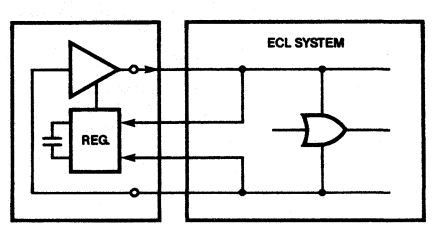
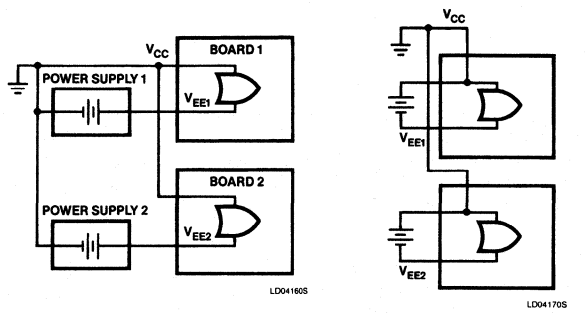


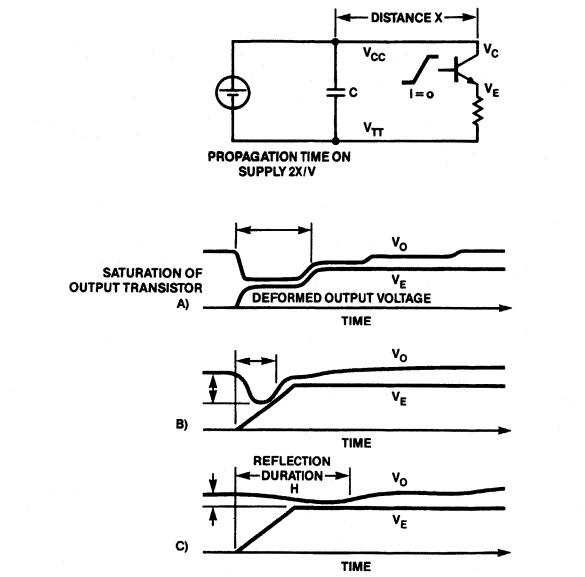
Figure 8.2. Kelvin Connection of Power Supplies

User's Guide



a. Wrong: Non-Equipotential V_{CC} b. Right: Equipotential V_{CC}

Figure 8.3. Coupling of Multiple Power Supplies



A) Capacitor too far away
B) Capacitor nearby
C) Distribution with low characteristic impedance

Figure 8.4. Decoupling of an ECL Gate

DYNAMIC PARASITIC EFFECTS

Figure 8.4 shows the effect of distance between the decoupling capacitor and output pin of an ECL circuit. The distance, x, acts like an inductance in series with the circuit and limits the effectiveness of the decoupling regardless of the value of the capacitor. Too large a distance between the decoupling capacitor and output pin could allow saturation of the output transistor and create a significant delay in response.

Two methods of decoupling are generally used. One consists of placing a decoupling capacitor at a distance of less than one centimeter from each 100K ECL package, and at a distance of less than five centimeters from each 10K ECL package (as shown in Figure 8.4b). These capacitors should, of course, be suitable for very high–frequency decoupling—several tens of nanofarads in value and constructed with high-quality dielectric material with low absorbtion characteristics.

In the second method, shown in Figure 8.4c, a long duration of reflection is acceptable because the reflection's amplitude is reduced by the power distribution having a very low characteristic impedance, thus providing an equivalent low inductance. This is obtained by means of large capacitors located near one another. In this case, the best solution is to use a multi-layer PC board with separate parallel planes for ground and V_{TT}. (If using a single- or dual-layer PC board, capacitance rails can be placed vertically on the PC board.) The impedance of the two parallel plane conductors can be calculated from:

$$Z_C = \frac{120\pi\ ht}{d\sqrt{E_r}} \qquad \text{Eq. 8.1}$$

where:

- h = the thickness of the dielectric between the conductors
- d = the width of the smaller conductor
- t = the relative dielectric constant of the insulating material
- Z_C = the characteristic impedance (expressed in Ω)

With Z < 1Ω, currents on the order of 20mA will cause voltage fluctuations of less than 20mV on the power supply lines, which is acceptable. Having Z_C too high risks interaction between two circuits, even in the absence of a signal on their inputs, due to fluctuations of voltage on the V_{CC} line. This in turn creates a risk of oscillation. On isolated circuits, excessively inductive power supplies can cause coupling to occur between inputs and outputs. The resulting oscillations can, over the long term, destroy some junctions in the input stage or in the regulator.

Chapter 9
Packages and Thermal Constraints

ECL Products

Integrated circuits implemented on silicon chips must generally be mounted in a package to be used. This package, located between the circuit and its environment, imposes its own characteristics, or modifies those of the chip. In ECL, this effect is especially important.

ROLE OF THE PACKAGE

First of all, the silicon chip is very small, mechanically fragile, and difficult to handle. It can be subject to corrosion, especially at the level of its connections to the outside world (metallic interfaces).

Finally, the chip is a major source of heat during operation. This heat must be removed efficiently to avoid the risk of rapid destruction of the chip due to excessive temperatures.

In view of these problems, the package provides greater ease of handling, and mechanical protection for the chip against shocks, scratches, and corrosive atmospheres. It also makes connections to the circuit easier, by connecting the fragile, microscopic areas on the silicon to sturdy metallic pins, which are accessible and easy to solder. This also makes circuit testing easier. On the thermal level, the package conducts the heat of the chip toward a larger surface area, and also makes chip–cooling easier to control.

THERMAL BEHAVIOR OF THE PACKAGE

The silicon chip acts as a heat generator connected to a heat media (the ambient air) by means of an environment consisting of different substances that present a resistance (depending on their type and size) to the circulation of the thermal flow.

The temperature of the chip is an important parameter, for both the electrical performance of the circuit and its reliability. It should be noted that the lifetime of a component is reduced by half for each 10°C increase in temperature. This is true for all logic families; but ECL circuits require more attention because their power level is generally higher.

The calculation of thermal resistances depends on several factors.

The chip acts as a heat generator which, by means of the Joule effect, provides a power W which it receives in electrical form from its power supplies. This power W has approximately the value of the product $V_{EE} \times I_{EE}$, to which must be added the power dissipated in the output transistors: ($V_o \times I_o$). The power associated with the inputs can generally be ignored (see Figure 9.1).

In order for this heat to be removed, the temperature of the chip must increase above that of the surrounding environment. The ratio between the difference in temperature (once it has stabilized) and the amount of heat dissipated is termed the "thermal resistance", θ.

Each element in the path of the thermal flow thus presents resistance, and the entire set of resistances is associated, in series or in parallel, to form the overall thermal resistance.

Thus, the package shown schematically in Figure 9.2 behaves thermally in a way that is analogous to the thermal behavior of the network shown in Figure 9.3. The characteristic temperatures are T_1 (the temperature of the junctions on the chip), T_3 (the temperature of the package wall), and T_5 (the initial temperature of the cooling air).

The thermal resistances to be taken into consideration belong to three types:

1. Conduction thermal resistances in solids: such as the silicon of the chip, the ceramic or plastic of the package, the metal of the pins, the glass-epoxy plane and the copper traces of which the printed-circuit board consists, etc.;
2. Convection thermal resistances related to a fluid medium: exchanges between the package wall and the ambient air, and (if applicable) between the wall of a tube and the cooling liquid, heat-transport phenomena within fluids in motion (ventilated air);
3. Radiation thermal resistances related to the heated surfaces. Some of these resistances are determined by the circuit manufacturer, who generally specifies the thermal resistance θJC between the internal heat-source (junctions of integrated circuits) and the package wall. On the other hand, the rest of these resistances depend on the user, who defines the mechanical assembly (part of the heat being dissipated via connections) and the ventilation conditions.

Thermal resistances can be calculated based on the specific thermal conductivities of the materials used.

Good thermal conductors, such as gold, aluminum, and copper, have conductivities from 200 to 400W/cm/°C; steel and alumina (of which ordinary packages are made) have lower conductivities, e.g., 15 to 30W/cm/°C. Still air and plastic substances (epoxy, etc.) are bad thermal conductors, typically having conductivities of less than 0.2W/cm/°C.

The standard method of removing heat from the package to the ambient environment is a mixture of convection and radiation, for which the theoretical analysis is very difficult. The power emitted by radiation is proportional to the surface area of the package, and to the fourth power of the absolute temperature of the emitting body (Stefan's Law), and depends greatly on the color of the package and on the condition of its surface.

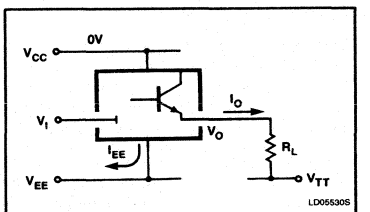


Figure 9.1. Evaluation of the Power Dissipated

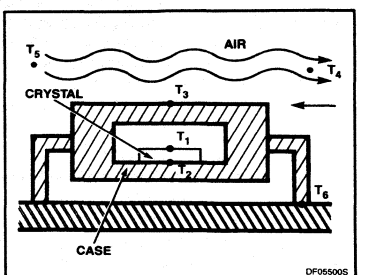


Figure 9.2. Thermal Analysis of a Flat Pack Package

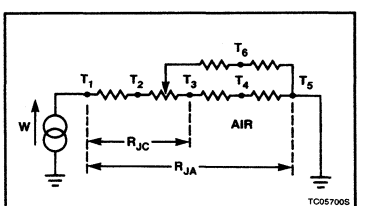


Figure 9.3. Thermal Diagram Equivalent to the Package Shown in Figure 9.2

User's Guide

Surfaces that are matte black in color allow better emission. However, within a system, this phenomenon is very limited, because the energy radiated by a package is essentially re-absorbed by the packages surrounding it, and vice-versa. Overall, this phenomenon does not contribute toward cooling the system.

Therefore, the principal phenomenon is convection, whether natural (air movement caused by the difference in density between the air heated by the package and the surrounding air) or forced (by a fan with a known speed).

Thermal resistance decreases as the air-flow increases, and as the surface area of the package exposed to the flow increases. ECL packages are generally specified for a transverse air-flow of 2.5 meters per second.

For low air-flow speeds (those less than one m/s, or natural convection), thermal resistance is not very well defined, and depends greatly on the environment and on the measurement conditions, inasmuch as the actual air-speed at the level of the package wall can be non-homogeneous, or very different from the measured speed.

Figure 9.4 shows, for a flat ECL 100K package, an example of the variation of the junction-to-ambient-air thermal resistance as a function of the air-flow rate. Therefore, it is important to ensure good ventilation of the circuits, so as to be certain of the measurement conditions and of the operation of the circuits.

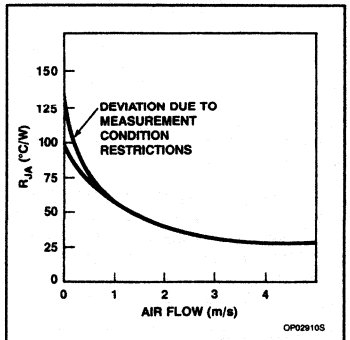


Figure 9.4. Thermal Resistance of a Flat ECL 100K Package as a Function of the Air-flow Rate

It should be noted that in very dense ECL systems containing many LSI packages side-by-side, some manufacturers use a cooling liquid (water or freon), because air-cooling is not sufficient to maintain a reasonable temperature at the junction area.

PRINCIPAL ECL PACKAGES

The ECL logic families, and memories, are available in conventional plastic or ceramic dual-in-line packages (DIPs). ECL 10K comes in 16-pin packages, and ECL 100K in 24-pin packages. The thermal resistance of the 16-pin package is approximately 50°C/W, and that of the 24-pin package is approximately 35°C/W, under normal utilization conditions (transverse air flow of 2.5m/s). In the absence of ventilation, these values can double or triple, which would be harmful to the circuits. The advantage of these packages is their easy insertion into boards, which makes them compatible with the utilization of automatic-insertion equipment. The disadvantage is that electrical performance of extremely fast circuits, such as ECL 100K, is penalized by 200 to 400ps.

For these reasons, another type of package is preferred by some customers: the "flat pack."

ECL 100K is available in a flat, square, 4×6-pin package, which has a thermal resistance of 30°C/W under normal conditions. Because of the smaller size of this package, the propagation time through the pins is shorter (on the order of 50ps), and parasitic inductances are smaller. The ability to place the packages closer together also makes it possible to reduce the length (and thus the propagation time) of connections between packages. However, these packages are more delicate, requiring greater care in handling and mounting, and are therefore more expensive to use.

When even denser interconnections are necessary, it is also possible to use ECL circuits in micropackages ("mini-DIP") or in leadless chip-carriers. This approach can cause problems for circuits having high power dissipation, but many 10K device types can be put into the SO package and are being offered as customer demand dictates. A ceramic J-lead chip-carrier package has been developed for 100K devices and will be available in the very near future. Contact your Field Applications Engineer or salesman for information.

In the case of highly complex integrated circuits (such as gate arrays), the amount of power dissipation (several watts) and the number of pins (50 to 200) require special attention. Special packages have been designed to solve these two problems, and several types can be utilized, depending on whether the cooling is by air or by a liquid, and depending on the method selected for placing them on the printed circuit board.

Chapter 10
Interfacing ECL Families

ECL Products

ECL is sometimes used in a system only in areas in which speed is critical. The rest of the system is implemented in slower technologies. Therefore, it is necessary to know how to interface between ECL circuits and other circuits. Precautions are also necessary when ECL circuits belonging to different families are connected to one another; and even when circuits in the same family, but located on different cards or in different sub-systems, are connected. This section provides several recommendations for implementing these interfaces.

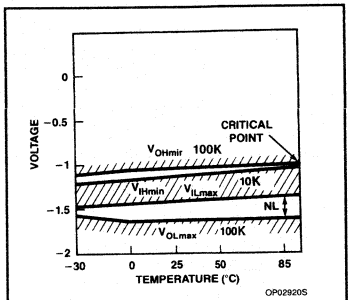


Figure 10.1. Static Levels— an ECL 100K Output Controlling an ECL 10K Input

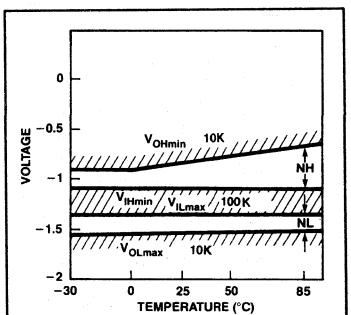


Figure 10.2. Static Levels— an ECL 10K Output Controlling an ECL 100K Input

INTERFACING 10K ECL TO 100K ECL

The problems encountered are mainly due to circuit power supplies and to the different behavior of logic levels depending on the temperature. With regard to the power supply, the ground for the two circuits should be the same. ECL 100K can operate at –5.2V and specification guarantees over this supply range are given in this data book for each Signetics 100K device. On the other hand, generally speaking, ECL 10K cannot operate at –4.5V. Therefore, two methods can be used. First, one could use two separate V_{EE} power supplies, which would be complicated and expensive; or else one could use a single –5.2V power supply. The latter solution is generally preferred when 100K circuits are in the minority in a system.

The diagrams in Figure 10.1 and Figure 10.2 show that direct 10K/100K coupling is functional throughout the temperature range, even though noise-immunity is reduced (mainly when an ECL 100K circuit controls a 10K circuit at high temperature).

In this case, it is recommended that the supply voltage of the 10K circuit be increased slightly (for example, to –5.5V). A more rigorous approach consists of utilizing a special 100K/10K interface circuit (100175), which has 100K input thresholds and 10K output levels. The "buffer register" function of this circuit also facilitates the asynchronous transfer of data between sub-systems, at different speeds.

INTERFACES BETWEEN ECL BOARDS

By utilizing the conventional interconnection system consisting of wires or "wrapped" panels between ECL boards, one risks causing phenomena such as ECL signal reflections at impedance discontinuities, or signal cross-coupling via radiation or by mutual capacitance.

Because the magnitude of these effects increases with the frequencies present in signals transmitted, and therefore with the sharpness of the edges, the simplest solution is to filter the signals as they are output from the boards by utilizing output circuits with especially slow edges (ECL 10K rather than ECL 100K), or special circuits. The outputs can also be slowed by capacitors on the order of 100pF, but the slopes obtained are not symmetrical (faster on the rise).

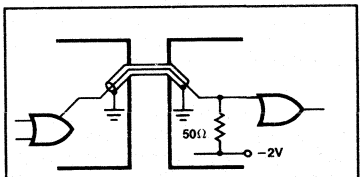


Figure 10.3. Interconnection Between Boards Via a 50Ω Coaxial Cable

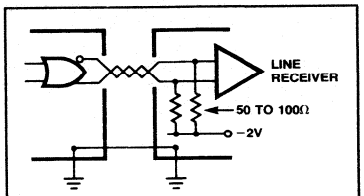


Figure 10.4. Twisted-Pair Cable Link

A radical solution to this type of problem is to implement the interconnections between boards by means of 50Ω coaxial cables.

This method is used when the connections are fairly few, because of the high cost of this technique (see Figure 10.3).

Good results can also be obtained with twisted-pair wire connections driven by complementary signals. These signals can be provided by most ECL gates.

The symmetrical dual-wire line has a regular characteristic impedance, and emits very little radiation. Therefore, its performance is scarcely worse than that of a coaxial cable. It also has the advantage of allowing the use of more conventional connectors. At the end of the line, a special "line receiver" with dif_ferential inputs should be used (see Figure 10.4).

This type of link allows great noise immunity, even when the grounds of the boards do not have exactly the same potential.

User's Guide

If absolutely necessary, ECL 10K signals can be transmitted via flat or ribbon cables provided that the signal and its complement are transmitted simultaneously on adjacent lines, so as to reduce radiation and coupling, and to systematically separate the pairs thus formed by ground lines. Thus, structures are obtained whose characteristic impedance is fairly regular, as indicated in Figure 10.5.

For short connections, a line receiver is not necessary. The characteristic impedance of flat cables is generally indicated by the cable manufacturer, so that the termination resistor can be selected.

All of these precautions become less critical when the links are short. Nevertheless, a signal connection should never be placed as far as several millimeters from a ground-plane, or from a connection transmitting the complementary signal. This way most echos and parasitic radiation can be avoided.

INTERFACE TO TTL CIRCUITS

The following remarks pertaining to TTL circuits also apply to all the circuits that are compatible with TTL levels and power supplies (TTL, TTL-LS, TTL-S, NMOS, and 5V CMOS circuits).

In all large systems in which ECL is utilized extensively, there is a negative power supply (V_{EE}) for ECL, and a separate positive power supply (V_{CC}) for TTL. These power supplies share a common ground. Translation circuits must be used to transmit signals between the two groups (see Figure 10.6).

There are two types of translation circuits:

1. Unidirectional interfaces, having inputs in one logic family, and outputs in the other. These perform very simple logic functions, as indicated below:

   TTL/10K interface: 10124

   10K/TTL interface: 10125

   TTL/100K interface: 100124

   100K/TTL interface: 100125

2. Bidirectional interfaces, allowing transmission in both directions, controlled by auxiliary logic signals, to define the direction of transmission and (in some cases) to improve the signal (see Figure 10.7). For example:

   TTL 100K interface: 100255

INTERFACE TO CMOS CIRCUITS

Some CMOS circuits require power at 9 to 12V, and have no TTL-compatible levels.

Although direct interfaces with ECL are fairly rare, they are possible by interfacing first via an ECL/TTL translation circuit, and then through a TTL gate with an open-collector output.

This interface is complex to use (see Figure 10.8). Furthermore, if there is no V_{CC} power supply for TTL within the system, it would be wiser to build the interface with discrete components.

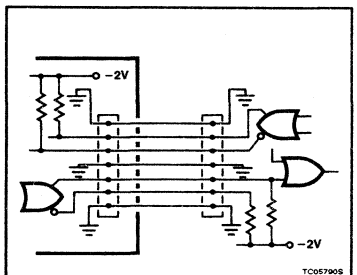


Figure 10.5. Flat-Cable Link

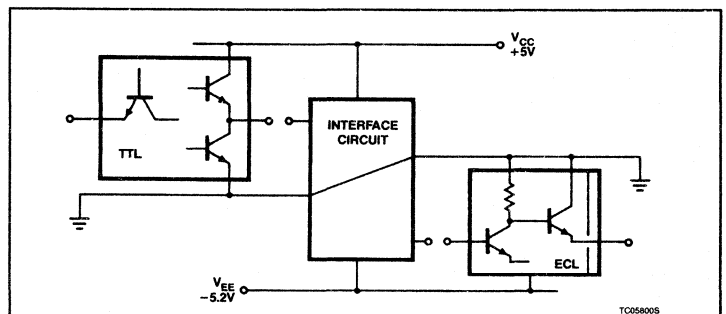


Figure 10.6. ECL/TTL Interfaces

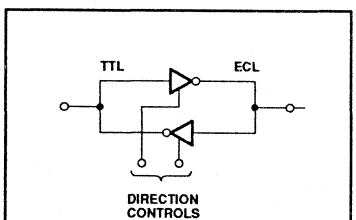


Figure 10.7. Bidirectional Interface

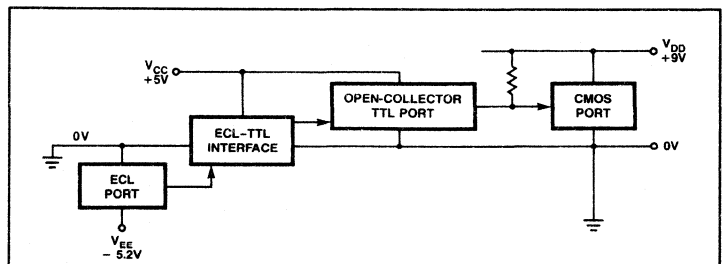


Figure 10.8. ECL/CMOS Interface Passing Through TTL Levels

User's Guide

SINGLE-SUPPLY TTL INTERFACE

In systems in which a single ECL circuit must be added and interfaced to TTL circuits, it is possible to avoid having to provide a special power supply for ECL by using the circuit with TTL power supplies.

The necessary level translation is achieved by a differential stage (consisting of discrete components) in the ECL-to-TTL direction, and by a diode-resistor network in the other direction (see Figure 10.9).

ANALOG ECL INTERFACE

High-speed digital signal-processing applications are becoming more and more common. For these purposes, digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) have been developed whose logic is compatible with ECL levels. The ADC converters are the simultaneous parallel conversion type; some of them allow sampling frequencies greater than 50MHz. DAC converters are simpler, utilizing current-source switching controlled by ECL gates.

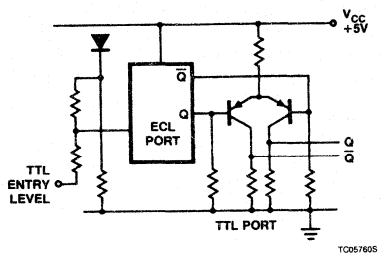


Figure 10.9. Single-Voltage ECL/TTL Interface

Chapter 11
Circuit Boards

ECL Products

THERMAL MANAGEMENT

At the board level, local overheating must be avoided. As a general rule, ECL circuit boards are cooled by moving air.

Overheating can be caused by either of two mechanisms:

1. The temperature of the air flow increases from the time it enters the system until it leaves, and the circuits located near the output risk reaching excessively high temperatures;
2. A component that is taller than the others can screen the flow of air from the other circuits.

Components subjected to overheating suffer a modification of their electrical characteristics. Moreover, their lifetime can be shortened considerably.

The board itself can contribute significantly to the removal of heat from the circuits, if care is taken to place it in close contact (via its edges) with the metallic chassis of the equipment. In some cases, the chassis itself can be cooled by a liquid (water or freon).

BOARD PRECAUTIONS

Generally speaking, the use of sockets is not recommended. On the contrary, circuits should be soldered directly onto the boards. This applies even to prototypes. Doing so avoids problems with oscillations or signal deformations caused by unsuitable connections. When it is absolutely necessary (as in the case of a test board, or of accelerated aging), a connection length less than 6mm should be used.

With regard to accelerated-aging boards (i.e. "burn-in"), it is important that all pins have electrical conditions that reflect normal operation, and that the power supply and environmental conditions respect the maximum junction temperature specified. (Somewhat paradoxically, this means cooling of the burn-in chamber, more often it means heating of the chamber!)

It is recommended that specially-designed burn-in chambers be used for ECL circuits because standard chambers risk insufficient temperature and air-flow control.

The section on interconnections explained why careless or semi-accurate implementation could lead to erratic operation and to reduced immunity to system noise. As an example, the use of wired-OR connections causes variations in the static and dynamic characteristics of the outputs connected between them. Because each output carries a smaller average current, it sees its static voltage levels V_{OH} and V_{OL} increase by several tens of millivolts. With regard to dynamic characteristics, the switching gate sees a line loaded by the outputs of other gates. If these gates are located too far from one another for the signal to reach them before it has completed its transition, then multiple echos will occur and the resulting signal will have undesirable oscillations.

Another necessary precaution concerns unused inputs or outputs. All outputs, even those not used, must be connected to V_T via a load resistor. If this precaution is not taken, then (1) the internal voltage drops of the circuit will be affected, significantly affecting the other outputs, and (2) for circuits with fast edges, having complementary outputs, a break in the load symmetry will cause irregular current "calls" on the auxiliary V_{CC}, possibly causing significant perturbations of the shape and duration of the (waveform) edges of the gate.

It is wise to connect all unused inputs to V_T (if they are in the LOW state). This procedure is a must for some circuits, like line receivers or certain memories, which do not have internal pull-down resistors on all their pins. For inputs that must be kept in the HIGH state, a small auxiliary source (on the order of –0.8V) should be used, formed by a diode and a resistor located between V_{CC} and V_T. These inputs can also be connected to a HIGH output of an unused gate. Some circuit inputs may be connected directly to V_{CC}, but this is not generally the case. Use of this method requires prior consultation with the vendor.

Furthermore, very long lines on the board can capture parasitic signals arising from a local electromagnetic field. It is possible to reduce this interference by interposing lines, or zones, connected to ground between the lines, driving the signals over a given distance.

Care should be taken to implement all ground connections (such as the bottom ends of load resistors or of decoupling capacitors, and the shielding of coaxial cables) by means of a short, wide conductor, to limit parasitic inductances. In fact, any loop, even one that appears small, presents an inductance and can radiate a high-frequency signal.

DEVICE PRECAUTIONS

High-speed components require very small dimensions, which limit the breakdown voltages of the transistors, allowing them to be destroyed by relatively small energies. Therefore, it is very important that the limit values for voltages, currents, and power recommended by the vendor be respected, even when the equipment is turned on and off.

In particular, care should be taken not to apply $V_T = -2V$ to the inputs and outputs before V_{EE} is applied.

Likewise, short-circuiting an output directly to V_{EE} or to V_T should be avoided.

In systems in which other supply voltages are present (e.g., TTL at +5V), care should be taken not to connect the inputs to these voltages. Unfortunately, this is a frequent mishap when boards are tested or when maintenance is performed, through contact with a screwdriver or with the probes of a measurement device.

Section 5
Data Sheet Specification Guide

INDEX

Introduction 67
Features and Description 67
Typical Propagation Delay and Supply Current 67
IEC/IEEE Symbols 67
Absolute Maximum Ratings 67
DC Operating Conditions 67
DC Electrical Characteristics 67
DC Electrical Characteristics 72
Glossary, 10K/100K Symbols, Terms, and Definitions 74

Data Sheet Specification Guide

ECL Products

INTRODUCTION

Signetics' 10K and 100K ECL data sheets have been configured for quick usability. They are self–contained and should require minimum reference to other sections for further information.

FEATURES AND DESCRIPTION

Features and/or Descriptions are shown starting at the top of the first page of the data sheets for quick reference.

TYPICAL PROPAGATION DELAY AND SUPPLY CURRENT

The typical propagation delays listed in the FEATURE of the data sheets are the average between t_{PLH} and t_{PHL} for the most significant data path through the part.

The typical I_{EE} current shown in the same FEATURE is the average current. It represents the total current through the package, not the current through the individual functions.

IEC/IEEE SYMBOLS

The IEC/IEEE symbols found in this handbook are in accordance with the IEC and IEEE standards. The logic symbols are described in

IEEE Standard
Graphic Symbols for Logic Functions
ANSI/IEEE Std 91–1984
(Review of ANSI/IEEE Std 91–1973

which can be ordered through
IEEE Service Center IEEE Service center
445 Hoes Lane
Piscataway, New Jersey 08854
Phone: 201–981–0060

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to all 10K and 100K devices, which should not be exceeded under the worst probable conditions.

These values are chosen by Signetics to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The user should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices.

Absolute maximum ratings imply that any transient voltages, currents, and temperatures should not exceed the maximum ratings.

Input voltage, V_{IN}, should never be more negative than V_{EE} at any time.

Output current should never exceed the maximum value in either High level or Low level state.

Family Specifications for Absolute Maximum Ratings for 10K and 100K families are shown in Tables 1 and 2, respectively.

DC OPERATING CONDITIONS

The DC Operating Conditions table has a dual purpose. In one sense, it sets some environmental conditions (operating case temperature), and in another, it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteristics tables.

10K ECL circuits are characterized with V_{CC1} and V_{CC2} at ground level and V_{EE} at –5.2V. This arrangement gives the best noise immunity. V_{EE} at –5.2 results in the best circuit speed. A more negative V_{EE} will increase noise margins at the expense of increased power consumption. Other values of V_{EE} are possible but DC and AC parameters will differ slightly from the specified values.

100K ECL circuits are characterized with V_{CC1} and V_{CC2} at ground level and V_{EE} at –4.2V, –4.5V, and –4.8V. This arrangement also gives the best noise immunity. Other values of V_{EE} are possible but DC and AC parameters will slightly differ from the specified values.

Family Specifications for DC Operating Conditions for 10K and 100K families are shown in Tables 3 and 4, respectively.

DC ELECTRICAL CHARACTERISTICS

Family Specifications for DC Characteristics for 10K and 100K ECL families are shown in Tables 5 and 6, respectively. However, I_{IH}, I_{IL}, and I_{EE} vary from device to device for 100K ECL families and similarly I_{IH}, I_{IL}, I_{EE}, $\Delta V_{OH}/\Delta V_{EE}$, $\Delta V_{OL}/\Delta V_{EE}$, $\Delta V_{BB}/\Delta V_{EE}$ vary from device to device for 100K ECL families.

It must be emphasized that the specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board.

Make sure that each output is terminated via a 50Ω resistor to –2.0V.

Although it is not recommended to use V_{EE} other than –5.2V, if V_{EE} other than –5.2V is used, changes in V_{OL}, V_{OH}, and V_{BB} level must be taken into consideration.

Although suggested test conditions are described for V_{OH}, V_{OHT}, V_{OL}, and V_{OLT}, refer to Section 3 Testing, DC testing for what to look for in considering output voltages in the worst cases.

The test values for DC Characteristics are defined and given in the Family Specifications for Transfer Characteristics for 10K and 100K ECL families and shown in Figures 1 and 2, respectively.

The conditions for the Transfer Characteristics for the 10K ECL families are T_A = +25°C, V_{EE} = –5.2V, V_{CC1} = V_{CC2} = ground; and 50 ohm matched inputs and outputs.

The conditions for the Transfer Characteristics for the 100K ECL family are T_A = +25°C, V_{EE} = –4.5V, V_{CC1} = V_{CC2} = ground; and 50 ohm matched inputs and outputs.

Data Sheet Specification Guide

TABLE 1. ABSOLUTE MAXIMUM RATINGS FOR THE 10K ECL FAMILY

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage range		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

TABLE 2. ABSOLUTE MAXIMUM RATINGS FOR THE 100K ECL FAMILY

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

TABLE 3. DC OPERATING CONDITIONS FOR THE 10K ECL FAMILY

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

Data Sheet Specification Guide

TABLE 4. DC OPERATING CONDITIONS FOR THE 100K ECL FAMILY

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

Data Sheet Specification Guide

TABLE 5. DC ELECTRICAL CHARACTERISTICS FOR THE 10K FAMILY $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	-1060		-890	mV
			$T_A = +25°C$	-960		-810	mV
			$T_A = +85°C$	-890		-700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	-1080			mV
			$T_A = +25°C$	-980			mV
			$T_A = +85°C$	-910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$			-1655	mV
			$T_A = +25°C$			-1630	mV
			$T_A = +85°C$			-1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	-1890		-1675	mV
			$T_A = +25°C$	-1850		-1650	mV
			$T_A = +85°C$	-1825		-1615	mV
I_{IH}	High level input current		$T_A = -30°C$				µA
			$T_A = +25°C$				µA
			$T_A = +85°C$				µA
			$T_A = -30°C$				µA
			$T_A = +25°C$				µA
			$T_A = +85°C$				µA
I_{IL}	Low level input current		$T_A = -30°C$				µA
			$T_A = +25°C$				µA
			$T_A = +85°C$				µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				mA
			$T_A = +25°C$				mA
			$T_A = +85°C$				mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

Data Sheet Specification Guide

TABLE 6. DC ELECTRICAL CHARACTERISTICS FOR THE 100K FAMILY

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current							µA
I_{IL}	Low level input current							µA
$-I_{EE}$	V_{EE} supply current							mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	V_{EE} = –4.2V, T_A = +25°C					0.025	V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation						0.030	V/V
$\frac{\Delta I_{EE}}{\Delta V_{EE}}$	Power supply current compensation						0.025	V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

Data Sheet Specification Guide

TRANSFER CHARACTERISTICS FOR THE 10K FAMILY

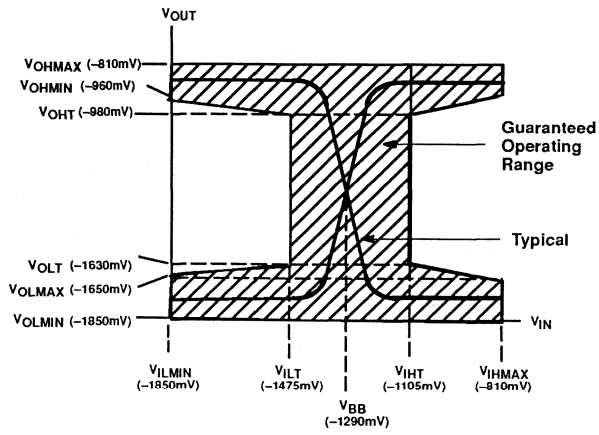


Figure 1

TRANSFER CHARACTERISTICS FOR THE 100K FAMILY

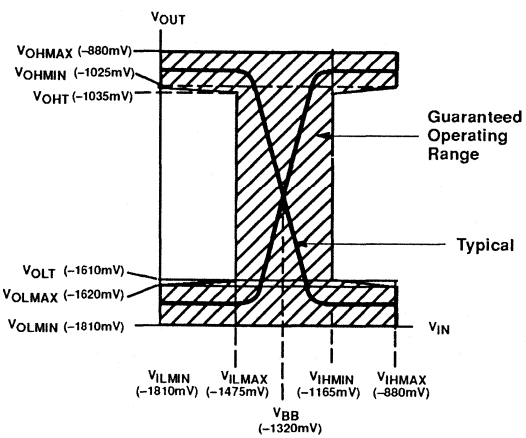


Figure 2

AC ELECTRICAL CHARACTERISTICS

Since AC Characteristics vary from device to device there is no family specifications as such.

It must be emphasized that the specified limits shown in the AC characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. AC characteristics may be tested either in non–offset bias condition or in offset bias condition. For 10K ECL, the non–offset bias condition is $V_{CC1} = V_{CC2} = 0V$ and $V_{EE} = -5.2V \pm 0.010V$ and the offset condition is $V_{CC1} = V_{CC2} = +2V \pm 0.010V$ and $V_{EE} = -3.2V \pm 0.010V$. For 100K ECL, the non–offset bias condition is $V_{CC1} = V_{CC2} = 0V$, and $V_{EE} = -4.8V$ to $-4.2V$ and the offset condition is $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, and $V_{EE} = -2.8V$ to $-2.2V$. The offset bias condition is for a bench–type tester to accommodate the oscilloscope ground configuration. Of course, the specified limits remain the same for the non–offset and the offset condition.

Data Sheet Specification Guide

AC WAVEFORMS

There is no Family Specification for AC Waveforms. Since AC Waveforms vary from device to device, refer to each individual data sheet.

AC TEST CIRCUIT

The AC test circuit shows how to arrange the test circuit for each device with pulse generator, sampling scope, and power supplies. A simplified arrangement for 10K and 100K families is shown in Figure 3. For special cases, refer to each individual data sheet.

Since AC characteristics are difficult to test, a whole section is devoted to Testng including a whole section describing the bench–type testing for AC characterisitics (Refer to Section 3 Testing, Chapter 2 AC Testing).

AC TEST CIRCUIT FOR THE 10K AND THE 100K ECL FAMILIES

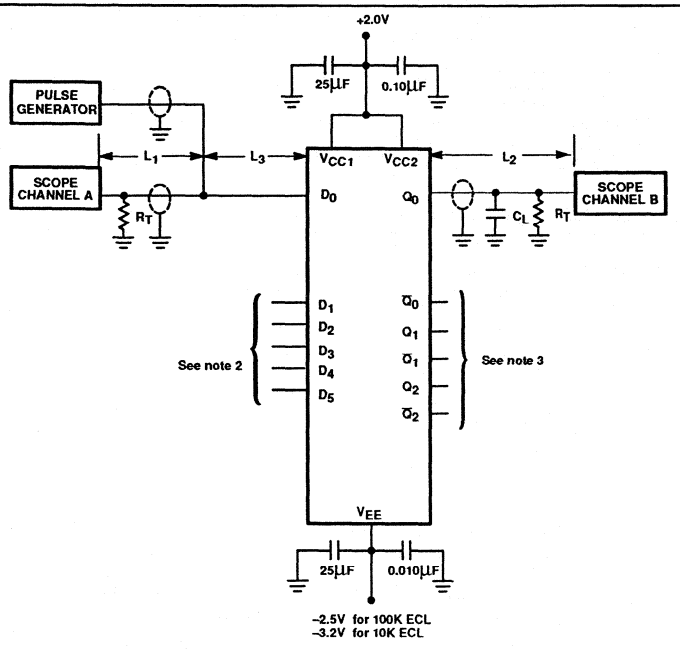


Figure 3

NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

Data Sheet Specification Guide

INPUT PULSE DEFINITION

The Input Pulse definition defines the input pulse requirements such as pulse amplitude, repetition rate, pulse width, and Transition Time (t_{TLH}, t_{THL}) together with the input pulsewaveform. The Family Specification for 10K and 100K for Input Pulse Definition and Requirement is as follows:

INPUT PULSE DEFINITION FOR THE 10K AND THE 100K ECL FAMILIES

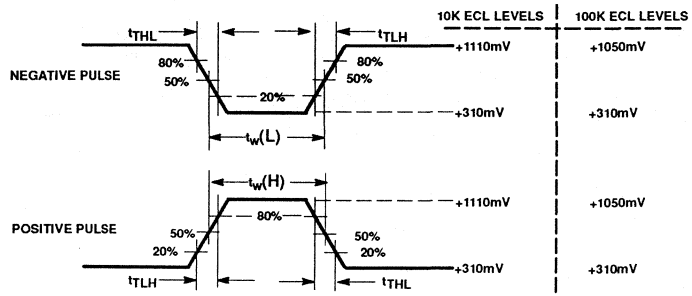


Figure 4. ECL Input Pulse Definition

TABLE 7. INPUT PULSE REQUIREMENTS FOR THE 10K AND THE 100K FAMILIES

INPUT PULSE REQUIREMENTS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T = 0V$ (system ground) for 10K ECL. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.8V$ to $-2.2V$, $V_T = 0V$ (system ground) for 100K ECL.				
FAMILY	**AMPLITUDE**	**REP RATE**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
10K ECL	800 mV_{p-p}	1MHz	500ns	2.0 +0.2ns
100K ECL	740 mV_{p-p}	1MHz	500ns	0.7 +0.1ns

DC SYMBOLS AND DEFINITIONS FOR VOLTAGES

All voltages are referenced to V_{CC} (V_{CC1} and V_{CC2}) which is usually ground (common) and the most positive potential in an ECL system.

SYMBOL	DESCRIPTION
GND	**Ground (Common):** The reference point from which all voltages in the system are measured. In a TTL/ECL or ECL/TTL translator, or other interface circuits, it is the common point to which all other voltage supplies are referenced.
V_{BB}	**Reference Bias voltage:** The internally–generated reference voltage which is used to set the input and output threshold level.
V_{BBMAX}	**Maximum Reference Bias voltage**
V_{BBMIN}	**Minimum Reference Bias voltage**
V_{BIN} (TTL)	**Input breakdown voltage:** Reverse breakdown voltage of the input diodes of a TTL/ECL Translator with 1.0 mA flowing into the input pin.
V_{BE}	**Base to Emitter voltage**
V_{CB}	**Collector to Base voltage**
V_{CC}	**Circuit Ground:** This is the most positive potential in the ECL system and it is used as the reference for other voltages and is usually ground except for the TTL/ECL or ECL/TTL system such as translator and interface circuits.
V_{CC1}	**Circuit Ground:** Usually ground in the ECL system (Output reference).
V_{CC2}	**Circuit Ground:** Usually ground in the ECL system (Internal circuit reference).
V_{CS}	**Current source voltage:** An internally–generated reference potential in an ECL system.
V_{EE}	**Power supply voltage:** This potential is the ECL system power supply voltage and it is the most negative potential in the ECL system.
V_F (TTL)	**Forward voltage:** Input voltage for measuring I_F on TTL/ECL translators.
V_{IH}	**High level input voltage:** An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. A logical "1" (nominal value).
V_{IHMAX}	**Maximum High level input voltage:** The most positive V_{IH}

Data Sheet Specification Guide

DC SYMBOLS AND DEFINITIONS FOR VOLTAGES (Continued)

All voltages are referenced to V_{CC} (V_{CC1} and V_{CC2}) which is usually ground (common) and the most positive potential in an ECL system.

SYMBOL	DESCRIPTION
V_{IHH}	V_{IHMAX} +1.0V (V_{IHMAX} shifted positive one volt for CMR test)
V_{IHL}	V_{IHMAX} –1.0V (V_{IHMAX} shifted negative one volt for CMR test)
V_{IHT}	**High level input threshold voltage:** The guaranteed High level input threshold voltage
V_{IHT}" (TTL)	**Hysteresis Mode High level input threshold voltage:** V_{IHT} for High to Low level transition in Hysteresis mode.
V_{IHT}"' (TTL)	**Hysteresis Mode High level input threshold voltage:** V_{IHT} for Low to High level transition in Hysteresis mode.
V_{IK}	**Input clamp voltage:** The input voltage level across the input clamping diode in a region of relatively low differential resistance that serves to limit the input voltage swing.
V_{IKMAX}	**Maximum input clamp diode voltage:** The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.
V_{IL}	**Low level input voltage:** An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A logical " 0 " (nominal level).
V_{ILT}	**Low level input threshold voltage:** The guaranteed Low level input threshold voltage.
V_{ILT}" (TTL)	**Hysteresis Mode Low level input threshold voltage:** V_{IHT} for High to Low level transition in Hysteresis mode.
V_{ILT}"' (TTL)	**Hysteresis Mode Low level input threshold voltage:** V_{IHT} for Low to High level transition in Hysteresis mode.
V_{ILMIN}	**Minimum Low level input voltage:** The most negative V_{IL}.
V_{ILH}	V_{ILMIN} +1.0V (V_{ILMIN} shifted positive one volt for CMR tests.)
V_{ILL}	V_{ILMIN} –1.0V (V_{ILMIN} shifted negative one volt for CMR tests.)
V_{IN}	**Input Voltage**
V_{NH}	**High level Noise Margin:** Noise margin between the output High level of a driving circuit and the input High threshold level of its driven load. A conservative value for V_{NH} is the difference between V_{OHT} and V_{IHMIN}.
V_{NL}	**Low level Noise Margin:** Noise margin between the output Low level of a driving circuit and the input Low threshold level of its drive load. A conservative value for V_{NL} is the difference between V_{ILMAX} and V_{OLT}.
V_{OH}	**High level output voltage:** The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a High level at the output (nominal output " 1 " state).
V_{OHMAX}	**Maximum High level output voltage:** The most positive V_{OH} under the specified input and loading conditions.
V_{OHMIN}	**Minimum High level output voltage:** The most negative V_{OH} under the specified input and loading condition.
V_{OHT}	**High level output threshold voltage:** The guaranteed High level threshold output voltage with the inputs set to their respective threshold levels, one at a time.
V_{OL}	**Low level output voltage:** The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a Low level at the output (nominal output " 0 " state).
V_{OLMAX}	**Maximum Low level output voltage:** The most positive V_{OL} under the specified input and loading conditions.
V_{OLMIN}	**Minimum Low level output voltage:** The most negative V_{OL} under the specified input and loading conditions.
V_{OLT}	**Low level output threshold voltage:** The guaranteed Low level output threshold voltage with the inputs set to their respective threshold levels, one at a time.
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	**Reference Bias voltage compensation:** The ratio of the change in the High level output voltage to the change in the supply voltage.
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	**High level output voltage compensation:** The ratio of the change in the input reference voltage to the change in the supply voltage.
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	**Low level output voltage compensation:** The ratio of the change in the Low level output voltage to the change in the supply voltage.
V_{OLS1} (TTL)	Low level output voltage on 10K ECL/TTL translator with all inputs at V_{EE} voltage to check indeterminate input level.
V_{OLS2} (TTL)	Low level output voltage on 10K ECL/TTL translator with all inputs open to check indeterminate input level.
V_{OUT}	**Output Voltage**
V_R (TTL)	**Reverse input voltage: Input voltage for measuring I_R on TTL/ECL Translator.**
V_T	**Line load–resistor terminating voltage,** positive or negative.

Data Sheet Specification Guide

DC SYMBOLS AND DEFINITIONS FOR CURRENTS

Positive current is defined as conventional current (Hole) flow into a device. Negative current is defined as conventional current flow out of a device.

SYMBOL	DESCRIPTION
I_{CC}	**Supply current:** The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst–case operations unless specified. Current out of a terminal is given as a negative value.
I_{CBO}	**Input (Collector to Base) leakage current:** Leakage current flowing out of an input on devices without pull–down resistors when test voltage is applied.
I_{CCH} (TTL)	**Supply current, outputs High:** The current into the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the High level. Current out of a terminal is given as a negative value.
I_{CCL} (TTL)	**Supply current, outputs Low:** The current into the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the Low level. Current out of a terminal is given as a negative value.
I_{EE}	**Power supply current:** The current required by each device from the V_{EE} supply. This value represents only the internal current required by the specified device and does not include the current required for loads or termination.
I_F (TTL)	**Input forward current:** The forward conduction current out of the input diode of a TTL/ECL Translator with the input voltage at a Low logic level (V_F).
I_I (TTL)	**Input leakage current:** The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guarantees the minimum breakdown voltage for the input.
I_{IH}	**High level input current:** The current flowing into an input when a specified High level voltage is applied to the input. Current out of the input is given as a negative value.
I_{IHMAX}	**Maximum High level input current:** The most positive I_{IH}.
I_{IHMIN}	**Minimum High level input current:** The most negative I_{IH}.
I_{IL}	**Low level input current:** The current flowing into an input when a Low level input voltage is applied to that input. In ECL devices, this is a measurement of the current flowing into the input pull–down resistor.
I_{ILMAX}	**Maximum Low level input current:** The most positive I_{IL}.
I_{ILMIN}	**Minimum Low level input current:** The most negative I_{IL}.
I_{OH}	**High level output current:** The current into an output with input conditions applied that, according to the product specification, will establish a High level at the output. Current out of the output is given as a negative value.
I_{OHT}	**High level output threshold current:** The guaranteed maximum High level output current of an ECL Bus Driver with current switch mode outputs with the inputs at their respective threshold levels, one at a time.
I_{OL}	**Low level output current:** The current into an output with input conditions applied that, according to the product specification, will establish a Low level at the output. Current out of the output is given as a negative value.
I_{OLT}	**Low level output threshold current:** The guaranteed maximum Low level output current of an ECL Bus Driver with current switch mode outputs with the inputs at their respective threshold levels, one at a time.
I_O	**Output source current (Absolute Maximum Rating):** The maximum current that may flow out of an output without causing permanent damage to the device. This is a function of the external Load Resistance and the Terminating Voltage (V_T) to which it is referenced and logic state of the output (V_{OHMAX} is worst–case).
I_{OS}	**Short circuit output current:** The current out of an output of an ECL/TTL translator when the output is short–circuited to ground with input conditions applied to establish a High state output logic level. Only one output should be shorted to ground at a time.
I_{OZH}	**Off–state output current High:** The leakage current of a disabled 3–state output with a specified High level voltage applied.
I_{OZL}	**Off–state output current Low:** The leakage current of a disabled 3–state output with a specified Low level voltage applied.
I_R (TTL)	**Reverse input current:** Reverse (leakage) current flowing into the input diodes of a TTL/ECL Translator when the input is at a High logic level (V_R).
I_T	**Line Terminating (Load) current**

Data Sheet Specification Guide

AC SYMBOLS AND DEFINITIONS

SYMBOL	DESCRIPTION
f_{MAX}	**Maximum clock frequency:** The maximum input frequency at a clock input for which predictable performance is guaranteed. Above this frequency the device may cease to function. (Specified as a minimum limit.)
t_h	**Hold time:** The time interval during which a signal must be retained at a specified input terminal after an active transition occurs at another specified input terminal. NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operated. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The hold time may have a negative value, in which case the minimum limit defines the longest interval (between the release of the signal and active transition) for which correct operation of the digital circuit is guaranteed.
t_{PD}	**Propagation delay time**
t_{PHL}	**Propagation delay time, High to Low:** The time between the specified reference points on the input and output waveforms with the output changing from the defined High level to the defined Low level.
t_{PHZ}	**Output disable time High:** The time between the specified reference points on the input and output waveforms with the 3–state output changing from the High level to a high impedance state.
t_{PLH}	**Propagation delay time, Low to High:** The time between the specified reference points on the input and output waveforms with the output changing from the defined Low level to the defined High level.
t_{PLZ}	**Output disable time Low:** The time between the specified reference points on the input and output waveforms with the 3–state output changing from the Low level to a high impedance state.
t_{PZH}	**Output enable time High:** The time between the specified reference points on the input and output waveforms with the 3–state output changing from a high impedance state to a High level.
t_{PZL}	**Output enable time Low:** The time between the specified reference points on the input and output waveforms with the 3–state output changing from a high impedance state to a Low level.
t_R	**Release time:** The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the master set or reset must be released (inactive) to ensure valid data is recognized.
t_s	**Setup time:** The time interval prior to an active transition applied to a specified input terminal that a signal at another specified input terminal must be applied in order to achieve the desired operation of the device. NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operated. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the release of the signal and active transition) for which correct operation of the digital circuit is guaranteed.
t_{TLH}	**Transition time, Low to High:** The time between two specified reference points on a waveform, normally 20% and 80% points, that is changing from Low to High.
t_{THL}	**Transition time, High to Low:** The time between two specified reference points on a waveform, normally 80% and 20% points, that is changing from High to Low.
t_w	**Pulse width:** The time between the specified reference points on the leading and trailing edges of a pulse.

Data Sheet Specification Guide

ANALOG SYMBOLS AND DEFINITIONS

SYMBOL	DESCRIPTION
CMR	**Common–Mode Rejection:** Ratio of common–mode voltage to common–mode error voltage where common–mode voltage is defined as the voltage above or below the reference level at each input when both inputs are at the same potential and common–mode error voltage is defined as the resultant error voltage measured at the output.
dBm	Power level relative to 1mW. dBm (Power level) = $10Log_{10}$ (power level in mW/ 1mW).
f_I	**Input frequency**
f_{IMAX}	**Maximum input frequency**
f_{IMIN}	**Minimum input frequency**
SR	**Slew rate:** Maximum rate of change of output voltage for a large step change.
V_{CM}	**Maximum common–mode voltage:** The maximum voltage that can be added to a pair of differential inputs without affecting the output voltage.
V_{DIFF}	**Minimum differential input voltage:** A minimum allowable voltage between differential data inputs such that the output will assume a defined logic level (Low or High).
V_L	**Load voltage**

THERMAL SYMBOLS AND DEFINITIONS

SYMBOL	DESCRIPTION
θ_{JA}	**Thermal resistance, junction to ambient**
θ_{JC}	**Thermal resistance, junction to case**
T_A	**Operating ambient temperature range:** The allowable air temperature range over which the electrical specifications of a device are guaranteed.
T_C	**Case temperature:** Case temperature of an integrated circuit package.
T_J	**Junction temperature (absolute maximum rating):** The absolute maximum allowable temperature at the junction of any P and N type material on the silicon chip. Temperatures exceeding this value will cause a permanent migration of the materials and therefore damage the junction.
T_S	**Storage temperature (absolute maximum rating):** Maximum temperature at which device may be stored without damage or performance degradation.

Section 6
10K Series Data Sheets

ECL Products

INDEX

10100	Quad 2-Input NOR Gate w/ Strobe	81
10101	Quad 2-Input OR/NOR Gate w/ Strobe	85
10102	Quad 2-Input NOR (3 NOR and 1 OR/NOR) Gate	89
10103	Quad 2-Input OR(3 OR and 1 OR/NOR) Gate	93
10104	Quad 2-Input AND Gate	97
10105	Triple 2-3-2 Input OR/NOR Gate	101
10106	Triple 4-3-3 Input NOR Gate	105
10107	Triple 2-Input Exclusive-OR/Exclusive-NOR Gate	109
10108	Dual 4-Input AND/NAND Gate	113
10109	Dual 4-5 Input OR/NOR Gate	118
10110	Dual 3-Input/3-Output OR Gate (Line Driver)	122
10111	Dual 3-Input/3-Output NOR Gate (Line Driver)	126
10113	Quad Exclusive-OR Gate w/ Enable Input	130
10114	Triple Differential Line Receiver	134
10115	Quad Differential Line Receiver	140
10116	Triple Differential Line Receiver	145
10117	Dual 2-Wide 2-3Input OR-AND/OR-AND-INVERT Gate	150
10118	Dual 2-Wide 3-Input OR-AND Gate	155
10119	4-Wide 4-3-3-3 Input OR-AND Gate	159
10121	4-Wide OR-AND/OR-AND-INVERT Gate	164
10123	Triple 4-3-3 Input Bus Driver	169
10124	Quad TTL-to-ECL Translator	175
10125	Quad ECL-to-TTL Translator	181
10129	Quad TTL-to-ECL Translator	188
10130	Dual D-Type Latch	197
10131	Dual D-Type Master-Slave Flip-Flop	203
10132	Dual 2-Input Multiplexer With Clocked D-Type Latches and Common Reset	210
10133	Quad Latch With D-Type Inputs and Enable Outputs	216
10134	Dual 2-Input Multiplexer With Clocked D-Type Latches	222
10135	Dual J-K Master-Slave Flip-Flop	228
10136	Universal Hexadecimal Counter	233
10137	Universal Decade Counter	240
10141	4-Bit Universal Shift Register	247
10158	Quad 2-to-1 Multiplexer, Non-Inverting	252
10159	Quad 2-to-1 Multiplexer, Inverting	256
10160	12-Bit Parity Checker/Generator	260
10161	1-of-8 Decoder With 2 Enable Inputs (Active-Low Outputs)	264
10162	1-of-8 Decoder With 2 Enable Inputs (Active-High Outputs)	268
10164	8-Input Multiplexer With Enable Input	272
10165	8-Input Priority Encoder	276
10171	Dual 1-of-4 Decoder With One Common and Two Individual Inputs (Active-Low Outputs)	281
10172	Dual 1-of-4 Decoder With One Common and Two Individual Inputs (Active-High Outputs)	285
10173	Quad 2-Input Multiplexer With Latched Outputs	289
10174	Dual 4-to-1 Multiplexer (With Output Enable)	294
10175	Quint D-Latch Width Common Reset and 2 Wired-OR Common Clock Inputs	298
10176	Hex D-Type Master-Slave Flip-Flop	303
10179	Carry Look-Ahead Block	307

10180	Dual 2-Bit Adder/Subtractor	311
10181	4-Bit Arithmetic Logic Unit/Function Generator	316
10188	Hex Buffer With Enable (Non-Inverting)	323
10189	Hex Inverter With Enable	327
10192	Quad Bus Driver	331
10210	High-Speed Dual 3-Input/3-Output OR Line Driver	336
10211	High-Speed Dual 3-Input/3-Output NOR Line Driver	340
10216	Triple Differential OR/NOR Line Receiver (High-Speed)	344
10231	Dual D-Type Master-Slave Flip-Flop (High-Speed)	349

Document No.	853–0636
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10100
Gate

Quad 2-Input NOR Gate with Strobe

FEATURES

- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 21mA**

DESCRIPTION

The 10100 is a Quad 2-Input NOR Gate with another input common to all gates. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

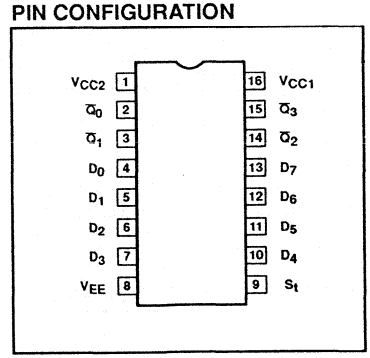
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10100N
16–Pin Ceramic DIP	10100F

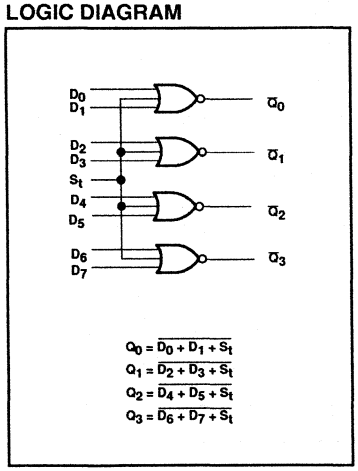
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
S_t	True Data Inputs (OR)
$\overline{Q}_0 - \overline{Q}_3$	Complementary Data Outputs (NOR)

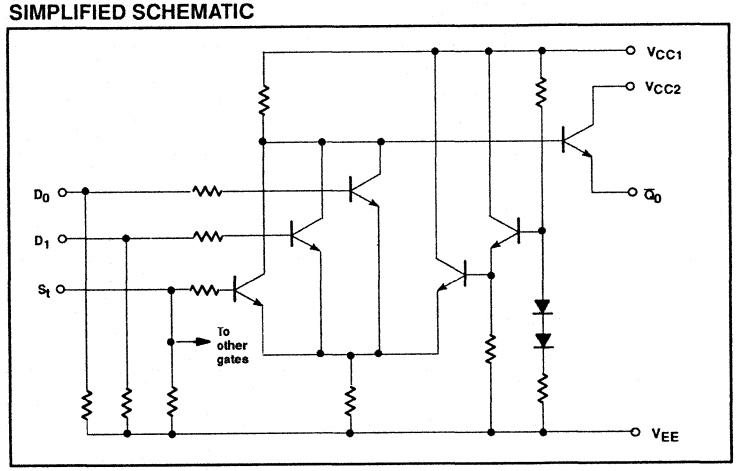
PIN CONFIGURATION



LOGIC DIAGRAM



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{ILMIN} to all inputs.	–1060		–890	mV
			$T_A = +25°C$		–960		–810	mV
			$T_A = +85°C$		–890		–700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	Apply V_{ILT} to S_T input with V_{ILMIN}	–1080			mV
			$T_A = +25°C$	applied to all other inputs.	–980			mV
			$T_A = +85°C$		–910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	Apply V_{IHT} to each input, one at a time,			–1655	mV
			$T_A = +25°C$	with V_{ILMIN} applied to all other inputs.			–1630	mV
			$T_A = +85°C$				–1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	Apply V_{ILMAX} to all inputs.	–1890		–1675	mV
			$T_A = +25°C$		–1850		–1650	mV
			$T_A = +85°C$		–1825		–1615	mV
I_{IH}	High level input current	D_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			390	µA
			$T_A = +25°C$	one at a time, with V_{ILMIN} applied to all			245	µA
			$T_A = +85°C$	other inputs.			245	µA
		S_T inputs	$T_A = -30°C$	Apply V_{IHMAX} to S_T input with V_{ILMIN}			750	µA
			$T_A = +25°C$	applied to all other inputs.			470	µA
			$T_A = +85°C$				470	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{IHMIN} to each input under test,	0.5			µA
			$T_A = +25°C$	one at a time, with V_{ILMAX} applied to all	0.5			µA
			$T_A = +85°C$	other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				29	mA
			$T_A = +25°C$			21	26	mA
			$T_A = +85°C$				29	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

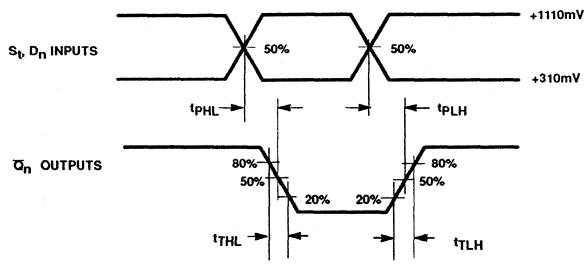
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay S_t, D_n to $\overline{Q}_n$	Waveform 1	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.10 1.10	3.60 3.60	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transitions Times

Document No.	853–0637
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10101
Gate

Quad 2-Input OR/NOR Gate with Strobe

FEATURES

- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 20mA**

DESCRIPTION

The 10101 is a Quad 2-Input OR/NOR Gate with one input from each gate common to Pin 12. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

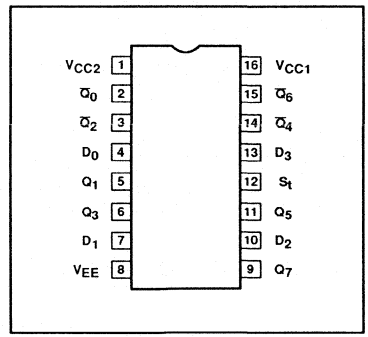
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10101N
16–Pin Ceramic DIP	10101F

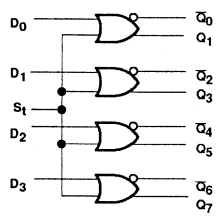
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
S_t	Strobe Input
Q_n, $\overline{Q}_n$	Data Outputs (OR/NOR)

PIN CONFIGURATION

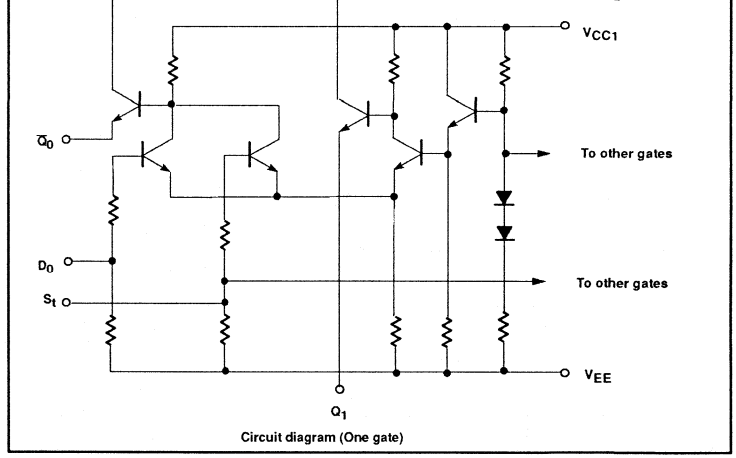


LOGIC DIAGRAM



$Q_0 = \overline{D_0 + S_t}$
$Q_1 = \overline{D_0 + S_t}$
$Q_2 = \overline{D_1 + S_t}$
$Q_3 = \overline{D_1 + S_t}$
$Q_4 = \overline{D_2 + S_t}$
$Q_5 = \overline{D_2 + S_t}$
$Q_6 = \overline{D_3 + S_t}$
$Q_7 = \overline{D_3 + S_t}$

SIMPLIFIED SCHEMATIC



Circuit diagram (One gate)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.E	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to	−1060		−890	mV
			$T_A = +25°C$	all inputs. For $\overline{Q}_n$ outputs, apply	−960		−810	mV
			$T_A = +85°C$	V_{ILMIN} to all inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to S_t input and	−1080			mV
			$T_A = +25°C$	V_{ILMIN} to all other inputs. For $\overline{Q}_n$ outputs, apply V_{ILT} to S_t input and V_{ILMIN}	−980			mV
			$T_A = +85°C$	to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to S_t input and			−1655	mV
			$T_A = +25°C$	V_{ILMIN} to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to S_t input and V_{ILMIN}			−1630	mV
			$T_A = +85°C$	to all other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to	−1890		−1675	mV
			$T_A = +25°C$	all inputs. For $\overline{Q}_n$ outputs, apply	−1850		−1650	mV
			$T_A = +85°C$	V_{IHMAX} to all inputs.	−1825		−1615	mV
I_{IH}	High level input current	D_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			425	µA
			$T_A = +25°C$	one at a time, with V_{ILMIN} applied			265	µA
			$T_A = +85°C$	to all other inputs.			265	µA
		S_t inputs	$T_A = -30°C$	Apply V_{IHMAX} to S_t input with V_{ILMIN}			850	µA
			$T_A = +25°C$	applied to all other inputs.			535	µA
			$T_A = +85°C$				535	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under test,	0.5			µA
			$T_A = +25°C$	one at a time, with V_{IHMAX} applied	0.5			µA
			$T_A = +85°C$	to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				29	mA
			$T_A = +25°C$			20	26	mA
			$T_A = +85°C$				29	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

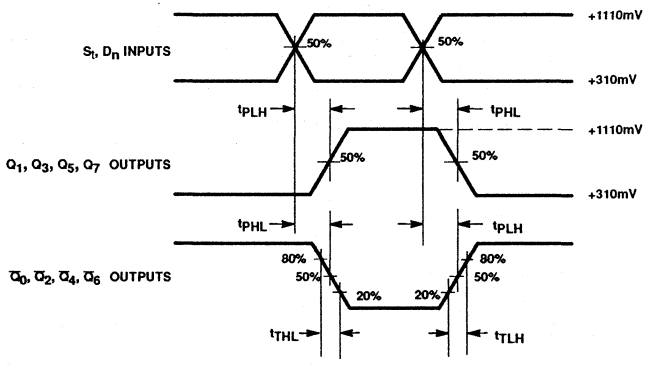
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay S_t, D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.10 1.10	3.60 3.60	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0638
ECN No.	82177
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10102
Gate

Quad 2-Input NOR (2 NOR and 1 OR/NOR) Gate

FEATURES

- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 20mA**

DESCRIPTION

The 10102 is a Quad 2-Input NOR gate. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

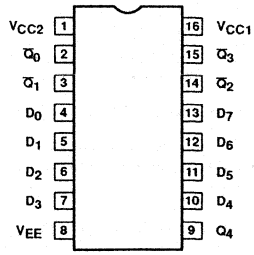
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10102N
16–Pin Ceramic DIP	10102F
16–Pin SO	10102D

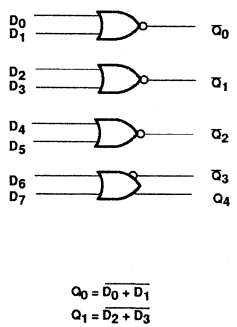
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
Q_4	Data Output (OR)
$\overline{Q}_0 - \overline{Q}_3$	Data Outputs (NOR)

PIN CONFIGURATION

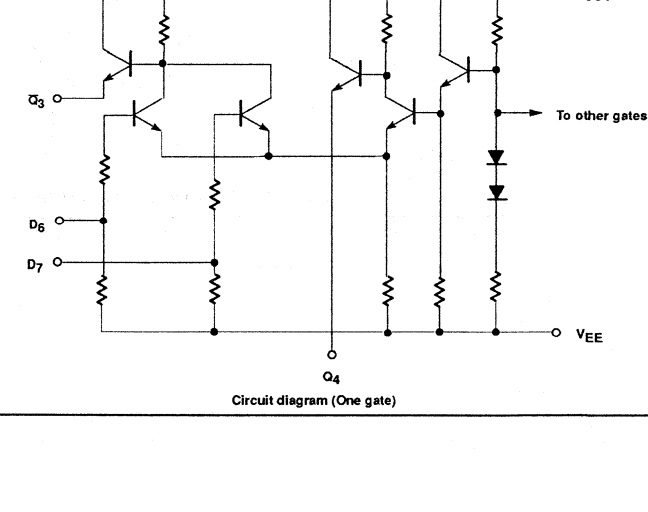


LOGIC DIAGRAM



$Q_0 = \overline{D_0 + D_1}$
$Q_1 = \overline{D_2 + D_3}$
$Q_2 = \overline{D_4 + D_5}$
$Q_3 = \overline{D_6 + D_7}$

SIMPLIFIED SCHEMATIC



Circuit diagram (One gate)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{ILMIN} to	–1060		–890	mV
		$T_A = +25°C$	all inputs. For Q_4 output, apply	–960		–810	mV
		$T_A = +85°C$	V_{IHMAX} to all inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{ILT} to one gate input	–1080			mV
		$T_A = +25°C$	with V_{ILMIN} applied to the other gate input. For Q_4 outputs, apply V_{IHT} to one gate input	–980			mV
		$T_A = +85°C$	with V_{ILMIN} applied to the other gate input.	–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{IHT} to one gate input			–1655	mV
		$T_A = +25°C$	with V_{ILMIN} applied to the other gate input. For Q_4 output, apply V_{ILT} to one gate input			–1630	mV
		$T_A = +85°C$	with V_{ILMIN} applied to the other gate input.			–1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{IHMAX} to	–1890		–1675	mV
		$T_A = +25°C$	all inputs. For Q_4 output, apply	–1850		–1650	mV
		$T_A = +85°C$	V_{ILMIN} to all inputs.	–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			425	µA
		$T_A = +25°C$	one at a time, with V_{ILMIN} applied to			265	µA
		$T_A = +85°C$	all other inputs.			265	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under test,	0.5			µA
		$T_A = +25°C$	one at a time, with V_{IHMAX} applied to	0.5			µA
		$T_A = +85°C$	all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				29	mA
		$T_A = +25°C$			20	26	mA
		$T_A = +85°C$				29	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

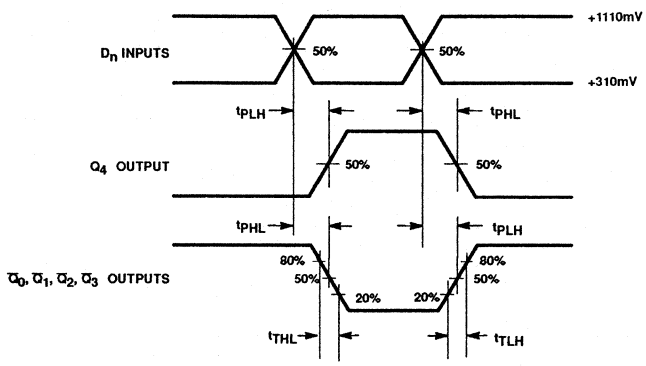
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$, Q_4	Waveform 1	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.10 1.10	3.60 3.60	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Philips Components

Document No.	853–0639
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10103
Gate

Quad 2-Input OR (3 OR and 1 OR/NOR) Gate

FEATURES

- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 21mA**

DESCRIPTION

The 10103 is a Quad 2-Input 3 OR and 1 OR/NOR gate. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

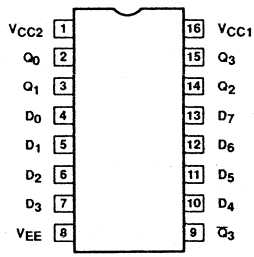
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10103N
16–Pin Ceramic DIP	10103F

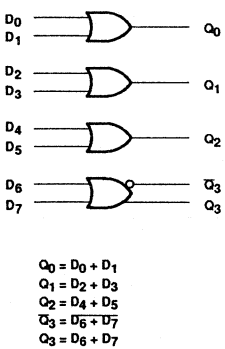
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
$Q_0 - Q_3$	Data Outputs (OR)
$\overline{Q}_3$	Data Output (NOR)

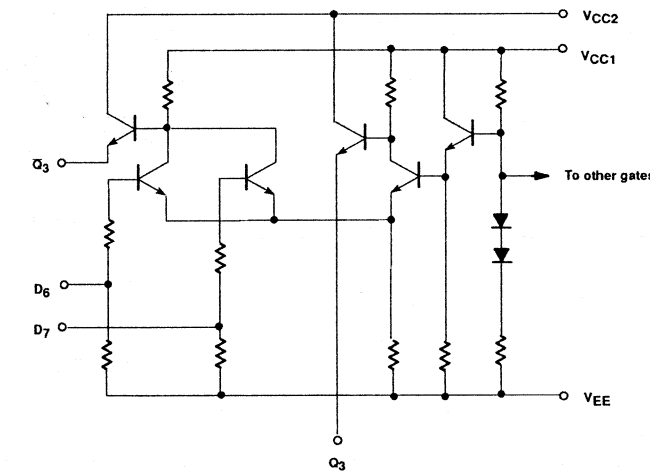
PIN CONFIGURATION



LOGIC DIAGRAM



SIMPLIFIED SCHEMATIC



Circuit diagram (One gate)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to	–1060		–890	mV
		$T_A = +25°C$	all inputs. For $\overline{Q}_3$ output, apply	–960		–810	mV
		$T_A = +85°C$	V_{ILMIN} to all inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to one gate input	–1080			mV
		$T_A = +25°C$	with V_{ILMIN} applied to the other gate inupt. For $\overline{Q}_3$ output, apply V_{ILT} to one gate input	–980			mV
		$T_A = +85°C$	with V_{ILMIN} applied to the other gate input.	–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to one gate input			–1655	mV
		$T_A = +25°C$	with V_{ILMIN} applied to the other gate input. For $\overline{Q}_3$ output, apply V_{IHT} to one gate input			–1630	mV
		$T_A = +85°C$	with V_{ILMIN} applied to the other gate input.			–1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to	–1890		–1675	mV
		$T_A = +25°C$	all inputs. For $\overline{Q}_3$ output, apply	–1850		–1650	mV
		$T_A = +85°C$	V_{IHMAX} to all inputs.	–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			390	µA
		$T_A = +25°C$	one at a time, with V_{ILMIN} applied			245	µA
		$T_A = +85°C$	to all other inputs.			245	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under test,	0.5			µA
		$T_A = +25°C$	one at a time, with V_{IHMAX} applied	0.5			µA
		$T_A = +85°C$	to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				29	mA
		$T_A = +25°C$			21	26	mA
		$T_A = +85°C$				29	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

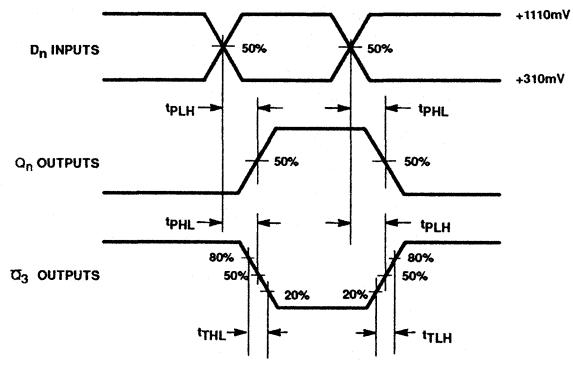
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_3$	Waveform 1	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.10 1.10	3.60 3.60	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0640
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10104
Gate

Quad 2-Input AND Gate

FEATURES

- **Typical propagation delay: 2.7ns**
- **Typical supply current ($-I_{EE}$): 20mA**

DESCRIPTION

The 10104 is a high-speed logic, low power, AND function.

All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

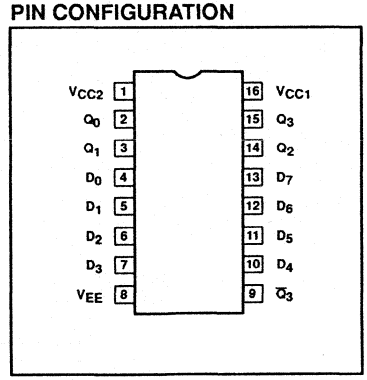
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic DIP	10104N
16-Pin Ceramic DIP	10104F
16-Pin SO	10104D

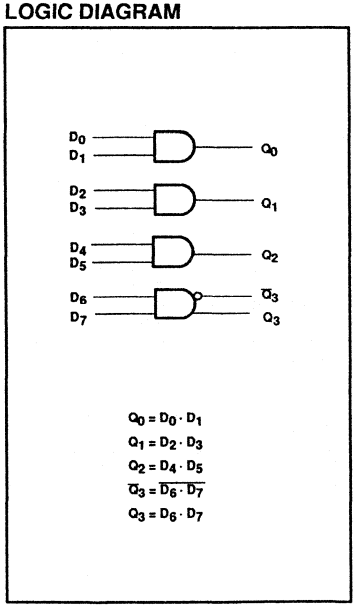
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
$Q_0 - Q_3$	Data Outputs (AND)
$\overline{Q}_3$	Data Output (NAND)

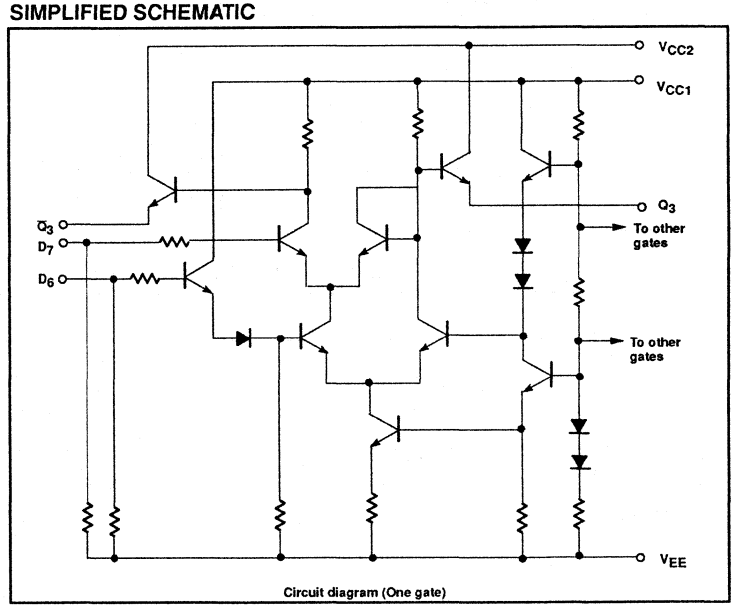
PIN CONFIGURATION



LOGIC DIAGRAM



SIMPLIFIED SCHEMATIC



Circuit diagram (One gate)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to	−1060		−890	mV
			$T_A = +25°C$	all inputs. For $\overline{Q}_3$ output, apply	−960		−810	mV
			$T_A = +85°C$	V_{ILMIN} to all inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to one gate input	−1080			mV
			$T_A = +25°C$	with V_{IHMAX} applied to the other gate input. For $\overline{Q}_3$ output, apply V_{ILT} to one gate input	−980			mV
			$T_A = +85°C$	with V_{IHMAX} applied to the other gate input.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to one gate input			−1655	mV
			$T_A = +25°C$	with V_{IHMAX} applied to the other gate input. For $\overline{Q}_3$ output, apply V_{IHT} to one gate input			−1630	mV
			$T_A = +85°C$	with V_{IHMAX} applied to the other gate input.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to	−1890		−1675	mV
			$T_A = +25°C$	all inputs. For $\overline{Q}_3$ output, apply	−1850		−1650	mV
			$T_A = +85°C$	V_{IHMAX} to all inputs.	−1825		−1615	mV
I_{IH}	High level input current	D_0, D_3 inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			425	µA
		D_4, D_7 inputs	$T_A = +25°C$	one at a time, with V_{ILMIN} applied			265	µA
			$T_A = +85°C$	to all other inputs.			265	µA
		D_1, D_2 inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			350	µA
		D_5, D_6 inputs	$T_A = +25°C$	one at a time, with V_{ILMIN} applied			220	µA
			$T_A = +85°C$	to all other inputs.			220	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under test,	0.5			µA
			$T_A = +25°C$	one at a time, with V_{IHMAX} applied	0.5			µA
			$T_A = +85°C$	to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				39	mA
			$T_A = +25°C$			20	35	mA
			$T_A = +85°C$				39	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

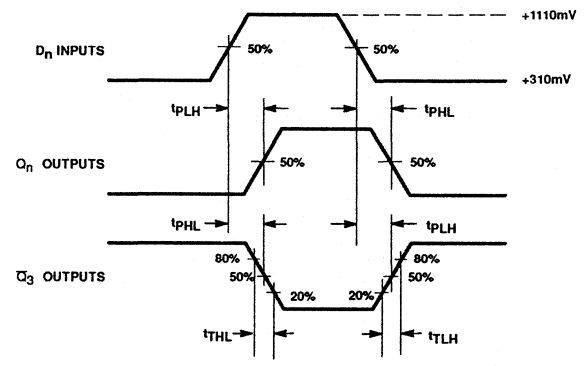
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_3$	Waveform 1	1.00 1.00	4.30 4.30	1.00 1.00	2.70 2.70	4.00 4.00	1.00 1.00	4.20 4.20	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.50 1.50	3.70 3.70	1.50 1.50	2.00 2.00	3.50 3.50	1.50 1.50	3.60 3.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0641
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10105
Gate

Triple 2-3-2 Input OR/NOR Gate

FEATURES

- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 17mA**

DESCRIPTION

The 10105 is a Triple 2-3-2 Input OR/NOR Gate.

All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

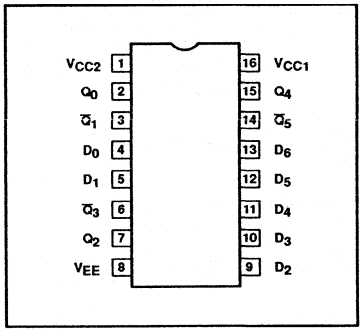
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10105N
16–Pin Ceramic DIP	10105F

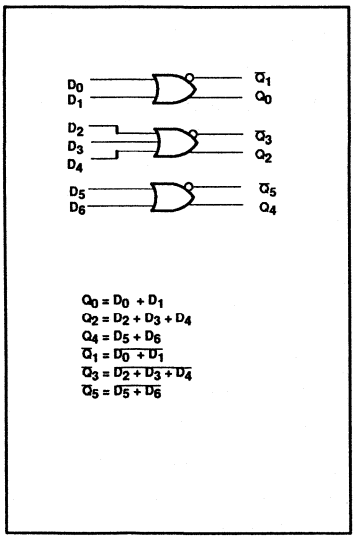
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_6$	Data Inputs
Q_0, Q_2, Q_4	Data Outputs (OR)
$\overline{Q}_1$, $\overline{Q}_3$, $\overline{Q}_5$	Data Outputs (NOR)

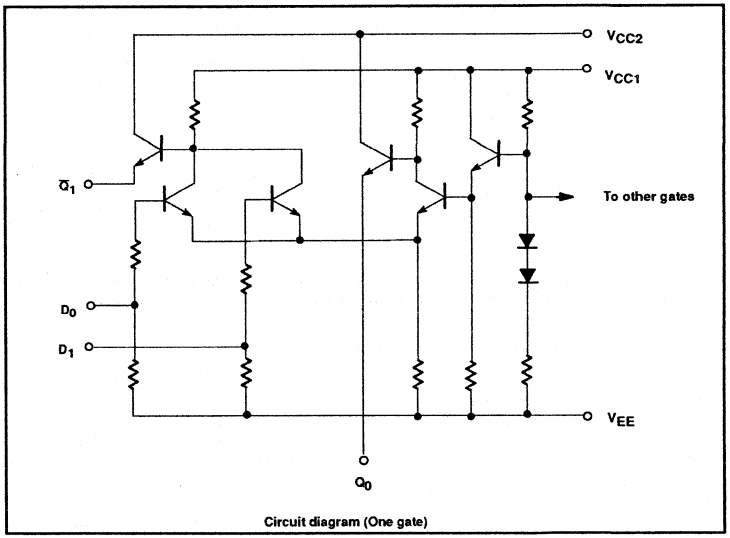
PIN CONFIGURATION



LOGIC DIAGRAM



SIMPLIFIED SCHEMATIC



Circuit diagram (One gate)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to	–1060		–890	mV
		$T_A = +25°C$	all inputs. For $\overline{Q}_n$ outputs, apply	–960		–810	mV
		$T_A = +85°C$	V_{ILMIN} to all inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to each input,	–1080			mV
		$T_A = +25°C$	one at a time, w/ V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{ILT} to each	–980			mV
		$T_A = +85°C$	input w/ V_{ILMIN} applied to all other inputs.	–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to each input,			–1655	mV
		$T_A = +25°C$	one at a time, w/ V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to each			–1630	mV
		$T_A = +85°C$	input w/ V_{ILMIN} applied to all other inputs.			–1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to	–1890		–1675	mV
		$T_A = +25°C$	all inputs. For $\overline{Q}_n$ outputs, apply	–1850		–1650	mV
		$T_A = +85°C$	V_{IHMAX} to all inputs.	–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			425	µA
		$T_A = +25°C$	one at a time, with V_{ILMIN} applied			265	µA
		$T_A = +85°C$	to all other inputs.			265	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under test,	0.5			µA
		$T_A = +25°C$	one at a time, with V_{IHMAX} applied	0.5			µA
		$T_A = +85°C$	to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				23	mA
		$T_A = +25°C$			17	21	mA
		$T_A = +85°C$				23	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

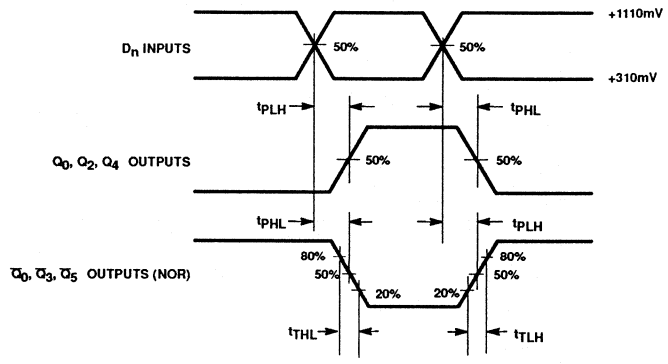
Gate | 10105

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.10 1.10	3.60 3.60	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853-0642
ECN No	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10106
Gate

Triple 4-3-3 Input NOR Gate

FEATURES

- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 17mA**

DESCRIPTION

The 10106 is a Triple 4-3-3 Input NOR Gate. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

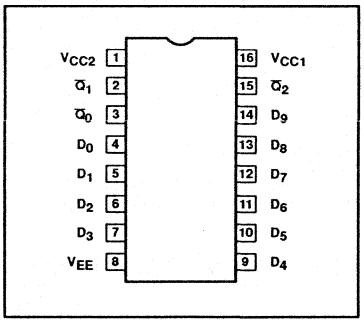
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10106N
16–Pin Ceramic DIP	10106F

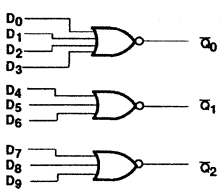
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_9$	Data Inputs
$\overline{Q}_0 - \overline{Q}_2$	Data Outputs

PIN CONFIGURATION

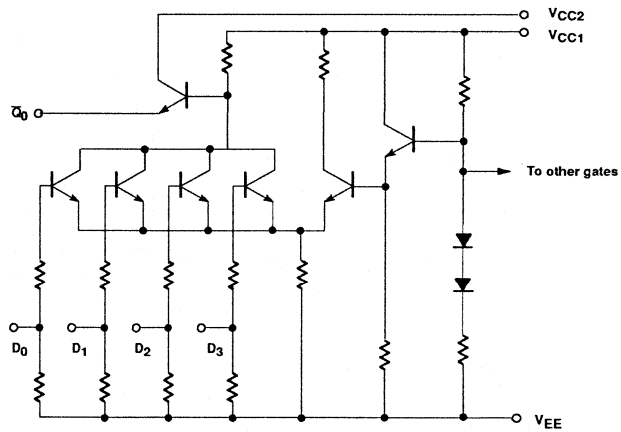


LOGIC DIAGRAM



$Q_0 = \overline{D_0 + D_1 + D_2 + D_3}$
$Q_1 = \overline{D_4 + D_5 + D_6}$
$Q_2 = \overline{D_7 + D_8 + D_9}$

SIMPLIFIED SCHEMATIC



Cicuit diagram (one gate)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Nom	Max	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Apply V_{ILMIN} to all inputs.	–1060		–890	mV
		$T_A = +25°C$		–960		–810	mV
		$T_A = +85°C$		–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{ILT} to each input,	–1080			mV
		$T_A = +25°C$	one at a time, with V_{ILMIN}	–980			mV
		$T_A = +85°C$	applied to all other inputs.	–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Apply V_{IHT} to each input,			–1655	mV
		$T_A = +25°C$	one at a time, with V_{ILMIN}			–1630	mV
		$T_A = +85°C$	applied to all other inputs.			–1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to all inputs.	–1890		–1675	mV
		$T_A = +25°C$		–1850		–1650	mV
		$T_A = +85°C$		–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under			425	µA
		$T_A = +25°C$	test, one at a time, with V_{ILMIN}			265	µA
		$T_A = +85°C$	applied to all other inputs.			265	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
		$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
		$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				23	mA
		$T_A = +25°C$			17	21	mA
		$T_A = +85°C$				23	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

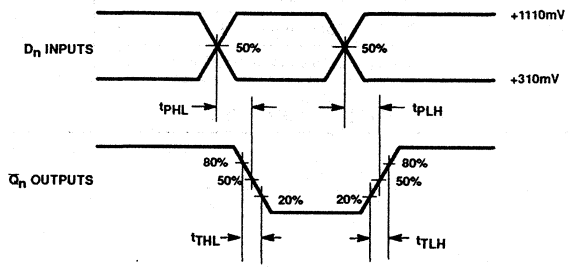
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 1	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.10 1.10	3.60 3.60	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0643
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10107
Gate

Triple 2-Input Exclusive-OR/Exclusive-NOR Gate

FEATURES

- **Typical propagation delay: 2.8ns**
- **Typical supply current ($-I_{EE}$): 22mA**

DESCRIPTION

The 10107 is a three gate array designed to provide the positive Exclusive-OR and NOR functions. All unused inputs can be left open due to pull-down resistors which avoid the need for a supply voltage.

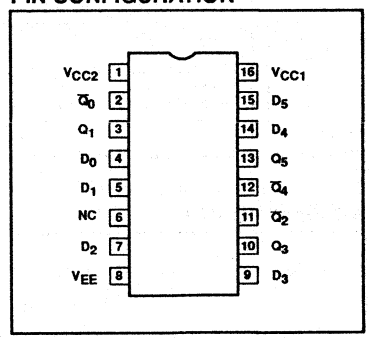
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10107N
16–Pin Ceramic DIP	10107F
16–Pin SO	10107D

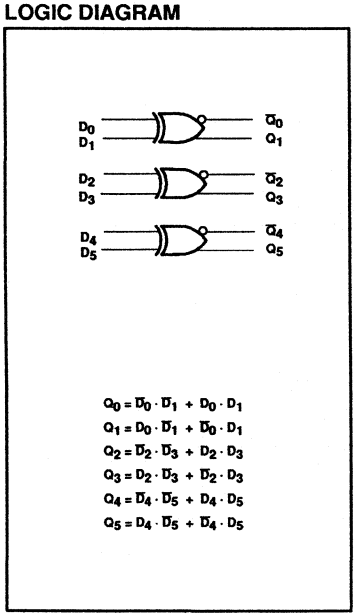
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
Q_1, Q_3, Q_5	Data Outputs (OR)
$\overline{Q}_0, \overline{Q}_2, \overline{Q}_4$	Data Outputs (NOR)

PIN CONFIGURATION

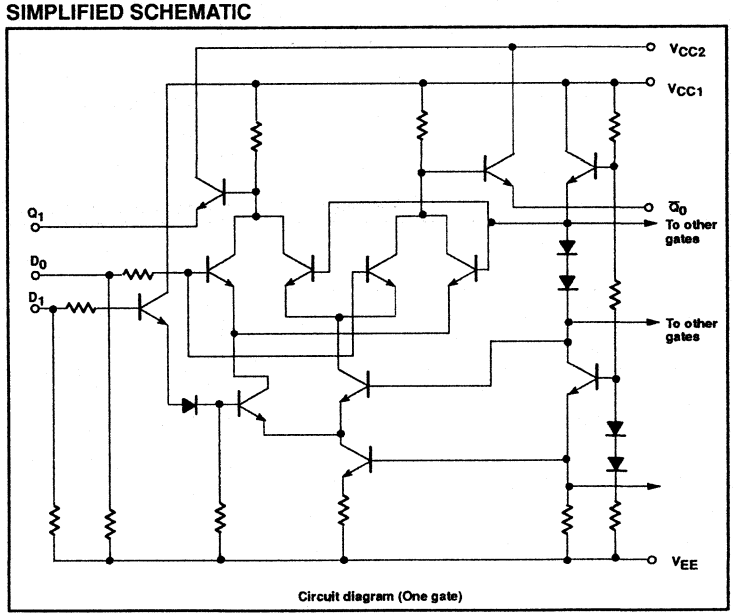


LOGIC DIAGRAM



$Q_0 = \overline{D}_0 \cdot \overline{D}_1 + D_0 \cdot D_1$
$Q_1 = D_0 \cdot \overline{D}_1 + \overline{D}_0 \cdot D_1$
$Q_2 = \overline{D}_2 \cdot \overline{D}_3 + D_2 \cdot D_3$
$Q_3 = D_2 \cdot \overline{D}_3 + \overline{D}_2 \cdot D_3$
$Q_4 = \overline{D}_4 \cdot \overline{D}_5 + D_4 \cdot D_5$
$Q_5 = D_4 \cdot \overline{D}_5 + \overline{D}_4 \cdot D_5$

SIMPLIFIED SCHEMATIC



Circuit diagram (One gate)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{ILMIN} to all inputs. For Q_n outputs, apply V_{IHMAX} to each input (D_1, D_2, D_5),	-1060		-890	mV
			$T_A = +25°C$	one at a time, w/ V_{ILMIN} applied to all other inputs. For Q_n outputs apply V_{IHMAX} to each input	-960		-810	mV
			$T_A = +85°C$	(D_0, D_3, D_4), one at a time, w/ V_{ILMIN} applied to all inputs. For $\overline{Q}_n$ outputs, apply V_{IHMAX} to all inputs.	-890		-700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to one gate input	-1080			mV
			$T_A = +25°C$	with V_{ILMIN} applied to the other gate input. For $\overline{Q}_n$ outputs, apply V_{IHT} to one gate input	-980			mV
			$T_A = +85°C$	with V_{ILMAX} applied to the other gate input.	-910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to one gate input			-1655	mV
			$T_A = +25°C$	with V_{ILMIN} applied to the other gate input. For $\overline{Q}_n$ outputs, apply V_{IHT} to one gate input			-1630	mV
			$T_A = +85°C$	with V_{ILMIN} applied to the other gate input.			-1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{ILMIN} to all inputs. For $\overline{Q}_n$ outputs, apply V_{IHMAX} to each input (D_1, D_2, D_5),	-1890		-1675	mV
			$T_A = +25°C$	one at a time, w/ V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs apply V_{IHMAX} to each input	-1850		-1650	mV
			$T_A = +85°C$	(D_0, D_3, D_4), one at a time, w/ V_{ILMIN} applied to all inputs. For Q_n outputs, apply V_{IHMAX} to all inputs.	-1825		-1615	mV
I_{IH}	High level input current	D_0, D_3, D_4 inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			425	µA
			$T_A = +25°C$	one at a time, with			265	µA
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			265	µA
		D_1, D_2, D_5 inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			350	µA
			$T_A = +25°C$	one at a time, with			220	µA
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			220	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with	0.5			µA
			$T_A = +85°C$	V_{IHMAX} applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$	Apply V_{IHMAX} to D_1, D_2, D_5			31	mA
			$T_A = +25°C$				28	mA
			$T_A = +85°C$				31	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

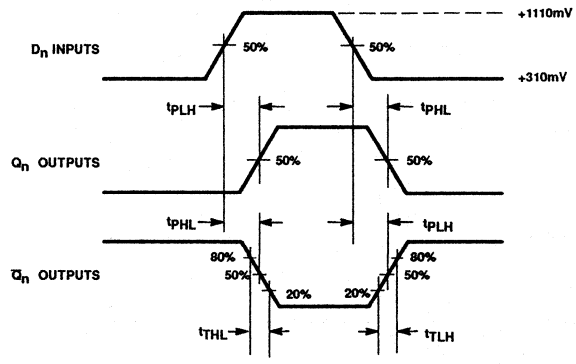
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.10 1.10	3.80 3.80	1.10 1.10	2.80 2.80	3.70 3.70	1.10 1.10	4.00 4.00	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.10 1.10	3.50 3.50	1.10 1.10	2.50 2.50	3.50 3.50	1.10 1.10	3.80 3.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0644
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10108
Gate

Dual 4-Input AND/NAND Gate

FEATURES

- **Typical propagation delay: 2.3ns for AND output, 2.8ns for NAND output**
- **Typical supply current ($-I_{EE}$): 28mA**

DESCRIPTION

The 10108 is a Dual AND/NAND Gate. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

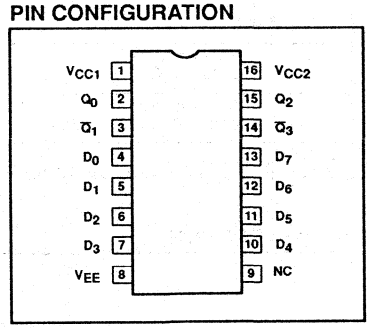
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10108N
16–Pin Ceramic DIP	10108F

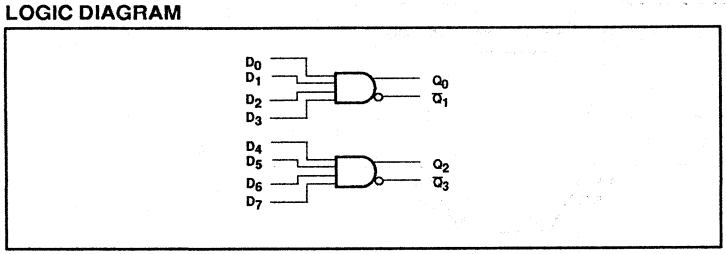
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
Q_0, Q_2	Data Outputs (AND)
$\overline{Q}_1$, $\overline{Q}_3$	Data Outputs (NAND)

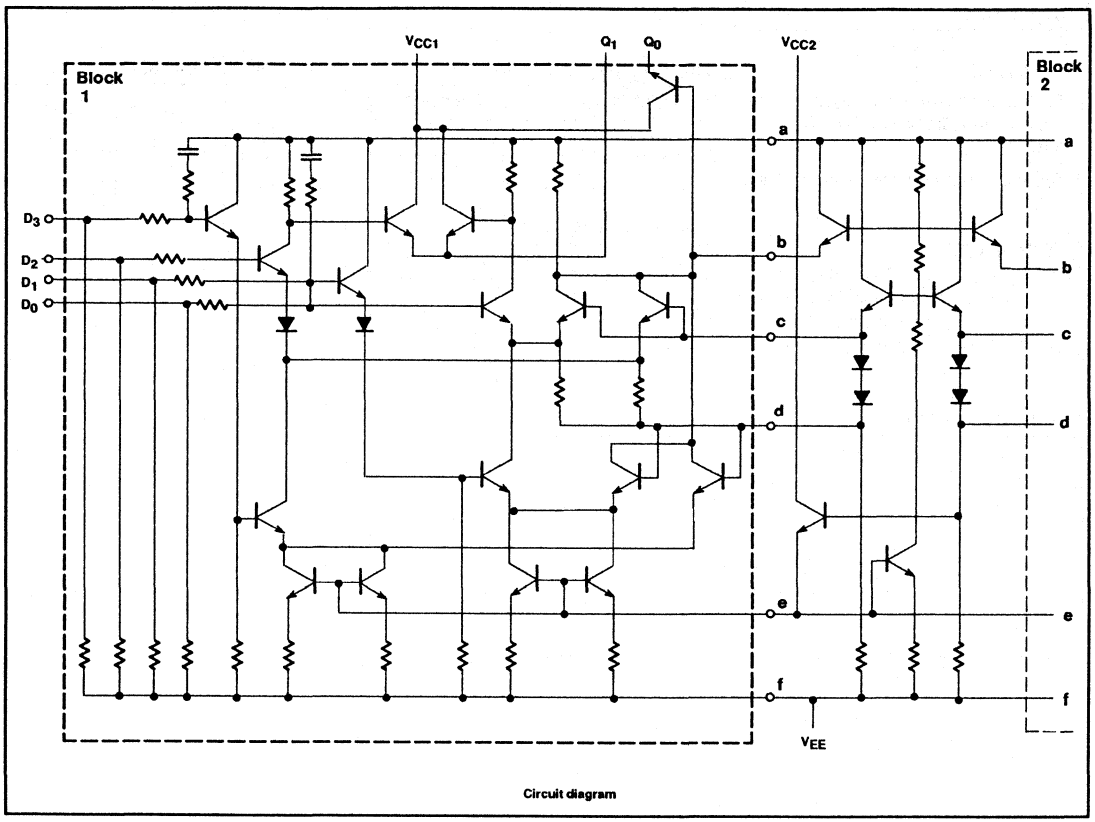
PIN CONFIGURATION



LOGIC DIAGRAM



SIMPLIFIED SCHEMATIC



Circuit diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to	–1060		–890	mV
		$T_A = +25°C$	all inputs. For $\overline{Q}_n$ outputs, apply	–960		–810	mV
		$T_A = +85°C$	V_{ILMIN} to all inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to each input,	–1080			mV
		$T_A = +25°C$	one at a time, w/ V_{IHMAX} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{ILT} to each	–980			mV
		$T_A = +85°C$	input w/ V_{IHMAX} applied to all other inputs.	–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to each input,			–1655	mV
		$T_A = +25°C$	one at a time, w/ V_{IHMAX} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to each			–1630	mV
		$T_A = +85°C$	input w/ V_{IHMAX} applied to all other inputs.			–1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to	–1890		–1675	mV
		$T_A = +25°C$	all inputs. For $\overline{Q}_n$ outputs, apply	–1850		–1650	mV
		$T_A = +85°C$	V_{IHMAX} to all inputs.	–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under			425	µA
		$T_A = +25°C$	test, one at a time, with V_{ILMIN}			265	µA
		$T_A = +85°C$	applied to all other inputs.			265	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
		$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
		$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				40	mA
		$T_A = +25°C$			28	36	mA
		$T_A = +85°C$				40	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

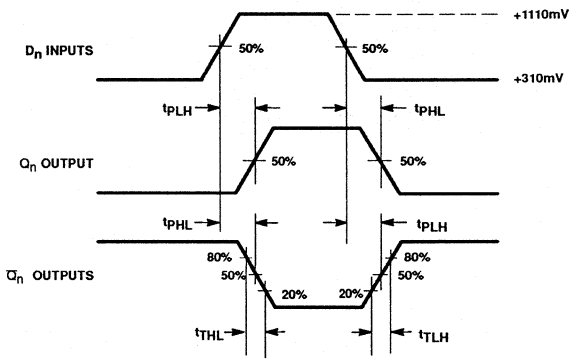
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.40 1.40	4.10 4.10	1.40 1.40	2.30 2.30	3.70 3.70	1.40 1.40	4.10 4.10	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.10 1.10	4.50 4.50	1.10 1.10	2.80 2.80	4.00 4.00	1.10 1.10	4.50 4.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0645
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10109
Gate

Dual 4-5 Input OR/NOR Gate

FEATURES

- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 11mA**

DESCRIPTION

The 10109 is a Dual 4-5 Input OR/NOR Gate. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

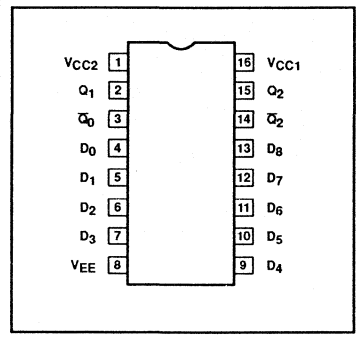
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10109N
16–Pin Ceramic DIP	10109F

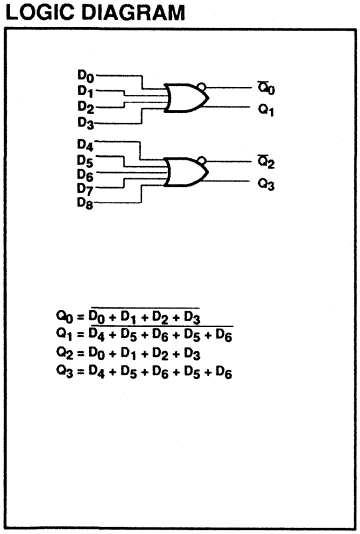
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_8$	Data Inputs
Q_1, Q_3	Data Outputs (OR)
$\overline{Q}_0$, $\overline{Q}_2$	Data Outputs (NOR)

PIN CONFIGURATION

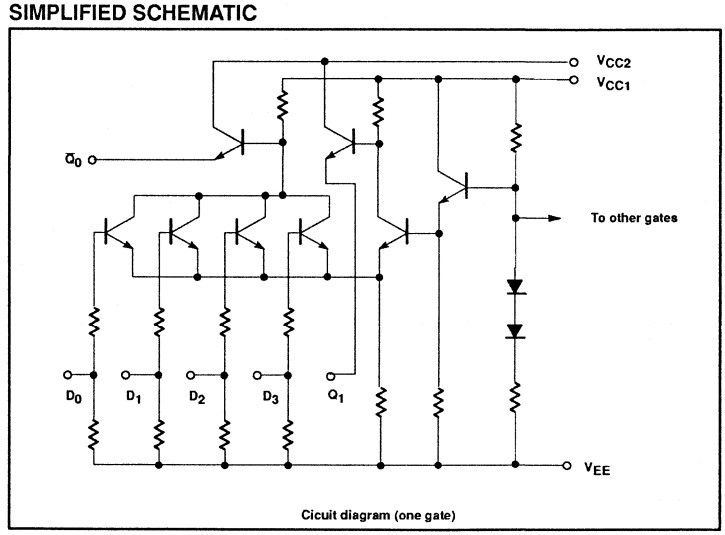


LOGIC DIAGRAM



$Q_0 = \overline{D_0 + D_1 + D_2 + D_3}$
$Q_1 = \overline{D_4 + D_5 + D_6 + D_5 + D_6}$
$Q_2 = D_0 + D_1 + D_2 + D_3$
$Q_3 = D_4 + D_5 + D_6 + D_5 + D_6$

SIMPLIFIED SCHEMATIC



Cicuit diagram (one gate)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to	–1060		–890	mV
		$T_A = +25°C$	all inputs. For $\overline{Q}_n$ outputs, apply	–960		–810	mV
		$T_A = +85°C$	V_{ILMIN} to all inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to each input,	–1080			mV
		$T_A = +25°C$	one at a time, w/ V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{ILT} to each	–980			mV
		$T_A = +85°C$	input w/ V_{IHMIN} applied to all other inputs.	–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to each input,			–1655	mV
		$T_A = +25°C$	one at a time, w/ V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to each			–1630	mV
		$T_A = +85°C$	input w/ V_{ILMIN} applied to all other inputs.			–1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to	–1890		–1675	mV
		$T_A = +25°C$	all inputs. For $\overline{Q}_n$ outputs, apply	–1850		–1650	mV
		$T_A = +85°C$	V_{ILMIN} to all inputs.	–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			425	µA
		$T_A = +25°C$	one at a time, with V_{ILMIN} applied			265	µA
		$T_A = +85°C$	to all other inputs.			265	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under test,	0.5			µA
		$T_A = +25°C$	one at a time, with V_{IHMAX} applied	0.5			µA
		$T_A = +85°C$	to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				15	mA
		$T_A = +25°C$			11	14	mA
		$T_A = +85°C$				15	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

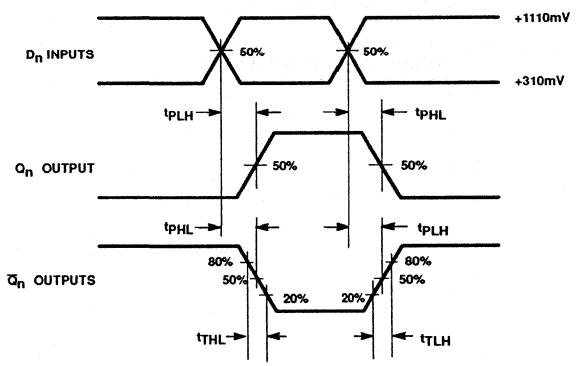
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_1, Q_3	Waveform 1	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_0$, $\overline{Q}_2$	Waveform 1	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.10 1.10	3.60 3.60	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Philips Components

Document No.	853–0646
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10110
Gate

Dual 3-Input/3-Output OR Gate (Line Driver)

FEATURES

- **Typical propagation delay: 2.4ns**
- **Typical supply current ($-I_{EE}$): 30mA**

DESCRIPTION

The 10110 is a Dual 3-Input/3-Output OR Gate intended to drive up to three transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

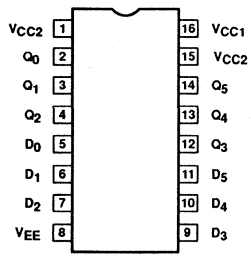
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10110N
16–Pin Ceramic DIP	10110F

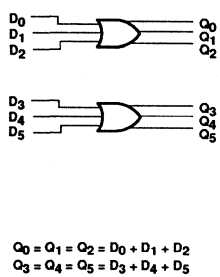
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
$Q_0 - Q_5$	Data Outputs (OR)

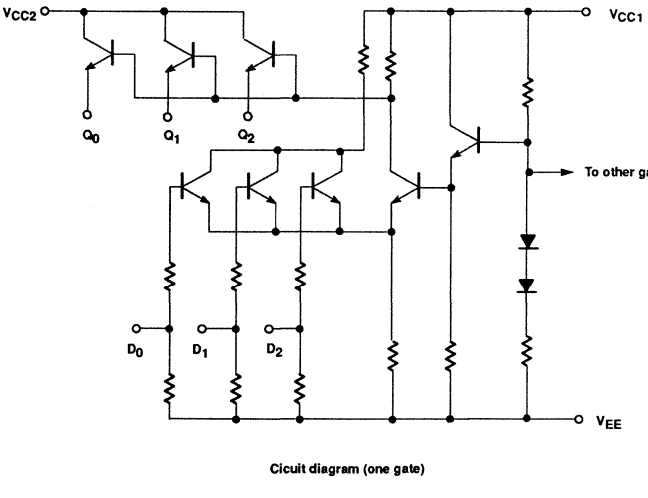
PIN CONFIGURATION



LOGIC DIAGRAM



SIMPLIFIED SCHEMATIC



Cicuit diagram (one gate)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to all inputs.	–1060		–890	mV
		$T_A = +25°C$		–960		–810	mV
		$T_A = +85°C$		–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{IHT} to each input,	–1080			mV
		$T_A = +25°C$	one at a time, with V_{ILMIN}	–980			mV
		$T_A = +85°C$	applied to all other inputs	–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Apply V_{ILT} to each input,			–1655	mV
		$T_A = +25°C$	one at a time, with V_{ILMIN}			–1630	mV
		$T_A = +85°C$	applied to all other inputs			–1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	Apply V_{ILMIN} to all inputs.	–1890		–1675	mV
		$T_A = +25°C$		–1850		–1650	mV
		$T_A = +85°C$		–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			680	µA
		$T_A = +25°C$	one at a time, with V_{ILMIN} applied			425	µA
		$T_A = +85°C$	to all other inputs.			425	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under test,	0.5			µA
		$T_A = +25°C$	one at a time, with V_{IHMAX} applied	0.5			µA
		$T_A = +85°C$	to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				42	mA
		$T_A = +25°C$			30	38	mA
		$T_A = +85°C$				42	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

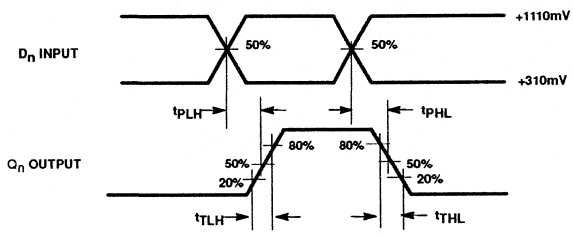
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.40 1.40	3.50 3.50	1.40 1.40	2.40 2.40	3.50 3.50	1.50 1.50	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	3.50 3.50	1.10 1.10	2.20 2.20	3.50 3.50	1.20 1.20	3.80 3.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0647
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10111
Gate

Dual 3-Input/3-Output NOR Gate (Line Driver)

FEATURES

- **Typical propagation delay: 2.4ns**
- **Typical supply current ($-I_{EE}$): 29mA**

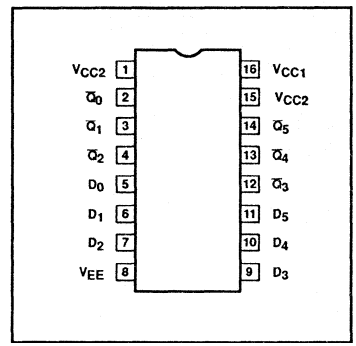
DESCRIPTION

The 10111 is a Dual 3-Input/3-Output NOR Gate intended to drive up to three transmission lines simultaneously. The ability to control three parallel lines makes this device particularly useful in clock distribution applications. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10111N
16–Pin Ceramic DIP	10111F

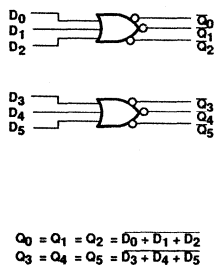
PIN CONFIGURATION



PIN DESCRIPTION

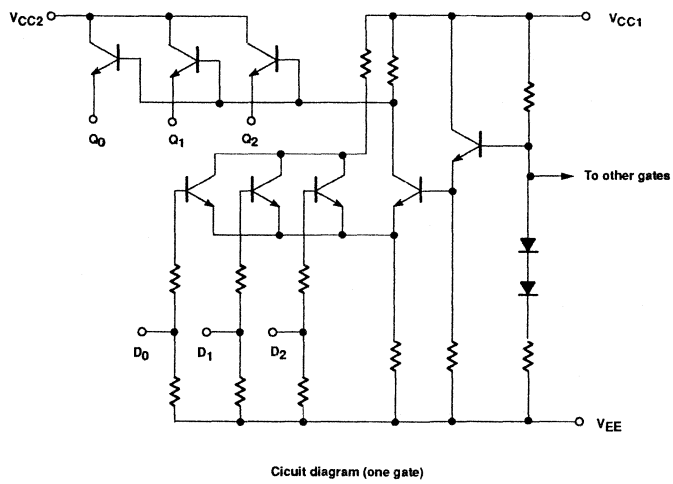
PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
$\overline{Q}_0 - \overline{Q}_5$	Data Outputs (NOR)

LOGIC DIAGRAM



$$Q_0 = Q_1 = Q_2 = \overline{D_0 + D_1 + D_2}$$
$$Q_3 = Q_4 = Q_5 = \overline{D_3 + D_4 + D_5}$$

SIMPLIFIED SCHEMATIC



Cicuit diagram (one gate)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Apply V_{ILMIN} to all inputs.	−1060		−890	mV
		$T_A = +25°C$		−960		−810	mV
		$T_A = +85°C$		−890		−700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{ILT} to each input,	−1080			mV
		$T_A = +25°C$	one at a time, with V_{ILMIN}	−980			mV
		$T_A = +85°C$	applied to all other inputs	−910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Apply V_{IHT} to each input,			−1655	mV
		$T_A = +25°C$	one at a time, with V_{ILMIN}			−1630	mV
		$T_A = +85°C$	applied to all other inputs			−1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to all inputs.	−1890		−1675	mV
		$T_A = +25°C$		−1850		−1650	mV
		$T_A = +85°C$		−1825		−1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under test,			680	µA
		$T_A = +25°C$	one at a time, with V_{ILMIN} applied			425	µA
		$T_A = +85°C$	to all other inputs.			425	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under test,	0.5			µA
		$T_A = +25°C$	one at a time, with V_{IHMAX} applied	0.5			µA
		$T_A = +85°C$	to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				42	mA
		$T_A = +25°C$			29	38	mA
		$T_A = +85°C$				42	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

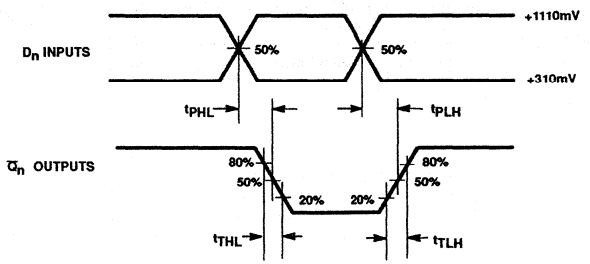
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 1	1.40 1.40	3.50 3.50	1.40 1.40	2.40 2.40	3.50 3.50	1.50 1.50	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	3.50 3.50	1.10 1.10	2.20 2.20	3.50 3.50	1.20 1.20	3.80 3.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0648
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10113
Gate

Quad Exclusive-OR Gate with Enable Input

FEATURES

- **Typical propagation delay: 2.6ns**
- **Typical supply current ($-I_{EE}$): 34mA**

DESCRIPTION

The 10113 is a Quadruple Exclusive-OR Gate with enable input common to all gates. The enable is active in Low State. A 4-bit comparison function (A = B) can be obtained by wire-ORing the four outputs together. Direct connection to buses is possible thanks to open-emitter outputs. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

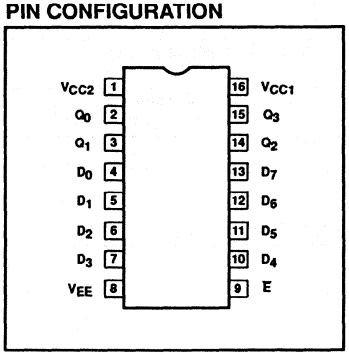
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10113N
16–Pin Ceramic DIP	10113F

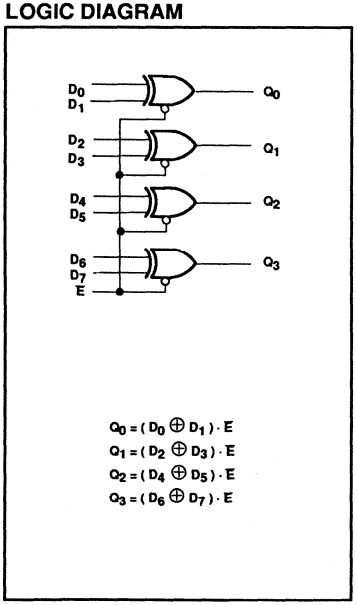
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
$\overline{E}$	Enable Input
$Q_0 - Q_3$	Data Outputs

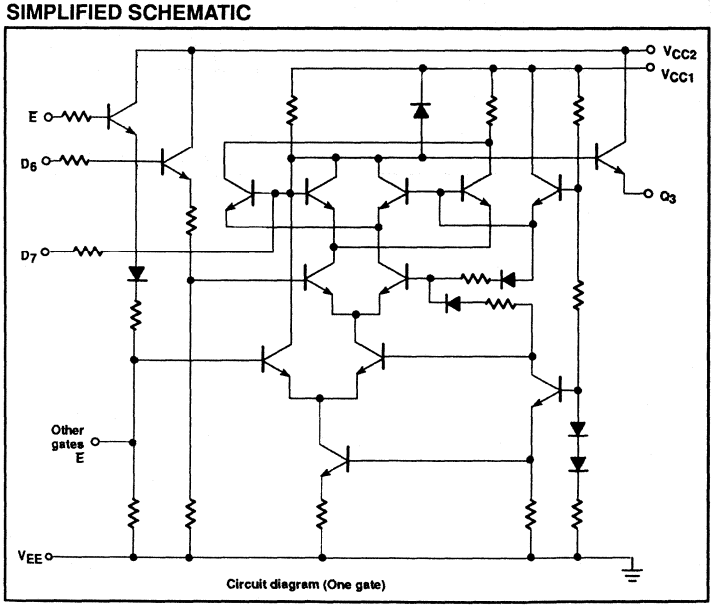
PIN CONFIGURATION



LOGIC DIAGRAM



SIMPLIFIED SCHEMATIC



Circuit diagram (One gate)

FUNCTION TABLE

INPUTS			OUTPUTS
D_0	D_1	$\overline{E}$	Q_0
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
X	X	H	L

H = High Voltage Level
X = Don't Care
L = Low Voltage Level

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{ILMIN} to enable input and one	−1060		−890	mV
			$T_A = +25°C$	gate input with V_{IHMAX} applied to	−960		−810	mV
			$T_A = +85°C$	the other gate input.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	Apply V_{IHT} to one gate input	−1080			mV
			$T_A = +25°C$	with V_{ILMIN} applied to the other	−980			mV
			$T_A = +85°C$	gate input and enable input.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	Apply V_{ILT} to one gate input			−1655	mV
			$T_A = +25°C$	with V_{ILMIN} applied to			−1630	mV
			$T_A = +85°C$	the other gate input.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$		−1890		−1675	mV
			$T_A = +25°C$	Apply V_{ILMIN} to all inputs for each output.	−1850		−1650	mV
			$T_A = +85°C$		−1825		−1615	mV
I_{IH}	High level input current	D_0, D_3	$T_A = -30°C$				425	µA
		D_4, D_7	$T_A = +25°C$	Apply V_{IHMAX} to each input under test,			265	µA
		inputs	$T_A = +85°C$	one at a time, with V_{ILMIN} applied			265	µA
		D_1, D_2	$T_A = -30°C$	to all other inputs.			350	µA
		D_5, D_6	$T_A = +25°C$				220	µA
		inputs	$T_A = +85°C$				220	µA
		$\overline{E}$	$T_A = -30°C$	Apply V_{IHMAX} to $\overline{E}$ input			870	µA
		input	$T_A = +25°C$	with V_{ILMIN} applied to			545	µA
			$T_A = +85°C$	all other inputs.			545	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under test,	0.5			µA
			$T_A = +25°C$	one at a time, with V_{IHMAX} applied	0.5			µA
			$T_A = +85°C$	to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				46	mA
			$T_A = +25°C$			34	42	mA
			$T_A = +85°C$				46	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

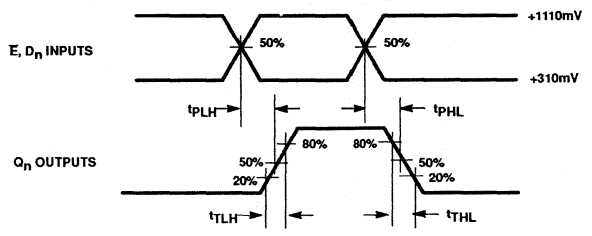
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.20 1.20	3.80 3.80	1.30 1.30	2.60 2.60	3.70 3.70	1.30 1.30	4.20 4.20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n	Waveform 1	1.30 1.30	4.10 4.10	1.50 1.50	3.40 3.40	4.00 4.00	1.50 1.50	4.60 4.60	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.30 1.30	3.50 3.50	1.30 1.30	2.50 2.50	3.50 3.50	1.30 1.30	3.50 3.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0649
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10114
Line Receiver

Triple Differential Line Receiver

FEATURES

- **Typical propagation delay: 2.4ns**
- **Typical supply current ($-I_{EE}$): 28mA**

DESCRIPTION

The 10114 is a Triple Differential Line Receiver with low-impedance emitter-follower complementary outputs. With translated emitter-follower inputs and an active current source, it features a peak common-mode rejection voltage of ± 1V.

Furthermore, the OR outputs keep a Low logic level whenever the inputs are left floating. Intended primarily to receive data from balanced twisted-pair lines, this device is also suitable for minicomputers, testing and instrumentation.

It can also be used as a sense amplifier for MOS RAMs as a MOS-to-ECL interface circuit, as a high-speed comparator and, having an internal reference bias voltage (V_{BB}) output, it can operate as a Schmitt trigger.

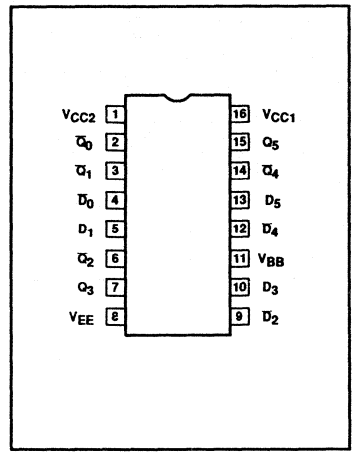
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10114N
16–Pin Ceramic DIP	10114F

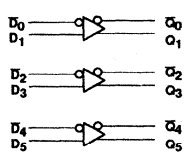
PIN DESCRIPTION

PINS	DESCRIPTION
$\overline{D}_0$, $\overline{D}_2$, $\overline{D}_4$; D_1, D_3, D_5	Data Inputs
Q_1, Q_3, Q_5	Data Outputs (OR)
$\overline{Q}_0$, $\overline{Q}_2$, $\overline{Q}_4$	Data Outputs (NOR)
V_{BB}	Reference Bias Voltage Output

PIN CONFIGURATION



LOGIC DIAGRAM



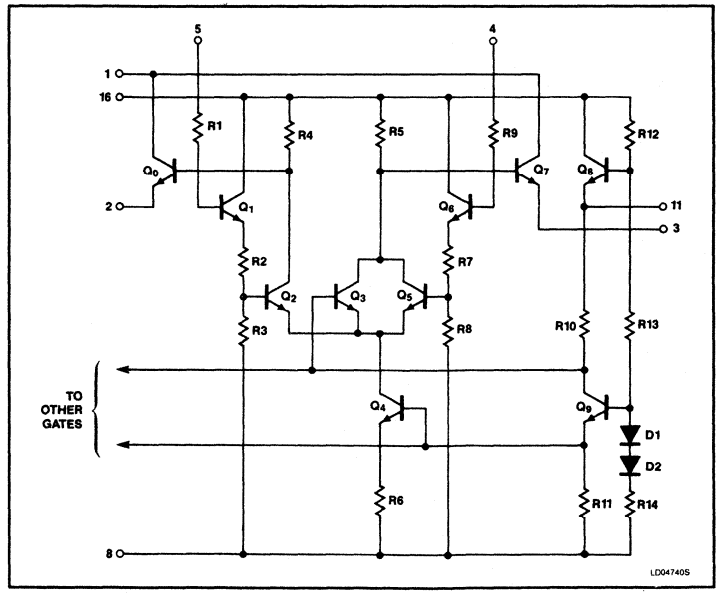
With inputs D_1, D_3 and D_5 connected to V_{BB} (pin 11)

$Q_0 = \overline{D}_0$
$Q_1 = D_0$
$Q_2 = \overline{D}_2$
$Q_3 = D_2$
$Q_4 = \overline{D}_4$
$Q_5 = D_4$

With all inputs open
$Q_0 = H$, $Q_1 = L$
$Q_2 = H$, $Q_3 = L$
$Q_4 = H$, $Q_5 = L$

H = High Voltage Level
L = Low Voltage Level

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		+5.0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC OPERATING CONDITIONS FOR COMMON–MODE REJECTION TEST $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{IHH}	V_{IHMAX} + 1.0V	$T_A = -30°C$			+110	mV
		$T_A = +25°C$			+190	mV
		$T_A = +85°C$			+300	mV
V_{IHL}	V_{IHMAX} – 1.0V	$T_A = -30°C$			–1890	mV
		$T_A = +25°C$			–1810	mV
		$T_A = +85°C$			–1700	mV
V_{ILH}	V_{ILMIN} + 1.0V	$T_A = -30°C$	–890			mV
		$T_A = +25°C$	–850			mV
		$T_A = +85°C$	–825			mV
V_{ILL}	V_{ILMIN} – 1.0V	$T_A = -30°C$	–2890			mV
		$T_A = +25°C$	–2850			mV
		$T_A = +85°C$	–2825			mV

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{IHMAX} to each inverting input, one at a time, w/ V_{ILMIN} applied to all other	–1060		–890	mV
		$T_A = +25°C$	inverting inputs and V_{BB} applied to all non–inverting inputs. For Q_n outputs, apply V_{ILMIN} to each	–960		–810	mV
		$T_A = +85°C$	inverting input, one at a time, with V_{BB} applied to all non–inverting inputs and w/ V_{IHMAX} applied to all other inverting inputs.[4]	–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{IHT} to each inverting input, one at a time, w/ V_{ILMIN} applied to all other inverting	–1080			mV
		$T_A = +25°C$	inputs and V_{BB} applied to all non–inverting inputs. For Q_n outputs, apply V_{ILT} to each inverting input,	–980			mV
		$T_A = +85°C$	one at a time, with V_{BB} applied to all non–inverting inputs and w/ V_{IHMAX} applied to all other inverting inputs.[4]	–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{ILT} to each inverting input, one at a time, w/ V_{BB} applied to all non–inverting			–1655	mV
		$T_A = +25°C$	inputs and V_{IHMAX} applied to all other inverting inputs. For Q_n outputs, apply V_{IHT} to each inverting			–1630	mV
		$T_A = +85°C$	input, one at a time, with V_{BB} applied to all non–inverting inputs and V_{ILMIN} applied to all other inverting inputs.[4]			–1595	mV

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OL}	Low level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to each inverting input, one at a time, w/ V_{BB} applied to all non–inverting	–1890		–1675	mV
		$T_A = +25°C$	inputs and V_{IHMAX} applied to all other inverting inputs. For Q_n outputs, apply V_{IHMAX} to each inverting	–1850		–1650	mV
		$T_A = +85°C$	input, one at a time, with V_{BB} applied to all non–inverting inputs and V_{ILMIN} applied to all other inverting inputs.[4]	–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each inverting input under test, one at a time, w/ V_{ILMIN} applied to all other inverting			70	µA
		$T_A = +25°C$	inputs and V_{BB} applied to all non–inverting inputs. Apply V_{IHMAX} to each non–inverting input under test,			45	µA
		$T_A = +85°C$	one at a time, with V_{ILMIN} applied to all other non–inverting inputs and V_{BB} applied to all inverting inputs.[4]			45	µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$	Apply V_{ILMIN} to all inverting			39	mA
		$T_A = +25°C$	inputs. Apply V_{BB} to all		28	35	mA
		$T_A = +85°C$	non–inverting inputs.			39	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V
V_{BB}	Reference voltage	$T_A = -30°C$	All inverting or all non–inverting	–1420		–1280	mV
		$T_A = +25°C$	input pins are tied to the V_{BB} pin	–1350	–1290	–1230	mV
		$T_A = +85°C$	during measurement.	–1295		–1150	mV
V_{OH}	High level output voltage for Common–Mode Rejection Test	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{IHH} to inverting inputs and	–1060		–1280	mV
		$T_A = +25°C$	V_{ILH} to non–inverting inputs. For Q_n outputs, apply	–960		–810	mV
		$T_A = +85°C$	V_{ILL} to inverting inputs and V_{IHL} to non–inverting inputs.	–890		–700	mV
V_{OL}	Low level output voltage for Common–Mode Rejection Test	$T_A = -30°C$	For $\overline{Q}_n$ outputs, apply V_{ILH} to inverting inputs and	–1890		–1675	mV
		$T_A = +25°C$	V_{IHH} to non–inverting inputs. For Q_n outputs, apply	–1850		–1650	mV
		$T_A = +85°C$	V_{IHL} to inverting inputs and V_{ILL} to non–inverting inputs.	–1825		–1615	mV
$-I_{CBO}$	Input leakage current	$T_A = -30°C$	Apply V_{EE} to each inverting input under test, one at			1.5	µA
		$T_A = +25°C$	a time, w/ V_{ILMIN} applied to all other inverting inputs			1.0	µA
		$T_A = +85°C$	and V_{BB} applied to all non–inverting inputs.[4]			1.0	µA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. Refer to DC Test Circuit.

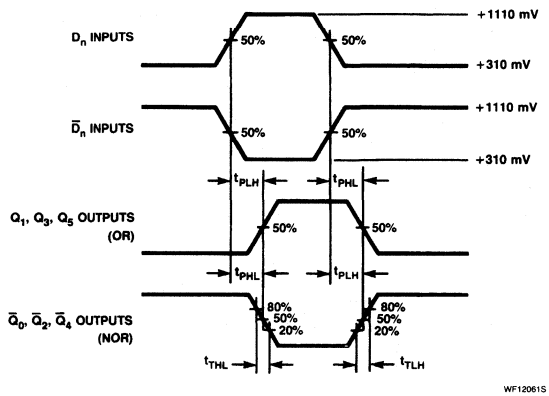
Line Receiver 10114

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	4.40 4.40	1.00 1.00	2.40 2.40	4.00 4.00	0.90 0.90	4.30 4.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{D}_n$ to Q_n		1.00 1.00	4.40 4.40	1.00 1.00	2.40 2.40	4.00 4.00	0.90 0.90	4.30 4.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.50 1.50	3.80 3.80	1.50 1.50	2.10 2.10	3.50 3.50	1.50 1.50	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

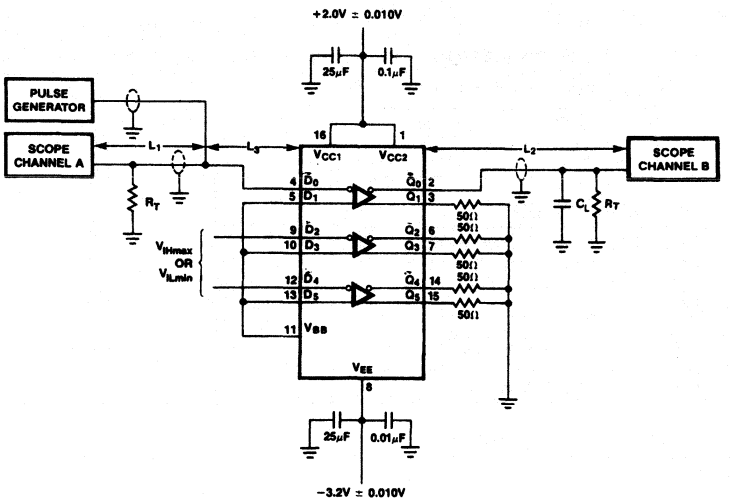
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

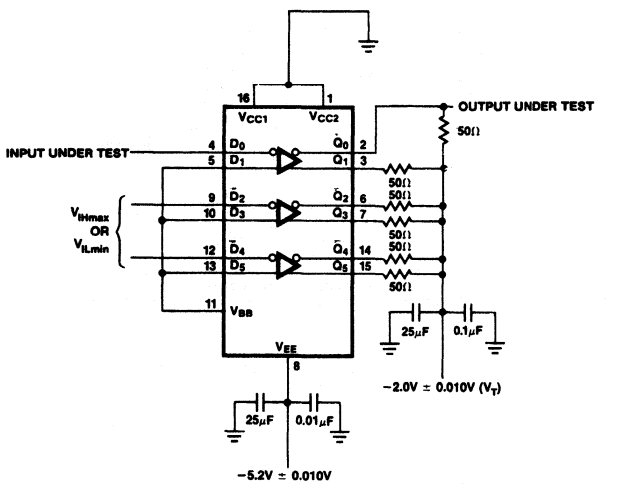
Line Receiver 10114

AC TEST CIRCUIT



NOTES:
1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}. 0.01μF and 25μF from GND to V_{EE} (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the logic function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 equal length 50Ω impedance lines. L_3 the distance from the DUT pin and the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

DC TEST CIRCUIT



NOTES:
1. $V_{CC1} = V_{CC2} = 0V$ (GND), $V_{EE} = -5.2V \pm 0.010V$.
2. Decoupling 0.01μF and 25μF from GND to V_{EE}, 0.1μF and 25μF from GND to V_T (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT, and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the logic function required.
4. All unused outputs are loaded with 50Ω to V_T.
5. All 50Ω resistors should have tolerance of ±1% or better.

Philips Components

Document No.	853–0650
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Date of Issue	June 14, 1990
Status	Product Status
ECL Products	

10115
Line Receiver

Quad Differential Line Receiver

FEATURES

- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 18mA**

DESCRIPTION

The 10115 is a Quad Differential Line Receiver intended for use in sensing signals over long lines. The base Reference Bias Voltage (V_{BB}) makes the device useful in other applications where a stable reference voltage is necessary.

One input from any unused amplifier in a package must be tied to V_{BB}.

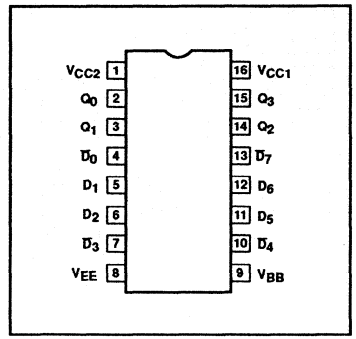
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10115N
16–Pin Ceramic DIP	10115F

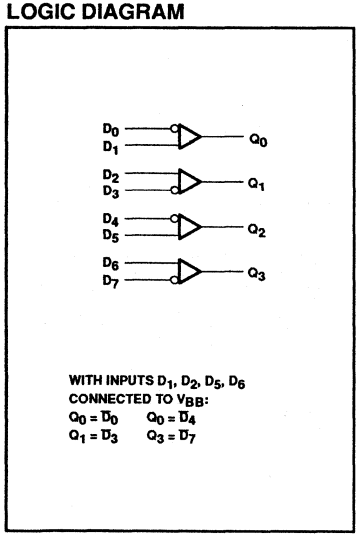
PIN DESCRIPTION

PINS	DESCRIPTION
D_1, D_2, D_5, D_6; $\overline{D}_0$, $\overline{D}_3$, $\overline{D}_4$, $\overline{D}_7$	Data Inputs
V_{BB}	Reference Bias Voltage Output
$Q_0 - Q_3$	Data Outputs

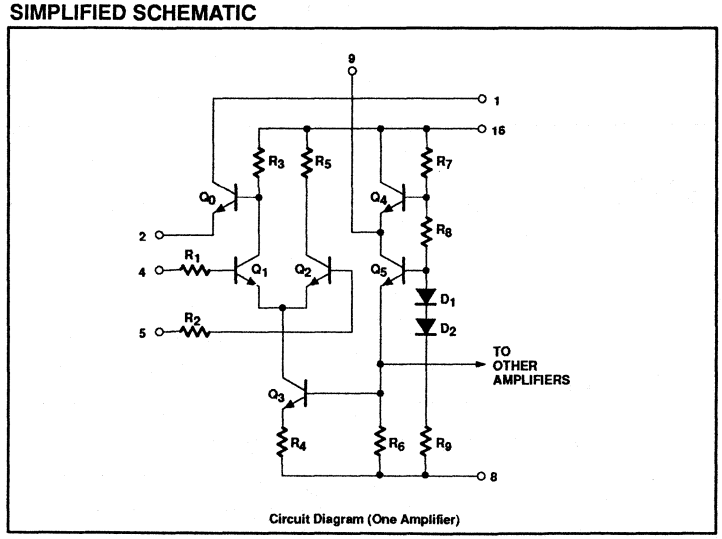
PIN CONFIGURATION



LOGIC DIAGRAM



SIMPLIFIED SCHEMATIC



Circuit Diagram (One Amplifier)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Apply V_{ILMIN} to each inverting input, one at a time, w/ V_{IHMAX} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs. Apply V_{IHMAX} to each non–inverting input, one at a time, with V_{ILMIN} applied to all other non–inverting inputs and w/ V_{BB} applied to all other inverting inputs.[4]	–1060		–890	mV
		$T_A = +25°C$		–960		–810	mV
		$T_A = +85°C$		–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{ILT} to each inverting input, one at a time, w/ V_{ILMIN} applied to all other inverting input and V_{BB} applied to all non–inverting inputs. Apply V_{IHT} to each non–inverting input, one at a time, with V_{ILMIN} applied to all other non–inverting inputs and w/ V_{BB} applied to all inverting inputs.[4]	–1080			mV
		$T_A = +25°C$		–980			mV
		$T_A = +85°C$		–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Apply V_{IHT} to each inverting input, one at a time, w/ V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs. Apply V_{ILT} to each non–inverting input, one at a time, with V_{ILMIN} applied to all other non–inverting inputs and V_{BB} applied to all inverting inputs.[4]			–1655	mV
		$T_A = +25°C$				–1630	mV
		$T_A = +85°C$				–1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	Apply V_{IhMAX} to each inverting input, one at a time, w/ V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs. Apply V_{ILMIN} to each non–inverting input, one at a time, w/ V_{IHMAX} applied to all other non–inverting inputs and V_{BB} applied to all inverting inputs.[4]	–1890		–1675	mV
		$T_A = +25°C$		–1850		–1650	mV
		$T_A = +85°C$		–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each inverting input under test, one at a time, w/ V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs. [4]			150	µA
		$T_A = +25°C$				95	µA
		$T_A = +85°C$				95	µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$	Apply V_{ILMIN} to all inverting inputs. Apply V_{BB} to all non–inverting inputs.			29	mA
		$T_A = +25°C$			18	26	mA
		$T_A = +85°C$				29	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V
V_{BB}	Reference voltage	$T_A = -30°C$	All inverting or all non–inverting input pins are tied to the V_{BB} pin during measurement.	–1420		–1280	mV
		$T_A = +25°C$		–1350	–1290	–1230	mV
		$T_A = +85°C$		–1295		–1150	mV
$-I_{CBO}$	Input leakage current	$T_A = -30°C$	Apply V_{EE} to each inverting input under test, one at a time, w/ V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]			1.5	µA
		$T_A = +25°C$				1.0	µA
		$T_A = +85°C$				1.0	µA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. Refer to DC Test Circuit.

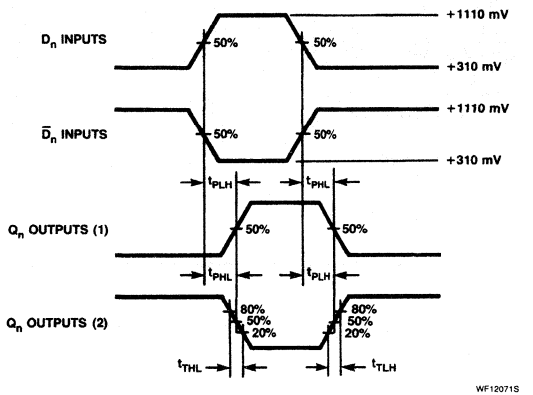
Line Receiver 10115

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n, $\overline{D}_n$ to Q_n	Waveform 1	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.10 1.10	3.60 3.60	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

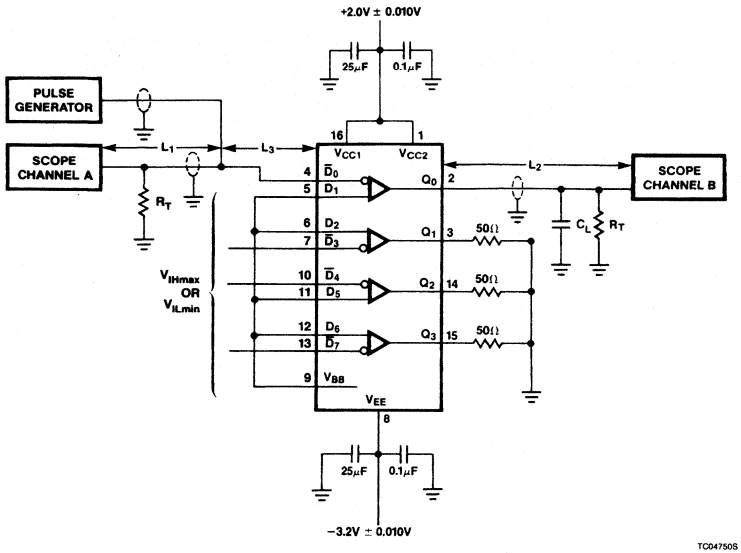
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

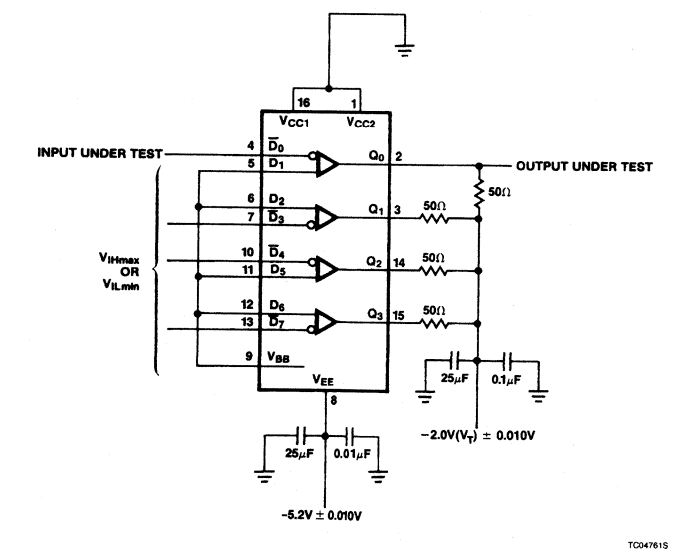
Line Receiver 10115

AC TEST CIRCUIT



NOTES:
1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to V_{CC}, 0.01μF and 25μF from GND to V_{EE} (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

DC TEST CIRCUIT



NOTES:
1. $V_{CC1} = V_{CC2}$ = GND (0V), $V_{EE} = -5.2V \pm 0.010V$.
2. Decoupling 0.01μF and 25μF from GND to V_{EE}, 0.1μF and 25μF from GND to V_T (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT, and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to V_T.
5. All 50Ω resistors should have tolerance of ± 1% or better.

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ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10116
Line Receiver

Triple Differential Line Receiver

FEATURES

- **Typical propagation delay: 2.4ns**
- **Typical supply current ($-I_{EE}$): 17mA**

DESCRIPTION

The 10116 is a Triple Differential Line Receiver with low-impedance emitter-follower complementary outputs.

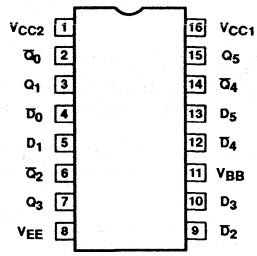
Intended primarily to receive data from twisted-pair lines, this device is also suitable for minicomputers, testing and instrumentation. It can also be used as a sense amplifier for MOS RAMs as a MOS-to-ECL interface circuit; as a high-speed comparator and having an internal reference supply voltage (V_{BB}) output, it can operate as a Schmitt Trigger.

One input from any unused amplifier in a package must be tied to V_{BB}.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10116N
16–Pin Ceramic DIP	10116F
16–Pin SO	10116D

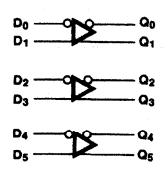
PIN CONFIGURATION



PIN DESCRIPTION

PINS	DESCRIPTION
$\overline{D}_0$, $\overline{D}_2$, $\overline{D}_4$; D_1, D_3, D_5	Data Inputs
V_{BB}	Reference Bias Voltage Output
Q_1, Q_3, Q_5	Data Outputs (OR)
$\overline{Q}_0$, $\overline{Q}_2$, $\overline{Q}_4$	Data Outputs (NOR)

LOGIC DIAGRAM

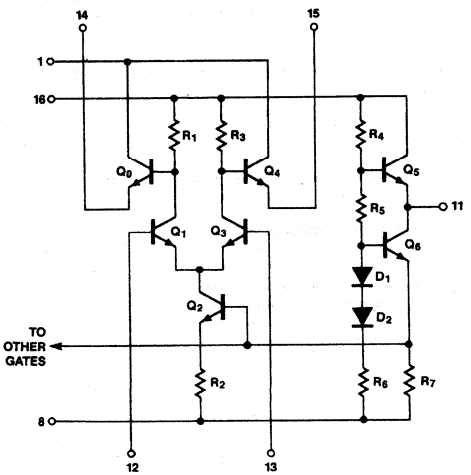


WITH INPUTS D_1,D_3 AND D_5 CONNECTED TO V_{BB} (PIN 11)

$Q_0 = D_0$
$Q_1 = \overline{D}_0$
$Q_2 = D_2$
$Q_3 = \overline{D}_2$
$Q_4 = D_4$
$Q_5 = \overline{D}_4$

LD05301S

SIMPLIFIED SCHEMATIC



TC04381S

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

Line Receiver | 10116

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to each inverting input, one at a time, w/ V_{IHMAX} applied to all other	–1060		–890	mV
		$T_A = +25°C$	inverting inputs and V_{BB} applied to all non–inverting inputs. For $\overline{Q}_n$ outputs, apply V_{IHMAX} to each	–960		–810	mV
		$T_A = +85°C$	inverting input, one at a time, with V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]	–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to each inverting input, one at a time, w/ V_{IHMAX} applied to all other	–1080			mV
		$T_A = +25°C$	inverting inputs and V_{BB} applied to all non–inverting inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to each inverting	–980			mV
		$T_A = +85°C$	input, one at a time, with V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]	–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to each inverting input, one at a time, w/ V_{ILMIN} applied to all other inverting			–1655	mV
		$T_A = +25°C$	inputs and V_{BB} applied to all non–inverting inputs. For $\overline{Q}_n$ outputs, apply V_{ILT} to each inverting			–1630	mV
		$T_A = +85°C$	input, one at a time, with V_{IHMAX} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]			–1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to each inverting input, one at a time, w/ V_{ILMIN} applied to all other	–1890		–1675	mV
		$T_A = +25°C$	inverting inputs and V_{BB} applied to all non–inverting inputs. For $\overline{Q}_n$ outputs, apply V_{ILMIN} to each	–1850		–1650	mV
		$T_A = +85°C$	inverting input, one at a time, with V_{IHMAX} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]	–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each inverting input under test, one at a time, w/ V_{ILMIN} applied to all other inverting			150	µA
		$T_A = +25°C$	inputs and V_{BB} applied to all non–inverting inputs. Apply V_{IHMAX} to each non–inverting input under test,			95	µA
		$T_A = +85°C$	one at a time, with V_{ILMIN} applied to all other non–inverting inputs and V_{BB} applied to all inverting inputs.[4]			95	µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$	Apply V_{ILMIN} to all inverting			23	mA
		$T_A = +25°C$	inputs. Apply V_{BB} to all		17	21	mA
		$T_A = +85°C$	non–inverting inputs.			23	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation	$T_A = +25°C$			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation	$T_A = +25°C$			0.148		V/V
V_{BB}	Reference voltage	$T_A = -30°C$	All inverting or all non–inverting	–1420		–1280	mV
		$T_A = +25°C$	input pins are tied to the V_{BB} pin	–1350	–1290	–1230	mV
		$T_A = +85°C$	during measurement.	–1295		–1150	mV
$-I_{CBO}$	Input leakage current	$T_A = -30°C$	Apply V_{EE} to each inverting input under test, one at			1.5	µA
		$T_A = +25°C$	a time, w/ V_{ILMIN} applied to all other inverting inputs			1.0	µA
		$T_A = +85°C$	and V_{BB} applied to all non–inverting inputs.[4]			1.0	µA

See notes on following page.

Line Receiver 10116

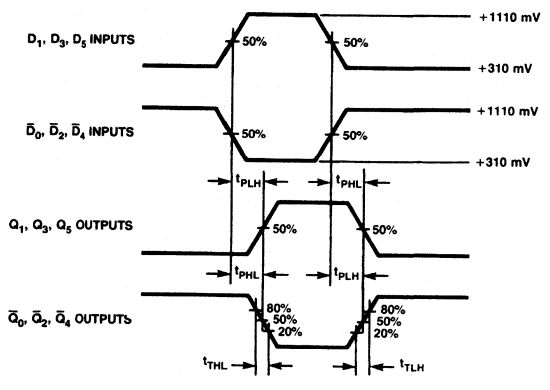
NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. Refer to DC Test Circuit.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{D}_n$ to Q_n		1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.10 1.10	3.60 3.60	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

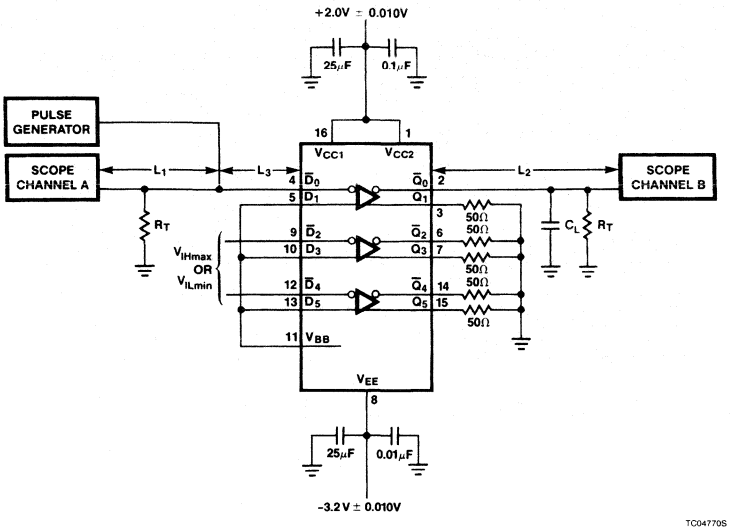
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

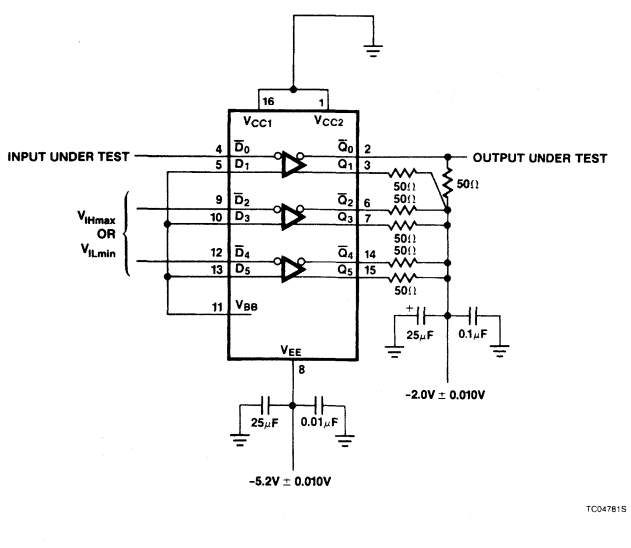
Line Receiver 10116

AC TEST CIRCUIT



NOTES:
1. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}, 0.01μF and 25μF from GND to V_{EE} (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lesd length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3 the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should should not exceed 1/4 inch (6mm).
6. R_T = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

DC TEST CIRCUIT



NOTES:
1. $V_{CC1} = V_{CC2} = 0V$ (GND), $V_{EE} = -5.2V \pm 0.010V$.
2. Decoupling 0.01μF and 25μF from GND to V_{EE}, 0.1μF and 25μF from GND to V_T (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¾ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to V_T.
5. All 50Ω resistors should have tolerance of ± 1% or better.

Document No.	853–0652
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10117
Gate

Dual 2-Wide 2-3 Input OR-AND/OR-AND-INVERT Gate

FEATURES

- **Typical propagation delay: 2.3ns**
- **Typical supply current ($-I_{EE}$): 20mA**

DESCRIPTION

The 10117 is a dual 2-wide 2-input OR-AND/OR-AND-INVERT Gate designed for use in data control as a general purpose logic element. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

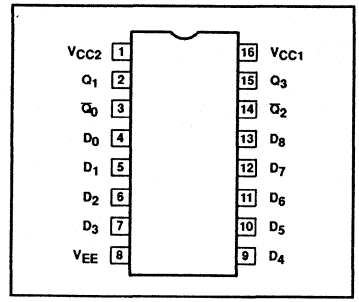
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10117N
16–Pin Ceramic DIP	10117F
16–Pin SO	10117D

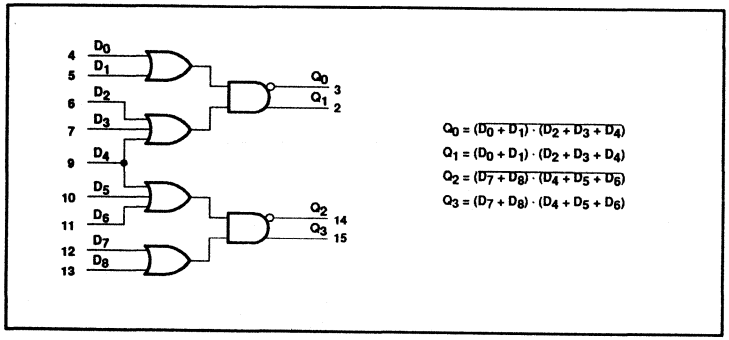
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_8$	Data Inputs
$\overline{Q}_0$, $\overline{Q}_2$, Q_1, Q_3	Data Outputs

PIN CONFIGURATION

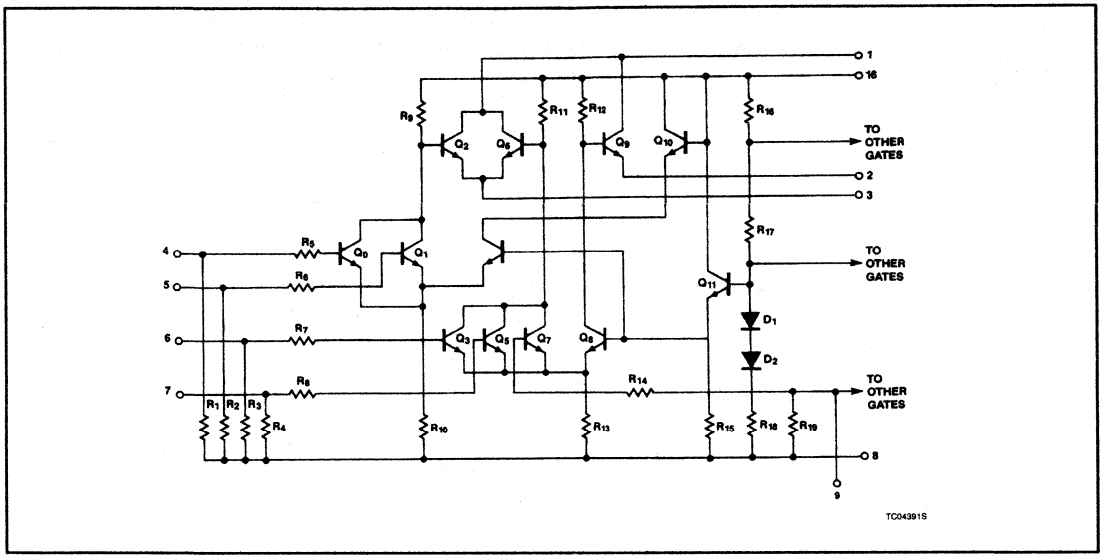


LOGIC DIAGRAM



Gate 10117

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_1 and Q_3 outputs, apply	–1060		–890	mV
			$T_A = +25°C$	V_{IHMAX} to all inputs. For $\overline{Q}_0$ and $\overline{Q}_2$	–960		–810	mV
			$T_A = +85°C$	outputs, apply V_{ILMIN} to all inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_1 input, apply V_{IHT} to D_0 input with V_{ILMIN}	–1080			mV
			$T_A = +25°C$	applied to D_1 input and V_{IHMAX} applied to all other inputs. For $\overline{Q}_0$ output, apply V_{ILT} to D_0 input with	–980			mV
			$T_A = +85°C$	V_{ILMIN} applied to D_1 input and V_{IHMAX} applied to all other inputs.	–910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_1 input, apply V_{ILT} to D_0 input with V_{ILMIN}			–1655	mV
			$T_A = +25°C$	applied to D_1 input and V_{IHMAX} applied to all other inputs. For $\overline{Q}_0$ output, apply V_{IHT} to D_0 input with			–1630	mV
			$T_A = +85°C$	V_{ILMIN} applied to D_1 input and V_{IHMAX} applied to all other inputs.			–1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_1 and Q_3 outputs, apply	–1890		–1675	mV
			$T_A = +25°C$	V_{ILMIN} to all inputs. For $\overline{Q}_0$ and $\overline{Q}_2$	–1850		–1650	mV
			$T_A = +85°C$	outputs, apply V_{IHMAX} to all inputs.	–1825		–1615	mV
I_{IH}	High level input current	D_4 input	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			560	µA
			$T_A = +25°C$				350	µA
			$T_A = +85°C$				350	µA
		All other inputs	$T_A = -30°C$				390	µA
			$T_A = +25°C$				245	µA
			$T_A = +85°C$				245	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				29	mA
			$T_A = +25°C$			20	26	mA
			$T_A = +85°C$				29	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.40 1.40	3.90 3.90	1.40 1.40	2.30 2.30	3.40 3.40	1.40 1.40	3.80 3.80	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 1	1.40 1.40	3.90 3.90	1.40 1.40	2.30 2.30	3.40 3.40	1.40 1.40	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	0.90 0.90	4.10 4.10	1.10 1.10	2.20 2.20	4.00 4.00	1.10 1.10	4.60 4.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

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Status	Product Specification
ECL Products	

10118
Gate

Dual 2-Wide 3-Input OR-AND Gate

FEATURES

- **Typical propagation delay: 2.3ns**
- **Typical supply current ($-I_{EE}$): 20mA**

DESCRIPTION

The 10118 is a dual 2-Wide 3-Input OR-AND Gate designed for use in data control as a general purpose logic element. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

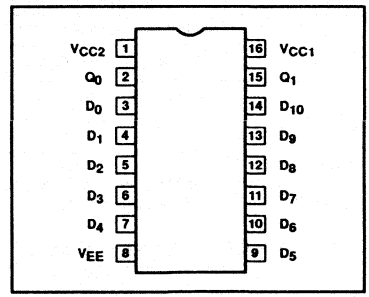
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10118N
16–Pin Ceramic DIP	10118F

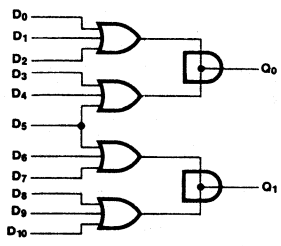
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_{10}$	Data Inputs
Q_0, Q_1	Data Outputs

PIN CONFIGURATION

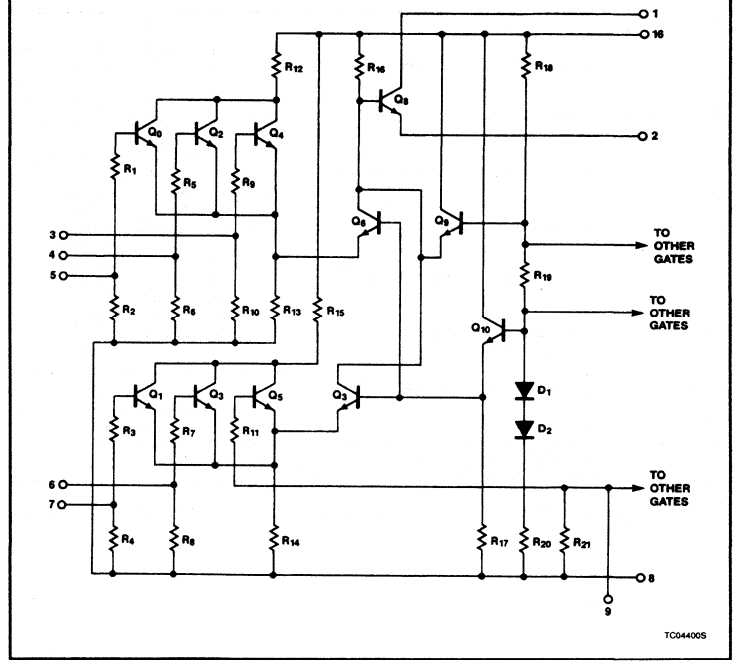


LOGIC DIAGRAM



$Q_1 = (D_0 + D_1 + D_2) \cdot (D_3 + D_4 + D_5)$
$Q_1 = (D_5 + D_6 + D_7) \cdot (D_8 + D_{10} + D_{11})$

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{IHMAX} to all inputs.	−1060		−890	mV
			$T_A = +25°C$		−960		−810	mV
			$T_A = +85°C$		−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_0 output, apply V_{IHT} to D_0 input with	−1080			mV
			$T_A = +25°C$	V_{ILMIN} applied to D_1 and D_2 inputs and	−980			mV
			$T_A = +85°C$	V_{IHMAX} applied to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_0 output, apply V_{ILT} to D_0 input with			−1655	mV
			$T_A = +25°C$	V_{ILMIN} applied to D_1 and D_2 inputs and			−1630	mV
			$T_A = +85°C$	V_{IHMAX} applied to all other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	Apply V_{ILMIN} to all inputs.	−2000		−1675	mV
			$T_A = +25°C$		−1990		−1650	mV
			$T_A = +85°C$		−1920		−1615	mV
I_{IH}	High level input current	D_5 input	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			560	µA
			$T_A = +25°C$				350	µA
			$T_A = +85°C$				350	µA
		All other inputs	$T_A = -30°C$				390	µA
			$T_A = +25°C$				245	µA
			$T_A = +85°C$				245	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under test, one at a time, with V_{IHMAX} applied to all other inputs.	0.5			µA
			$T_A = +25°C$		0.5			µA
			$T_A = +85°C$		0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				29	mA
			$T_A = +25°C$			20	26	mA
			$T_A = +85°C$				29	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.40 1.40	3.90 3.90	1.40 1.40	2.30 2.30	3.40 3.40	1.40 1.40	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	0.80 0.80	4.10 4.10	1.50 1.50	2.50 2.50	4.00 4.00	1.50 1.50	4.60 4.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

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Status	Product Specification
ECL Products	

10119
Gate

4-Wide 4-3-3-3-Input OR-AND Gate

FEATURES

- **Typical propagation delay: 2.3ns**
- **Typical supply current ($-I_{EE}$): 20mA**

DESCRIPTION

The 10119 is a 4-wide 4-3-3-3-Input OR-AND Gate designed for use in data control as a general purpose logic element. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

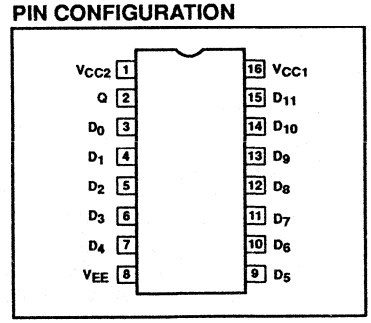
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10119N
16–Pin Ceramic DIP	10119F

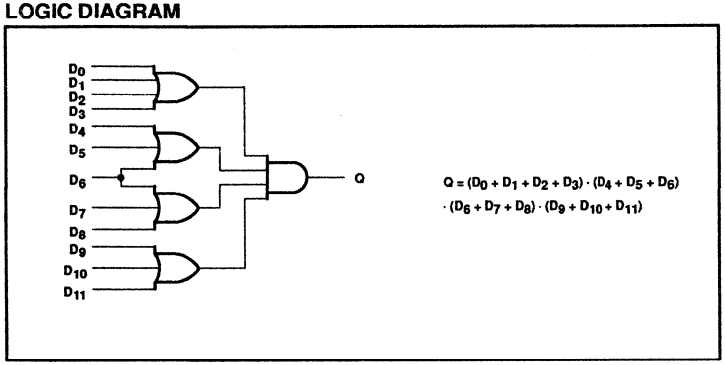
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_{11}$	Data Inputs
Q	Data Output

PIN CONFIGURATION

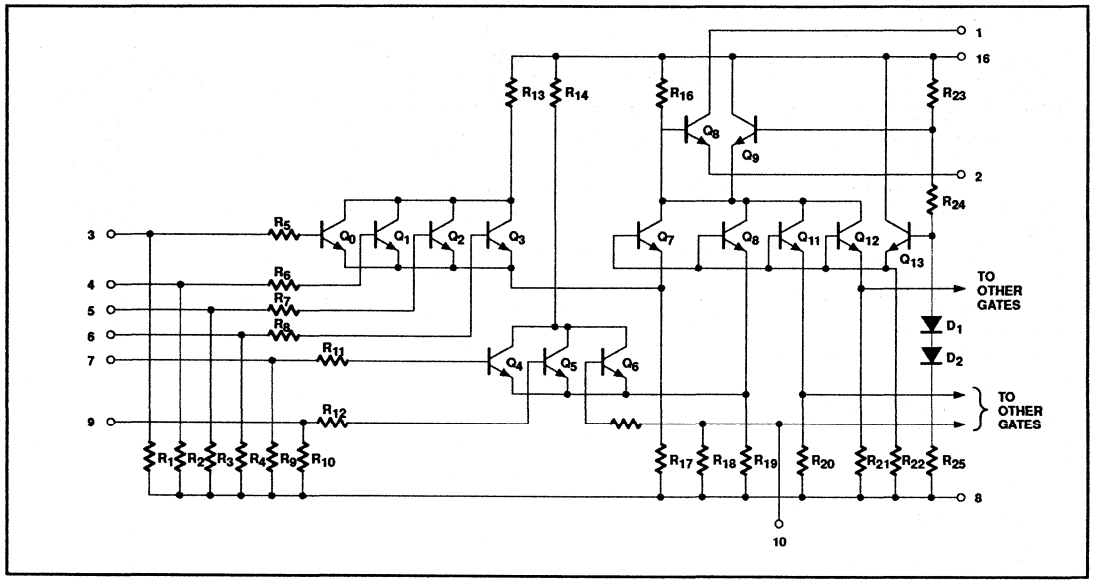


LOGIC DIAGRAM



Gate 10119

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{IHMAX} to all inputs.	−1060		−890	mV
			$T_A = +25°C$		−960		−810	mV
			$T_A = +85°C$		−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	Apply V_{IHT} to D_0 input with V_{ILMIN}	−1080			mV
			$T_A = +25°C$	applied to D_1, D_2, and D_3 inputs and	−980			mV
			$T_A = +85°C$	V_{IHMAX} applied to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	Apply V_{ILT} to D_0 input with V_{ILMIN}			−1655	mV
			$T_A = +25°C$	applied to D_1, D_2, and D_3 inputs and			−1630	mV
			$T_A = +85°C$	V_{IHMAX} applied to all other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	Apply V_{ILMIN} to all inputs.	−2000		−1675	mV
			$T_A = +25°C$		−1990		−1650	mV
			$T_A = +85°C$		−1920		−1615	mV
I_{IH}	High level input current	D_6 input	$T_A = -30°C$	Apply V_{ILMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			495	mV
			$T_A = +25°C$				310	mV
			$T_A = +85°C$				310	mV
		All other inputs	$T_A = -30°C$				390	mV
			$T_A = +25°C$				245	mV
			$T_A = +85°C$				245	mV
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under test, one at a time, with V_{IHMAX} applied to all other inputs.	0.5			µA
			$T_A = +25°C$		0.5			µA
			$T_A = +85°C$		0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				29	mA
			$T_A = +25°C$			20	26	mA
			$T_A = +85°C$				29	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH}	Propagation delay	Waveform 1	1.40	3.90	1.40	2.30	3.40	1.40	3.80	ns
t_{PHL}	D_n to Q_n		1.40	3.90	1.40	2.30	3.40	1.40	3.80	ns
t_{TLH}	Transition time		0.80	4.10	1.50	2.50	4.00	1.50	4.60	ns
t_{THL}	20% to 80%, 80% to 20%		0.80	4.10	1.50	2.50	4.00	1.50	4.60	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

Philips Components

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Status	Product Specification
ECL Products	

10121
Gate

4-Wide OR-AND/OR-AND-INVERT Gate

FEATURES

- **Typical propagation delay: 2.3ns**
- **Typical supply current ($-I_{EE}$): 20mA**

DESCRIPTION

The 10121 is a 4-Wide OR-AND/OR-AND-INVERT Gate designed for use in data control as a general purpose logic element. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

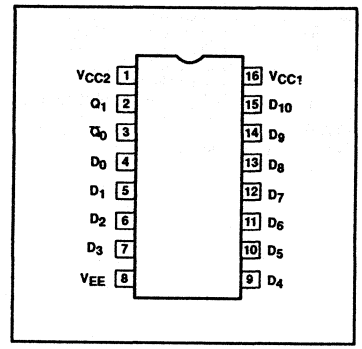
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10121N
16–Pin Ceramic DIP	10121F

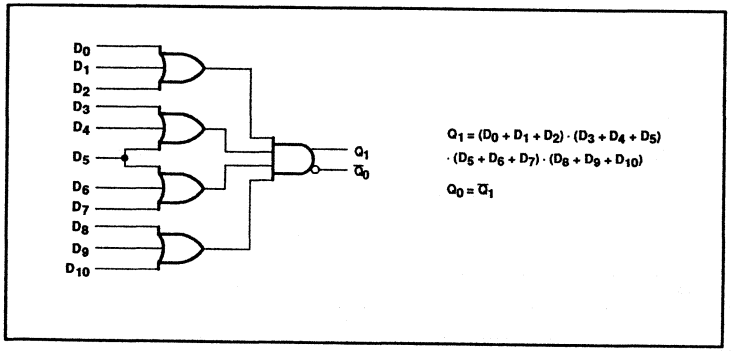
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_{10}$	Data Inputs
$\overline{Q}_0$, Q_1	Data Outputs

PIN CONFIGURATION

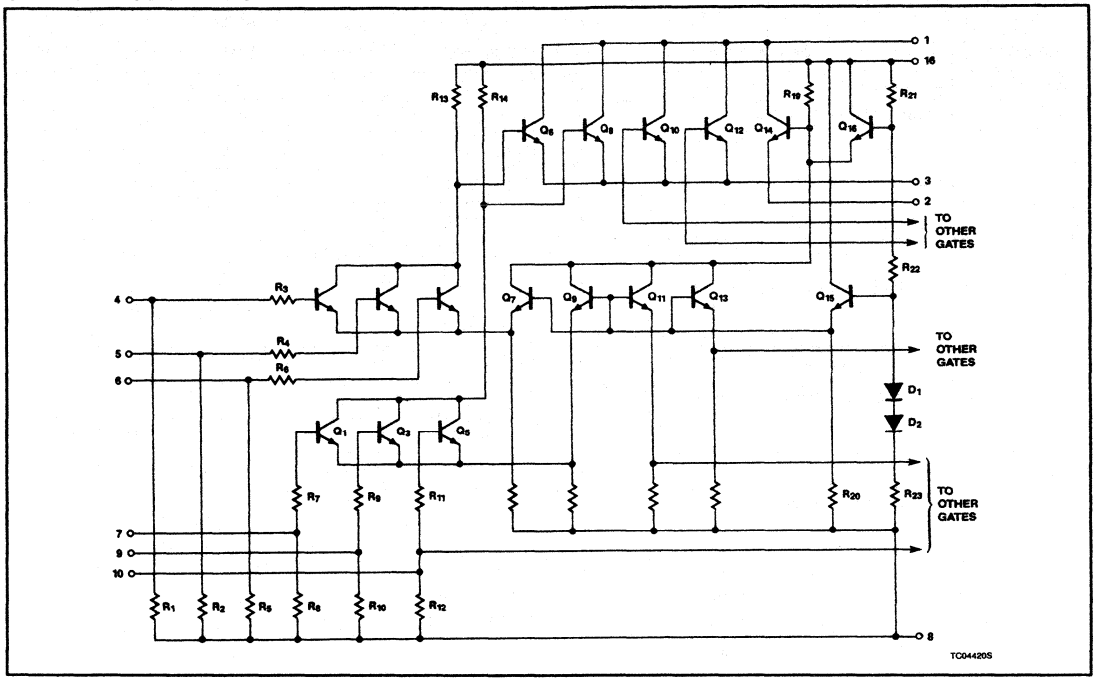


LOGIC DIAGRAM



Gate 10121

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_1 output, apply V_{IHMAX}	−1060		−780	mV
			$T_A = +25°C$	to all inputs. For $\overline{Q}_0$ output	−960		−700	mV
			$T_A = +85°C$	apply V_{ILMIN} to all inputs.	−890		−590	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_1 output apply V_{IHT} to D_0 input with V_{ILMIN}	−1080			mV
			$T_A = +25°C$	applied to D_1 and D_2 inputs and V_{IHMAX} applied to all other inputs. For $\overline{Q}_0$ output, apply V_{ILT} to D_0 input	−980			mV
			$T_A = +85°C$	with V_{ILMIN} applied to D_1 and D_2 and V_{IHMAX} applied to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_1 output apply V_{ILT} to D_0 input with V_{ILMIN}			−1655	mV
			$T_A = +25°C$	applied to D_1 and D_2 inputs and V_{IHMAX} applied to all other inputs. For $\overline{Q}_0$ output, apply V_{IHT} to D_0 input			−1630	mV
			$T_A = +85°C$	with V_{ILMIN} applied to D_1 and D_2 and V_{IHMAX} applied to all other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_1 output, apply V_{ILMIN}	−2000		−1675	mV
			$T_A = +25°C$	to all inputs. For $\overline{Q}_0$ output	−1990		−1650	mV
			$T_A = +85°C$	apply V_{IHMAX} to all inputs.	−1920		−1615	mV
I_{IH}	High level input current	D_5 input	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			495	µA
			$T_A = +25°C$				310	µA
			$T_A = +85°C$				310	µA
		All other inputs	$T_A = -30°C$				390	µA
			$T_A = +25°C$				245	µA
			$T_A = +85°C$				245	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				29	mA
			$T_A = +25°C$			20	26	mA
			$T_A = +85°C$				29	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_0$, Q_1	Waveform 1	1.40 1.40	3.90 3.90	1.40 1.40	2.30 2.30	3.40 3.40	1.40 1.40	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		0.90 0.90	4.10 4.10	1.10 1.10	2.50 2.50	4.00 4.00	1.10 1.10	4.60 4.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

Document No.	853–0656
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10123
Bus Driver

Triple 4-3-3-Input Bus Driver

FEATURES

- **Typical propagation delay: 3.0ns**
- **Typical supply current ($-I_{EE}$): 71mA**

DESCRIPTION

The 10123 consists of three NOR Gates for use as Drivers. Each can drive a bus with characteristic impedance of not less than 25Ω, such as the case of a bus terminated at both ends in 50Ω. When the output is Low it presents a high impedance to the bus so that its characteristic impedance is not reduced. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

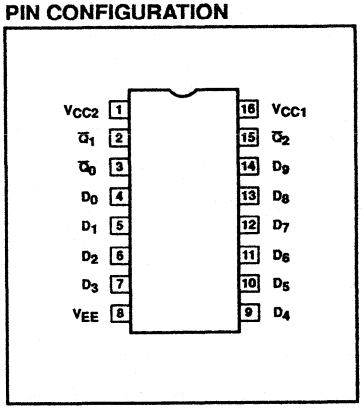
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10123N
16–Pin Ceramic DIP	10123F

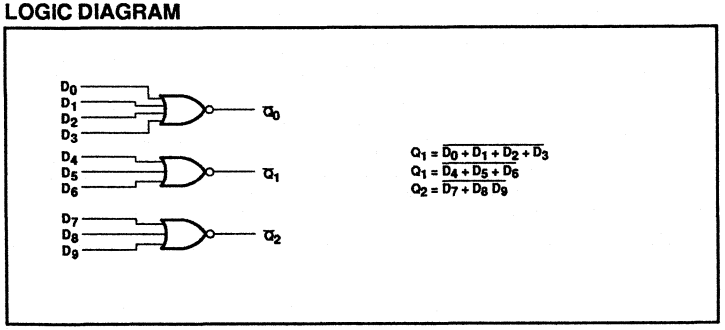
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_9$	Data Inputs
$\overline{Q}_0 - \overline{Q}_2$	Data Outputs

PIN CONFIGURATION

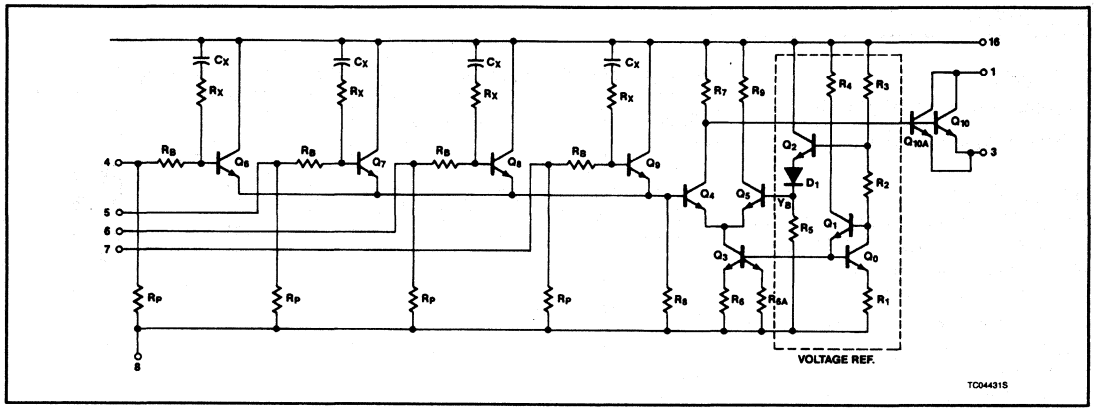


LOGIC DIAGRAM



Bus Driver 10123

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading with 25Ω to $-2.1V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Apply V_{ILMIN} to all inputs.	-1060		-890	mV
		$T_A = +25°C$		-960		-810	mV
		$T_A = +85°C$		-890		-700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{ILT} to one input of each	-1080			mV
		$T_A = +25°C$	gate, one at a time, with V_{ILMIN}	-980			mV
		$T_A = +85°C$	applied to all other inputs.	-910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Apply V_{ILT} to one input of each			-2010	mV
		$T_A = +25°C$	gate, one at a time, with V_{ILMIN}			-2010	mV
		$T_A = +85°C$	applied to all other inputs.			-2010	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to all inputs.	-2100		-2030	mV
		$T_A = +25°C$		-2100		-2030	mV
		$T_A = +85°C$		-2100		-2030	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under			350	µA
		$T_A = +25°C$	test, one at a time, with V_{ILMIN}			220	µA
		$T_A = +85°C$	applied to all other inputs.			220	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under	0.5			µA
		$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
		$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$	Apply V_{IHMAX} to all inputs.			82	mA
		$T_A = +25°C$			71	75	mA
		$T_A = +85°C$				82	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

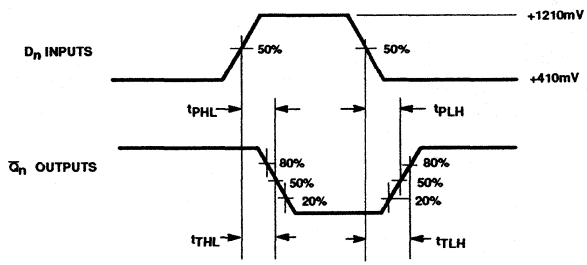
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 1	1.20 1.20	4.60 4.60	1.20 1.20	3.00 3.00	4.40 4.40	1.20 1.20	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	3.70 3.70	1.00 1.00	2.50 2.50	3.50 3.50	1.00 1.00	3.90 3.90	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

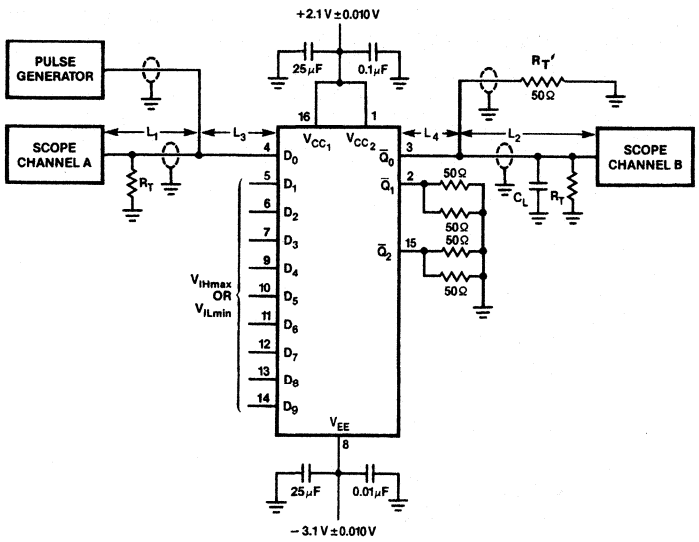
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Bus Driver 10123

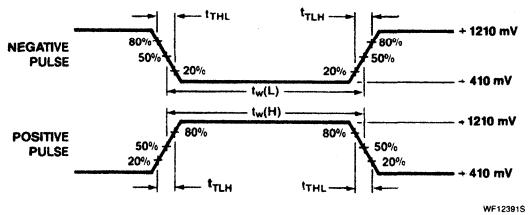
AC TEST CIRCUIT



NOTES:

1. $V_{CC1} = V_{CC2} = +2.1V \pm 0.010V$, $V_{EE} = -3.1V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to V_{CC}. 0.01μF and 25μF from GND to V_{EE}. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 25Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3 and L_4, the distance from the DUT input and output pins to the junction of their respective interconnecting cables, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope. $R_T' = 50\Omega$ termination resistor at the end of a 50Ω impedance line, the length of which is irrelevant but should be kept as short as possible to reduce stray capacitance.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS
$V_{CC1} = V_{CC2} = +2.1V \pm 0.010V$, $V_{EE} = -3.1V \pm 0.010V$, V_T = GND (0V)

Family	Amplitude	Rep Rate	Pulse Width	t_{TLH}	t_{THL}
10K ECL	800mVp-p	1MHz	500ns	2.0 ±0.2ns	2.0 ±0.2ns

Philips Components

Document No.	853–0657
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10124
Translator

Quad TTL-to-ECL Translator

FEATURES

- **Typical propagation delay: 3.5ns**
- **Typical supply current ($-I_{EE}$): 53mA**

DESCRIPTION

The 10124 is a Quad TTL-ECL Translator with an individual Data and Common Select TTL-compatible input on each gate. When the Select input is in the LOW State, all ECL non-inverting outputs are in a LOW State and inverting inputs are in a HIGH State.

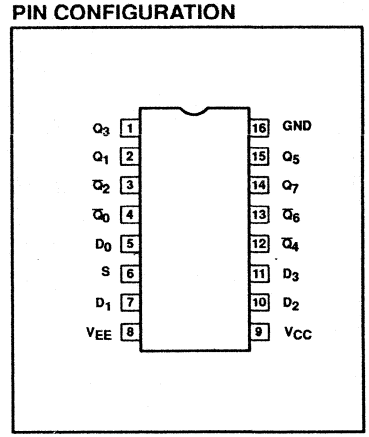
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10124N
16–Pin Ceramic DIP	10124F
16–Pin SO	10124D

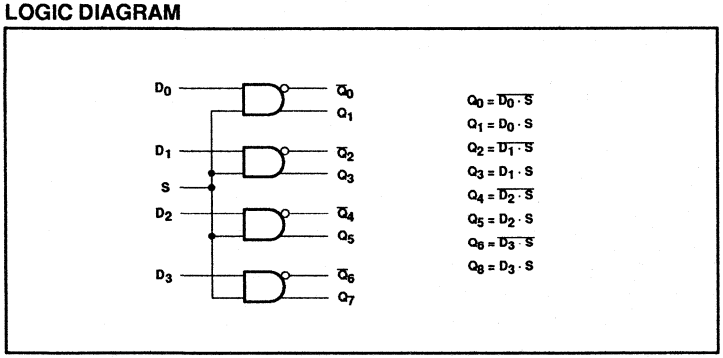
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs (Schottky TTL)
S	Select Input (Schottky TTL)
Q_1, Q_3, Q_5, Q_7	Data Outputs (AND) (10K ECL)
$\overline{Q}_0, \overline{Q}_2, \overline{Q}_4, \overline{Q}_6$	Data Outputs (NAND) (10K ECL)

PIN CONFIGURATION

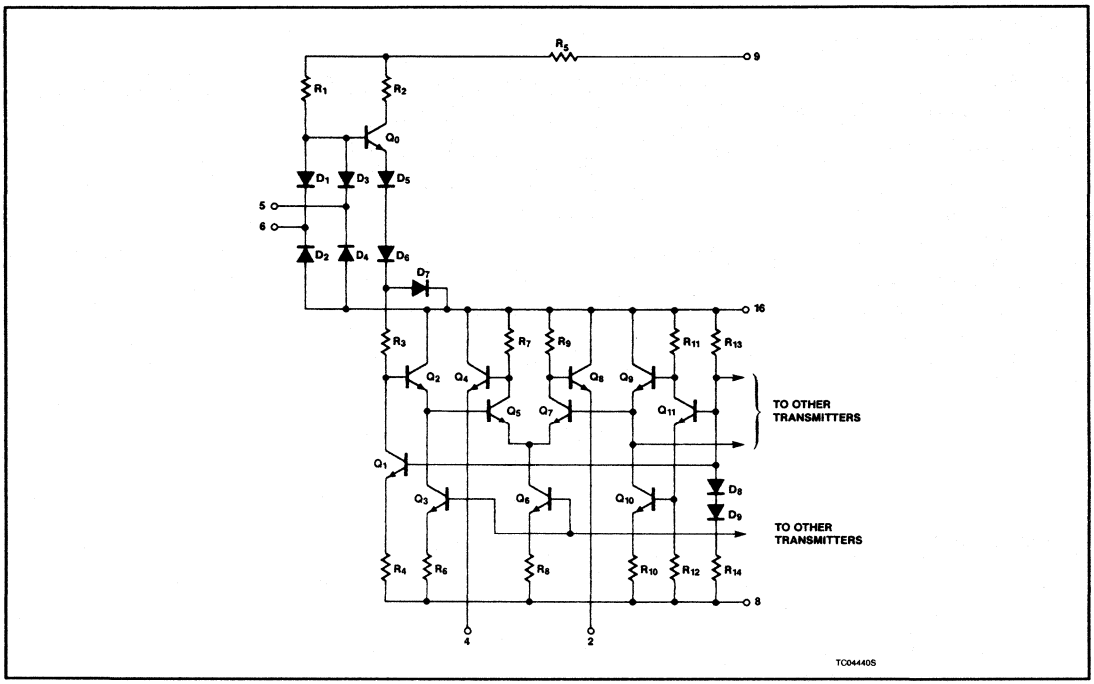


LOGIC DIAGRAM



Translator 10124

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage (negative)		–8.0	V
V_{CC}	Supply voltage (positive)		+7.0	V
V_{IN}	Input voltage		0 to V_{CC}	V
I_{IN}	Input current		–30 to +5.0	mA
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
GND	Device ground (common)		0	0	0	V
V_{CC}	Supply voltage (positive)			5.0		V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C	2.0		4.0	V
		T_A = +25°C	1.8		4.0	V
		T_A = +85°C	1.8		4.0	V
V_{IHT}	High level input threshold voltage	T_A = –30°C	2.0			V
		T_A = +25°C	1.8			V
		T_A = +85°C	1.8			V
V_{ILT}	Low level input threshold voltage	T_A = –30°C			1.1	V
		T_A = +25°C			1.1	V
		T_A = +85°C			0.9	V
V_{IL}	Low level input voltage	T_A = –30°C	0.4		1.1	V
		T_A = +25°C	0.4		1.1	V
		T_A = +85°C	0.4		0.8	V
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

GND = ground, V_{CC} = +5.0V ± 0.010V, V_{EE} = –5.2V ± 0.010V, T_A = –30°C to +85°C output loading 50Ω to –2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		T_A = –30°C	For Q_n outputs, apply V_{IHMAX}	–1060		–890	mV
			T_A = +25°C	to all inputs. For $\overline{Q}_n$ outputs apply	–960		–810	mV
			T_A = +85°C	V_{ILMIN} to all inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage		T_A = –30°C	For Q_n outputs, apply V_{IHT} to D_1 input with	–1080			mV
			T_A = +25°C	V_{IHMAX} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{ILT} to D_1 input with V_{IHMAX} applied to	–980			mV
			T_A = +85°C	all other inputs.	–910			mV
V_{OLT}	Low level output threshold voltage		T_A = –30°C	For Q_n outputs, apply V_{ILT} to D_1 input with			–1655	mV
			T_A = +25°C	V_{IHMAX} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to D_1 input with V_{IHMAX} applied to			–1630	mV
			T_A = +85°C	all other inputs.			–1595	mV
V_{OL}	Low level output voltage		T_A = –30°C	For Q_n outputs, apply V_{ILMIN}	–1890		–1675	mV
			T_A = +25°C	to all inputs. For $\overline{Q}_n$ outputs apply	–1850		–1650	mV
			T_A = +85°C	V_{IHMAX} to all inputs.	–1825		–1615	mV
$-I_{EE}$	V_{EE} supply current		T_A = –30°C				72	mA
			T_A = +25°C	Apply V_{IHMAX} to all inputs.		53	66	mA
			T_A = +85°C				72	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		T_A = +25°C			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V
V_{IK}	Clamp input voltage	S input	Apply –20mA to S input.				–1.5	V
		other inputs	Apply –10mA to each input under test, one at a time.				–1.5	
V_{BIN}	Input breakdown voltage		Apply 1.0mA to each input under test, one at a tme		5.5			V
I_F	Forward current	S input	Apply VF(0.4.0V) to S input and VR(2.4V) to all other inputs.				–12.8	mA
		other inputs	Apply VF(0.4.0V) to each input under test, one at a time, with VR(2.4V) applied to all other inputs.				–3.2	mA
I_R	Reverse current	S input	Apply VR(2.4V) to S input with VF(0.4V) to all other inputs.				200	µA
		other inputs	Apply VR(2.4V) to each input under test, one at a time, with VF(0.4V) applied to all other inputs.				50	µA
I_{CCH}	High level output voltage		T_A = –30°C				16	mA
			T_A = +25°C	Apply V_{IHMAX} to all inputs.			16	mA
			T_A = +85°C				18	mA
I_{CCL}	Supply current Low (positive)		Ground all inputs.				25	mA

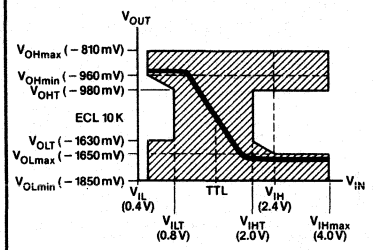
NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

Translator

10124

TRANSFER CHARACTERISTICS



NOTES:

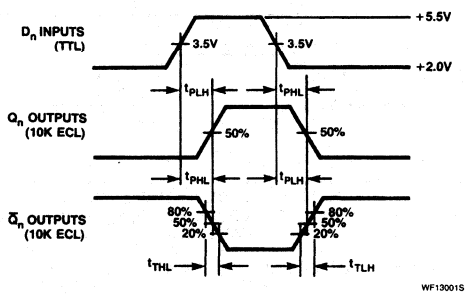
V_{IHmax} – Maximum HIGH level input voltage (the most positive V_{IH}).
V_{IHT} – HIGH level input threshold voltage.
V_{ILT} – LOW level input threshold voltage.
V_{ILmin} – Minimum LOW level input voltage (the most negative V_{IL}).
V_{OHmax} – Maximum HIGH level output voltage (the most positive V_{OH}) under the specified input and loading condition.
V_{OHmin} – Minimum HIGH level output voltage (the most negative V_{OH}) under the specified input and loading condition.
V_{OHT} – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
V_{OLT} – LOW level output threshold voltage with the inputs set to their respective threshold levels.
V_{OLmax} – Maximum LOW level output voltage (the most positive V_{OL}) under the specified input and loading conditions.
V_{OLmin} – Minimum LOW level output voltage (the most negative V_{OL}) under the specified input and loading conditions.
V_{BB} – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

AC ELECTRICAL CHARACTERISTICS GND = ground, V_{CC} = 5.0V ± 0.010V, V_{EE} = −5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = −30°C		T_A = +25°C			T_A = +85°C		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH}	Propagation delay	Waveform 1	1.00	6.50	1.00	3.50	6.00	1.00	6.50	ns
t_{PHL}	D_n to Q_n, $\overline{Q}_n$		1.00	6.50	1.00	3.50	6.00	1.00	6.50	ns
t_{TLH}	Transition time		1.30	4.10	1.30	2.50	3.90	1.30	4.10	ns
t_{THL}	20% to 80%, 80% to 20%		1.30	4.10	1.30	2.50	3.90	1.30	4.10	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

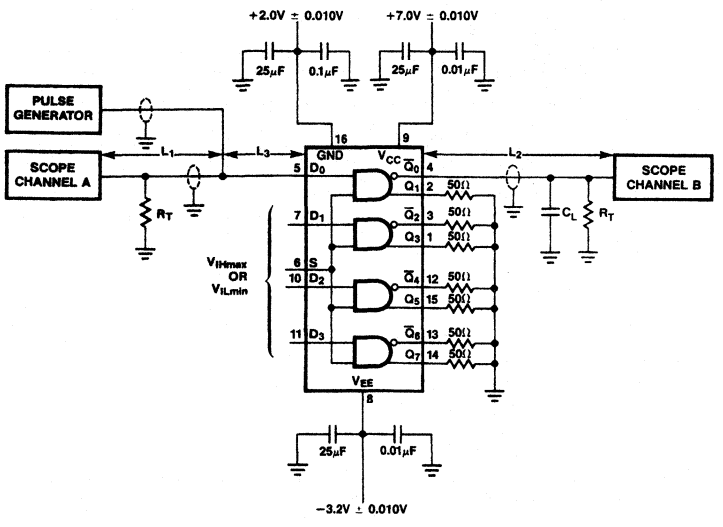
AC WAVEFORMS



Waveform 1. Propagation Delay and Transitions Times

Translator 10124

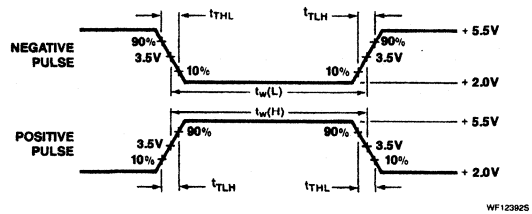
AC TEST CIRCUIT



NOTES:

1. GND = +2.0V ±0.010V, V_{CC} = +7.0V ±0.010V, V_{EE} = −3.2V + 0.010V.
2. Decoupling 0.1μF and 25μF from GND to Sys. Gnd., 0.01μF and 25μF from V_{CC} to Sys. Gnd. and from V_{EE} to Sys. Gnd. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to Sys. Gnd.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. R_T = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance < 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS GND = +2.0V ± 0.010V, V_{CC} = +7.0V ± 0.010V, V_{EE} = −3.2V ± 0.010V, V_T = SYS. Gnd.(0V)					
Family	**Amplitude**	**Rep Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
TTL	$3.5V_{P-P}$	1MHz	500ns	2.0 ± 0.2ns	2.0 ± 0.2ns

Document No.	853–0658
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10125
Gate

Quad ECL-to-TTL Translator

FEATURES

- **Typical propagation delay: 3.5ns**
- **Typical supply current ($-I_{EE}$): 30mA**

DESCRIPTION

The 10125 is a Quad ECL-to-TTL Translator for interfacing data between two different logic systems. It also provides a separate Reference Bias Voltage output (V_{BB}) to be used in case of single-ended input busing. Input and output levels are, respectively, ECL 10K and TTL Schottky. This device features a peak common-mode rejection voltage of ± 1V.

The 10125 outputs are designed to go to a Low logic level whenever both inputs are left open.

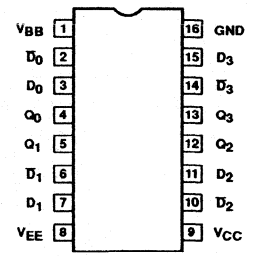
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10125N
16–Pin Ceramic DIP	10125F
16–Pin SO	10125D

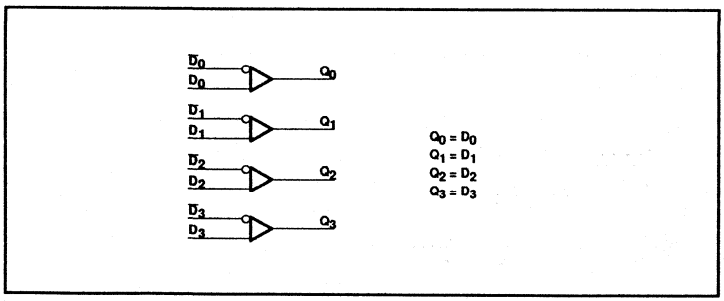
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$, $\overline{D}_0 - \overline{D}_3$	Data Inputs (ECL 10K)
V_{BB}	Reference Bias Voltage Output (ECL 10K)
$Q_0 - Q_3$	Data Outputs (Schottky TTL)

PIN CONFIGURATION

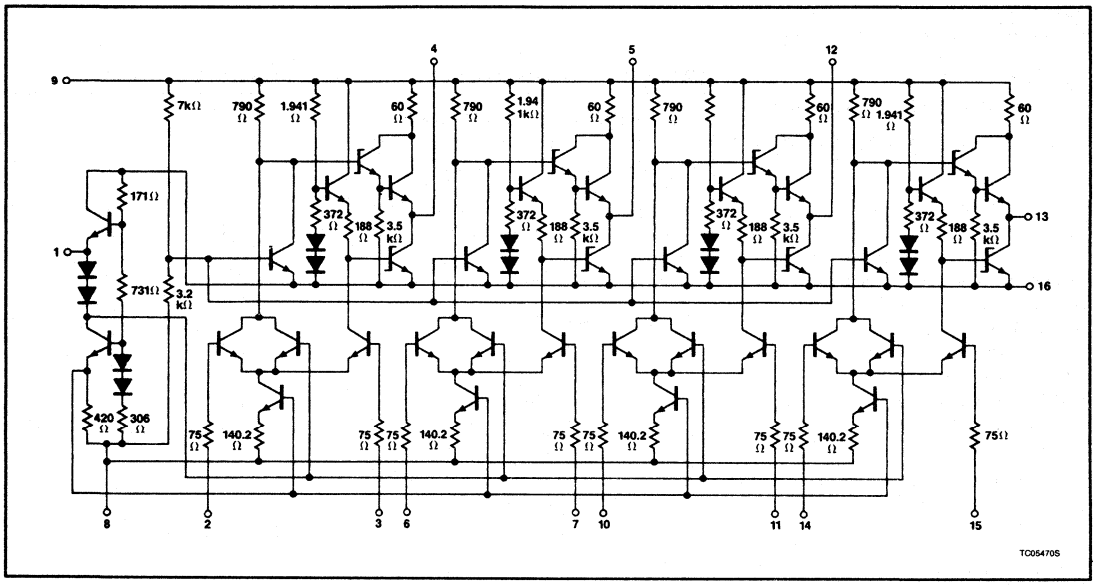


LOGIC DIAGRAM



Gate 10125

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage (negative)		–8.0	V
V_{CC}	Supply voltage (positive)		+7.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		+0.5 to V_{EE}	V
V_{OUT}	Voltage applied to output in High–State		–0.5 to +V_{CC}	V
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
GND	Device ground (common)		0	0	0	V
V_{CC}	Supply voltage (positive)			+5.0		V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C	1.8		–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC OPERATING CONDITIONS FOR COMMON–MODE REJECTION TEST

GND = ground, V_{CC} = +5.0V ± 0.010V, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{IHH}	V_{IHMAX} +1.0V	T_A = –30°C			+110	mV
		T_A = +25°C			+190	mV
		T_A = +85°C			+300	mV
V_{IHL}	V_{IHMAX} –1.0V	T_A = –30°C			–1890	mV
		T_A = +25°C			–1810	mV
		T_A = +85°C			–1700	mV
V_{ILH}	V_{ILMIN} +1.0V	T_A = –30°C	–890			mV
		T_A = +25°C	–850			mV
		T_A = +85°C	–825			mV
V_{ILL}	V_{ILMIN} –1.0V	T_A = –30°C	–2890			mV
		T_A = +25°C	–2850			mV
		T_A = +85°C	–2825			mV

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

GND = ground, V_{CC} = +5.0V ± 0.010V, V_{EE} = –5.2V ± 0.010V, T_A = –30°C to +85°C unless otherwise specified[1,4]

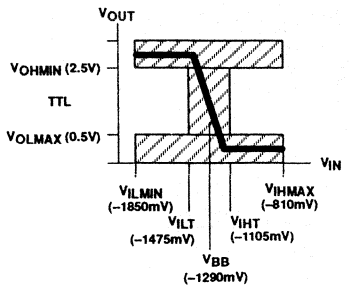
SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Apply V_{IHMAX} to all non–inverting inputs with V_{BB} applied to all inverting inputs. Force –2.0mA on measureed output.[5]		2.5			V
V_{OL}	Low level output voltage	Apply V_{ILMIN} to all non–inverting inputs with V_{BB} applied to all inverting inputs. Force 20mA on measureed output.[5]				0.5	V
V_{OH}	High level output voltage for CMR test	Apply V_{IHH} to D_n and V_{ILH} to $\overline{D}_n$ inputs. Apply V_{IHL} to D_n and V_{ILL} to $\overline{D}_n$ inputs. Force –2.0mA on measured output.		2.5			V
V_{OL}	Low level output voltage for CMR test	Apply V_{IHH} to $\overline{D}_n$ and V_{ILH} to D_n inputs. Apply V_{IHL} to $\overline{D}_n$ and V_{ILL} to D_n inputs. Force +20mA on measured output.				0.5	V
V_{OLS1}	Indeterminate input protection test	Apply V_{EE} to all inputs. Force 20mA on measured output.				0.5	V
V_{OLS2}	Indeterminate input protection test	All inputs left floating. Force 20mA on measured output.				0.5	V
V_{BB}	Reference bias voltage	T_A = –30°C	Connect all inverting inputs to	–1420		–1280	mV
		T_A = +25°C	V_{BB} pin during test. All other	–1350	–1290	–1230	mV
		T_A = +85°C	inputs are not connected.	–1295		–1150	mV
I_{IH}	High level input current	T_A = –30°C	Apply V_{IHMAX} to each input under			180	µA
		T_A = +25°C	test, one at a time, with V_{ILMIN}			115	µA
		T_A = +85°C	applied to all other inputs.			115	µA
$-I_{CBO}$	Input leakage current	T_A = –30°C	Apply V_{EE} to each inverting input under test, one at			1.5	µA
		T_A = +25°C	at time, with V_{ILMIN} applied to all other inverting			1.0	µA
		T_A = +85°C	inputs and V_{BB} applied to all non–inverting inputs.[5]			1.0	µA
$-I_{EE}$	V_{EE} supply current	T_A = –30°C	Apply V_{BB} to all $\overline{D}_n$ inputs and V_{ILMIN} to all D_n inputs.			44	mA
		T_A = +25°C			30	40	mA
		T_A = +85°C				44	mA
$-I_{OS}$	Short circuit current[4]	T_A = –30°C	Apply V_{ILMIN} to all $\overline{D}_n$ input with V_{BB} applied	40		100	mA
		T_A = +25°C	to all D_n inputs. Test each output one at a time, with all other outputs unloaded.	40		100	mA
		T_A = +85°C	Force 0V (GND) on measured output.[4]	40		100	mA
I_{CCH}	Supply current output High	Apply V_{ILMIN} to all $\overline{D}_n$ inputs with V_{BB} applied to D_n inputs.				52	mA
I_{CCL}	Supply current output Low	Apply V_{IHMAX} to all $\overline{D}_n$ inputs with V_{BB} applied to D_n inputs.				39	mA
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation	T_A = +25°C			0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high–speed test apparatus and/or sample–and–hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. Refer to DC Test Circuit.

Gate 10125

TRANSFER CHARACTERISTICS



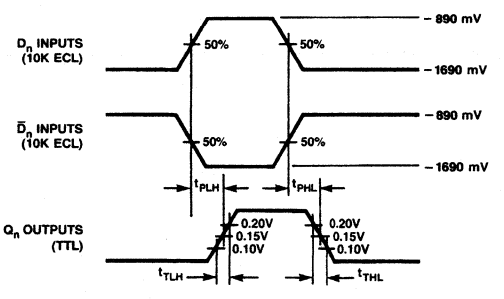
NOTES:
V_{IHMAX} = Maximum HIGH level input voltage (the most positive V_{IH}).
V_{IHT} = HIGH level input threshold voltage.
V_{ILT} = LOW level input threshold voltage.
V_{ILMIN} = Minimum LOW level input voltage (the most negative V_{IL}).
V_{OHMIN} = Minimum HIGH level output voltage (the most negative V_{OH}) under the specified input and loading condition.
V_{OLMAX} = Maximum LOW level output voltage (the most positive V_{OL}) under the specified input and loading conditions.
V_{BB} = Reference Bias Voltage. The internally generated reference voltage which is used to set the input and output threshold level.

AC ELECTRICAL CHARACTERISTICS GND = 0V, V_{CC} = +5.0V ± 0.010V, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = –30°C		T_A = +25°C			T_A = +85°C		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	6.00 6.00	1.00 1.00	4.50 4.50	6.00 6.00	1.00 1.00	6.00 6.00	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		0.50 0.50	3.30 3.30	0.50 0.50		3.30 3.30	0.50 0.50	3.30 3.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS

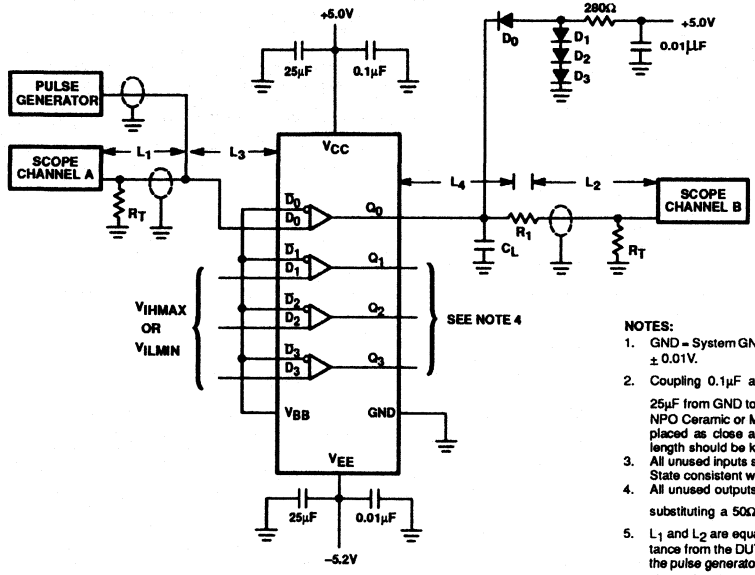


NOTE:
The output waveform in Waveform 1 is shown with the actual output voltages of the AC Test Circuit which are attenuated by a factor of 10 as a result of the voltage divider formed by the 450Ω resistor and R_T.

Waveform 1. Propagation Delay and Transition Times

Gate | 10125

AC TEST CIRCUIT

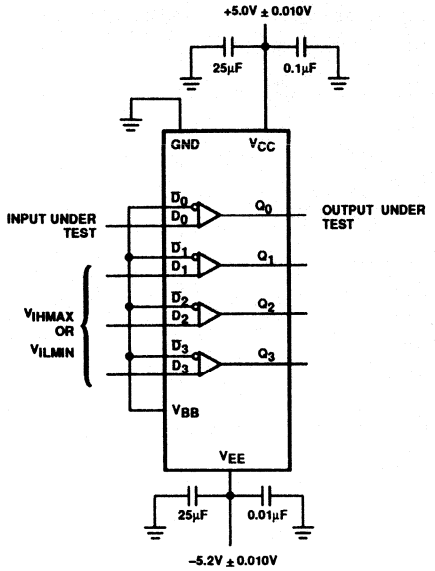


NOTES:

1. GND = System GND (0V), V_{CC} = +5.0V ±0.010V, V_{EE} = −5.2V ± 0.01V.
2. Coupling 0.1μF and 25μF from GND to V_{CC}, 0.01μF and 25μF from GND to V_{EE} (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either High– or Low–State consistent with the Logic function required.
4. All unused outputs are loaded identically to output under test, substituting a 50Ω termination for the scope.
5. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the distance from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm). L_4, the lead length from the DUT output pin to R_1 and D_1, should not exceed 1/4 inch.
6. R_T = 50Ω termination internal to scope. R_1 = 450Ω.
7. C_L = 25pf including fixture and stray capacitance (not including scope cable capacitance).
8. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section AC setup procedure).
9. D_1 through D_4 are High Frequency (low capacitance) switching diodes.

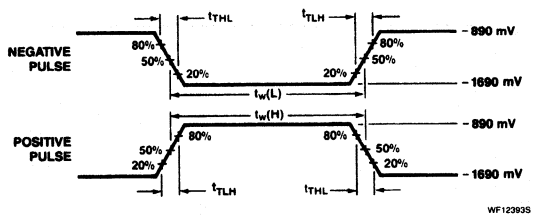
Gate 10125

DC TEST CIRCUIT



NOTES:
1. GND = System GND (0V). V_{CC} = +5.0V ±0.010V, V_{EE} = −5.2V ± 0.01V.
2. Coupling 0.1μF and 25μF from GND to V_{CC}, 0.01μF and 25μF from GND to V_{EE} (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either High– or Low–State consistent with the Logic function required.
4. All unused outputs are open.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS
GND = 0V, V_{CC} = +5.0V ±0.010V, V_{EE} = -5.2V ±0.010V, V_T = GND (0V)

Family	Amplitude	Rep Rate	Pulse Width	t_{TLH}	t_{THL}
10K ECL	800mVp-p	1MHz	500ns	2.0 ±0.2ns	2.0 ±0.2ns

Philips Components

Document No.	853–1436
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10129
Line Receiver

Quad TTL-to-ECL Translator

FEATURES

- **Typical propagation delay: 10.0ns**
- **Typical TTL supply current (I_{CC}): 3.0mA**
- **Typical ECL supply current ($-I_{EE}$): 144mA**

DESCRIPTION

The 10129 is intended to allow interfacing of 10K family types with other logic devices or systems. The enable, reset and strobe inputs are compatible with 10K family logic levels whereas data inputs accept TTL logic levels compatible with IBM-type busses. The information received from the bus is stored temporarily in latch storage elements.

The strobe input is useful to provide accurate synchronization of signals and/or connection to 10K family type level busses. When the enable is Low, the reset input is disabled and the outputs will follow the data inputs. The latches store data when the enable goes High. Unused data inputs must be tied to V_{CC} or ground. On the other hand, enable, strobe and reset inputs must be tied to V_{IL} or V_{EE} if unused.

The outputs are enabled when the strobe input is High. Two modes of operation are provided. In the first mode, obtained by tying the hysteresis control input to V_{EE}, the input threshold points of the D inputs are fixed. In the second mode this hysteresis control input is connected to ground which gives an hysteresis input effect useful for increasing the D input noise margin.

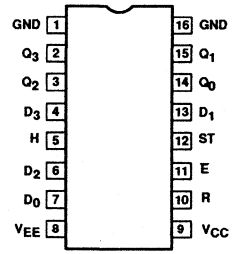
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10129N
16–Pin Ceramic DIP	10129F

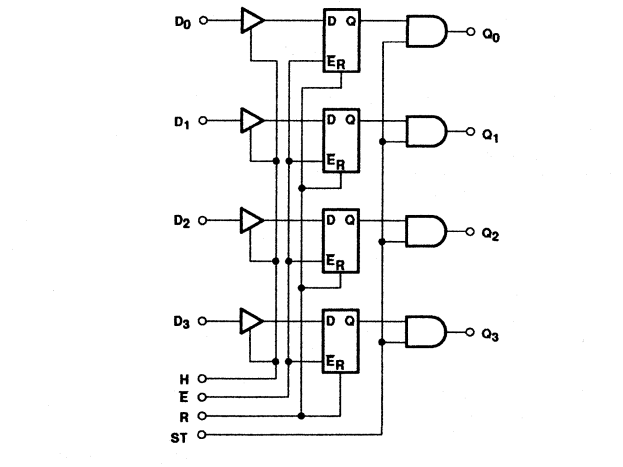
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
H	Hysteresis control Input
$\overline{E}$	Enable Input
R	Reset Input
ST	Strobe Input
$Q_1 - Q_3$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Line Receiver | 10129

FUNCTION TABLE

INPUTS				OUTPUT
D_n	$\overline{E}$	ST	R	Q_{n+1}
X	X	L	X	L
X	H	X	H	L
L	L	H	X	H
X	H	H	L	Q_n
H	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS FOR ECL–COMPATIBLE LINES

SYMBOL	PARAMETER		LIMIT	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

ABSOLUTE MAXIMUM RATINGS FOR TTL–COMPATIBLE LINES

SYMBOL	PARAMETER	LIMIT	UNIT
V_{CC}	TTL supply voltage	–5.0 to +7.0	V
V_{IN}	Input voltage	–0.5 to V_{TTL}	V
I_{IN}	Input current	–30 to +5	mA

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS FOR ALL INPUT LEVELS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	NOM.	MAX.	
GND	Circuit ground	0	0	0	V
V_{EE}	ECL supply voltage		–5.2		V
V_{CC}	TTL supply voltage		+5.0		V
T_A	Operating ambient temperature range	–30	+25	+85	°C

NOTE:
When operating at V_{EE} other than specified voltage (–5.2V), the DC and AC Characteristics will vary slighly from specified values. (See table of DC Characteristics.)

DC OPERATING CONDITIONS FOR ECL INPUT LEVELS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{IH}	High level input voltage	$T_A = -30°C$			–890	mV
		$T_A = +25°C$			–810	mV
		$T_A = +85°C$			–700	mV
V_{IHT}	High level input threshold voltage	$T_A = -30°C$	–1205			mV
		$T_A = +25°C$	–1105			mV
		$T_A = +85°C$	–1035			mV
V_{ILT}	Low level input threshold voltage	$T_A = -30°C$			–1500	mV
		$T_A = +25°C$			–1475	mV
		$T_A = +85°C$			–1440	mV
V_{IL}	Low level input voltage	$T_A = -30°C$	–1890			mV
		$T_A = +25°C$	–1850			mV
		$T_A = +85°C$	–1825			mV

DC OPERATING CONDITIONS FOR TTL INPUT LEVELS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{IH}	High level input voltage	$T_A = -30°C$	3.000			V
		$T_A = +25°C$	3.000			V
		$T_A = +85°C$	3.000			V
V_{IHT}'	High level input threshold voltage	$T_A = -30°C$	2.000			V
		$T_A = +25°C$	2.000			V
		$T_A = +85°C$	2.000			V
V_{ILT}'	Low level input threshold voltage	$T_A = -30°C$			0.800	V
		$T_A = +25°C$			0.800	V
		$T_A = +85°C$			0.800	V
V_{IL}	Low level input voltage	$T_A = -30°C$			0.400	V
		$T_A = +25°C$			0.400	V
		$T_A = +85°C$			0.400	V

Line Receiver | 10129

DC OPERATING CONDITIONS FOR IBM INPUT LEVELS

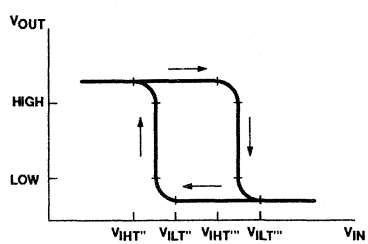
SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{IH}	High level input voltage	$T_A = -30°C$	3.110			V
		$T_A = +25°C$	3.110			V
		$T_A = +85°C$	3.110			V
V_{IHT}'	High level input threshold voltage	$T_A = -30°C$				V
		$T_A = +25°C$	1.700			V
		$T_A = +85°C$				V
V_{ILT}'	Low level input threshold voltage	$T_A = -30°C$				V
		$T_A = +25°C$			0.700	V
		$T_A = +85°C$				V
V_{IL}	Low level input voltage	$T_A = -30°C$			0.150	V
		$T_A = +25°C$			0.150	V
		$T_A = +85°C$			0.150	V

DC OPERATING CONDITIONS FOR HYSTERESIS MODE THRESHOLD VOLTAGES

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{IHT}''	Hysteresis mode High level input threshold voltage	$T_A = -30°C$	2.900			V
		$T_A = +25°C$	2.600			V
		$T_A = +85°C$	2.300			V
V_{ILT}''	Hysteresis mode Low level input threshold voltage	$T_A = -30°C$			2.000	V
		$T_A = +25°C$			1.700	V
		$T_A = +85°C$			1.400	V
V_{IHT}'''	Hysteresis mode High level input threshold voltage	$T_A = -30°C$	2.200			V
		$T_A = +25°C$	1.900			V
		$T_A = +85°C$	1.600			V
V_{ILT}'''	Hysteresis mode Low level input threshold voltage	$T_A = -30°C$			1.300	V
		$T_A = +25°C$			1.000	V
		$T_A = +85°C$			0.700	V

NOTE:
V_{IH}'', V_{IL}'', V_{IH}''' and V_{IL}''' are logic "1" and "0" threshold voltages in the hystersis mode.

HYSTERSIS MODE THRESHOLD VOLTAGES



DC ELECTRICAL CHARACTERISTICS

GND = ground, V_{EE} = –5.2V ± 0.010V, V_{CC} = +5.0V ± 0.010V, T_A = –30°C to +85°C output loading 50Ω to –2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		T_A = –30°C	ST = V_{IHMAX}, $\overline{E}$ = V_{ILMIN}, R = V_{ILMIN}	–1060		–890	mV
			T_A = +25°C		–960		–810	mV
			T_A = +85°C		–890		–700	mV
V_{OHT}	High level output threshold voltage		T_A = –30°C	ST = V_{IHMAX}, $\overline{E}$ = V_{ILMIN}, R = V_{ILMIN}	–1080			mV
			T_A = +25°C		–980			mV
			T_A = +85°C		–910			mV
V_{OLT}	Low level output threshold voltage		T_A = –30°C	ST = V_{IHMAX}, $\overline{E}$ = V_{ILMIN}, R = V_{ILMIN}			–1655	mV
			T_A = +25°C				–1630	mV
			T_A = +85°C				–1595	mV
V_{OL}	Low level output voltage		T_A = –30°C	ST = V_{IHMAX}, $\overline{E}$ = V_{ILMIN}, R = V_{ILMIN}	–1890		–1675	mV
			T_A = +25°C		–1850		–1650	mV
			T_A = +85°C		–1825		–1615	mV
I_{IH}	High level input current	D_n inputs	T_A = –30°C				150	µA
			T_A = +25°C				95	µA
			T_A = +85°C				95	µA
		R input	T_A = –30°C	$\overline{E}$ = R = V_{ILMAX}			720	µA
			T_A = +25°C				450	µA
			T_A = +85°C				450	µA
		$\overline{E}$, ST inputs	T_A = –30°C	$\overline{E}$ or ST = V_{IHMAX}			390	µA
			T_A = +25°C				245	µA
			T_A = +85°C				245	µA
$-I_{CBO}$	Input leakage current	D_n inputs	T_A = –30°C	Apply V_{EE} to H one D_n = V_{IL} (TTL or IBM) at a time.			1.5	µA
			T_A = +25°C				1.0	µA
			T_A = +85°C				1.0	µA
I_{IL}	Low level input current	R, $\overline{E}$, ST inputs	T_A = –30°C		0.5			µA
			T_A = +25°C		0.5			µA
			T_A = +85°C		0.3			µA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
$-I_{EE}$	ECL supply current	$T_A = -30°C$	Connect H to GND			167	mA
		$T_A = +25°C$	ST = V_{IHMIN}, $\overline{E}$ = V_{ILMIN}			152	mA
		$T_A = +85°C$				167	mA
		$T_A = -30°C$	Apply V_{EE} to H			189	mA
		$T_A = +25°C$	ST = V_{IHMIN}, $\overline{E}$ = V_{ILMIN}			172	mA
		$T_A = +85°C$				189	mA
I_{CC}	TTL supply current	$T_A = -30°C$				8.0	mA
		$T_A = +25°C$	Apply V_{EE} to H			8.0	mA
		$T_A = +85°C$				8.0	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

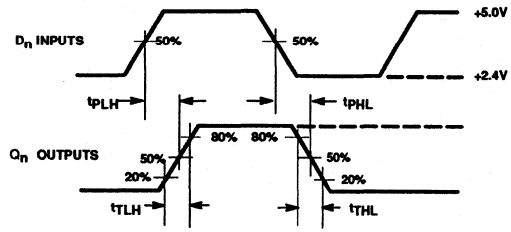
AC ELECTRICAL CHARACTERISTICS GND = ground, V_{EE} = –5.2V ± 0.010V, V_{CC} = +5.0V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS $T_A = -30°C$ MIN.	LIMITS $T_A = -30°C$ MAX.	LIMITS $T_A = +25°C$ MIN.	LIMITS $T_A = +25°C$ TYP.	LIMITS $T_A = +25°C$ MAX.	LIMITS $T_A = +85°C$ MIN.	LIMITS $T_A = +85°C$ MAX.	UNIT
t_{PLH}	Propagation delay without Hysteresis, D_n to Q_n	Connect H to V_{EE}, Waveform 1	3.7	15	3.7	10.0	15	3.7	30	ns
t_{PHL}			3.7	15	3.7	10.0	15	3.7	40	ns
t_{PLH}	Propagation delay with Hysteresis, D_n to Q_n	Connect H to GND, Waveform 1	6.6	30	6.7	18.0	25	6.6	30	ns
t_{PHL}			3.7	17	3.7	10.0	15	3.7	40	ns
t_{PLH}	Propagation delay $\overline{E}$ to Q_n	Waveforms 2, 4	2.7	11	2.7	5.0	9.0	2.7	11	ns
t_{PHL}			2.7	11	2.7	5.0	9.0	2.7	11	ns
t_{PLH}	Propagation delay ST to Q_n	Waveform 3	1.6	8.0	1.6	4.0	7.0	1.6	8.0	ns
t_{PHL}			1.6	8.0	1.6	4.0	7.0	1.6	8.0	ns
t_{PLH}	Propagation delay R to Q_n	Waveform 4	2.0	8.0	2.0	5.0	6.5	2.0	8.0	ns
t_{PHL}			2.0	8.0	2.0	5.0	6.5	2.0	8.0	ns
t_s	Setup time D_n to $\overline{E}$	Waveform 5	30		2.7	15.0		30		ns
t_h	Hold time D_n to $\overline{E}$	Waveform 5	0		–2.0	15.0		–2.0		ns
t_{TLH}	Transition time 20% to 80%, 80% to 20%	Waveforms 1, 2, 3, 4	1.5	5.0	1.5	2.0	4.3	1.5	5.0	ns
t_{THL}			1.5	5.0	1.5	2.0	4.3	1.5	5.0	ns

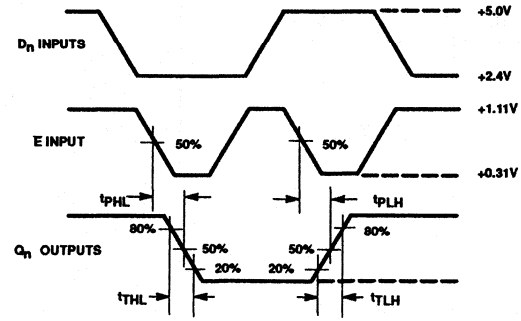
NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

Line Receiver 10129

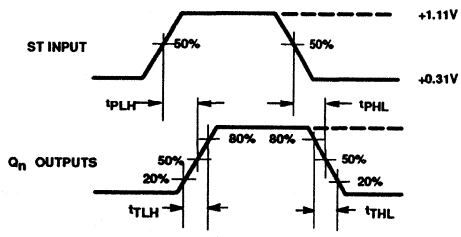
AC WAVEFORMS



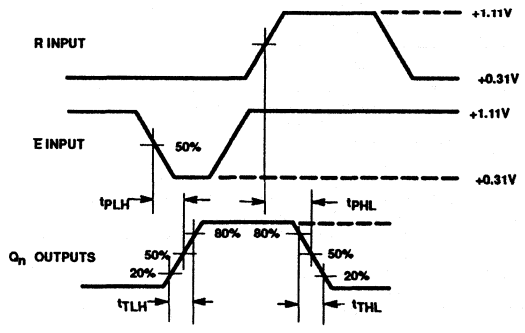
Waveform 1. D_n Timing ($\overline{E}$ and R are Low, ST is High)



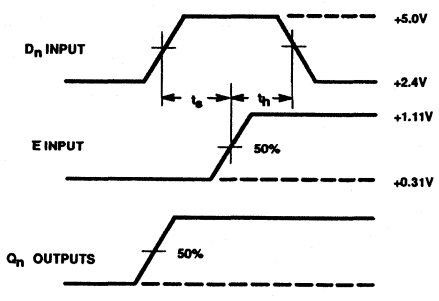
Waveform 2. D_n Timing (R is Low, ST is High)



Waveform 3. Strobe Timing ($\overline{E}$ and R are Low, D_n is High)



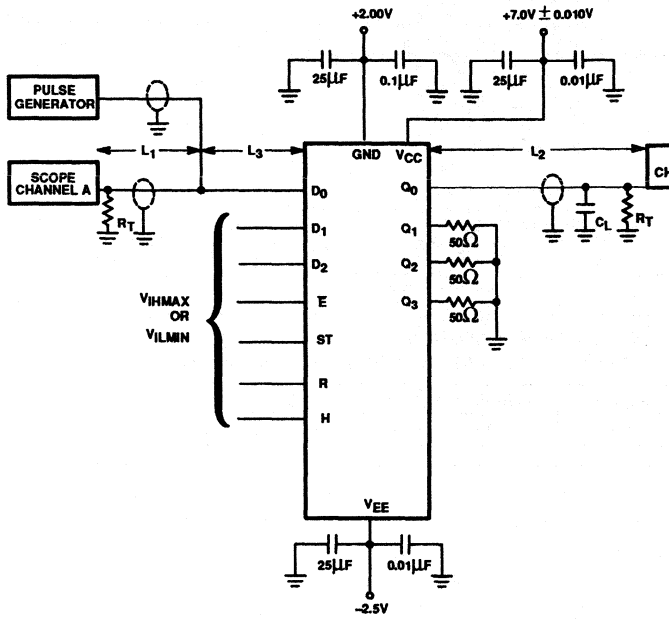
Waveform 4. Reset Timing (D_n and ST are High)



Waveform 5. Setup and Hold Times

Line Receiver | 10129

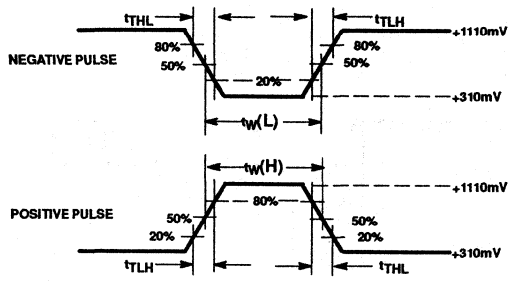
AC TEST CIRCUIT



NOTES:

1. GND =+2.0V ±0.010V, V_{CC} = + 7.0V ± 0.010V. V_{EE} = –3.2V ± 0.010V
2. Decoupling 0.1µF and 25µFfrom GND to system ground, 0.01µF and 25µF from V_{CC} to system ground (0.01µF and 0.1µF capacitors should be NPO Ceramic or MLC type). All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either a High or a Low state, consistent with the logic function required.
4. All unused outputs are loaded with 50Ω to system ground.
5. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
6. R_T = 50Ω termination internal to scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. Fixture and stray capacitance = $C_L \leq 3pF$.
9. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

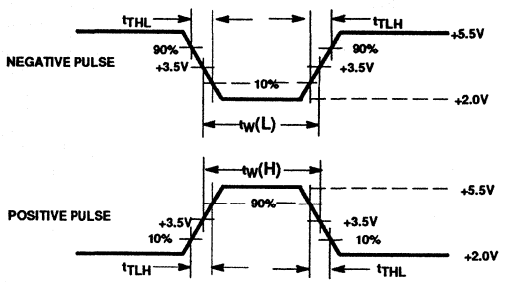
ECL INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS
GND = +2.0V± 0.010V, V_{CC} = +7.0V ± 0.010V, V_{EE} = –3.2V± 0.010V, V_T = 0V (system ground)

Family	Amplitude	Rep Rate	$t_{W(H)}$, $t_{W(L)}$	t_{TLH}	t_{THL}
10K ECL	800mV_{P-P}	1MHz	500ns	2.0 ± 0.2ns	2.0 ± 0.2ns

TTL INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS
GND = +2.0V ± 0.010V, V_{CC} = +7.0V ±0.010V, V_{EE} = –3.2V ±0.010V, V_T = 0V (system ground)

Family	Amplitude	Rep Rate	$t_{W(H)}$, $t_{W(L)}$	t_{TLH}	t_{THL}
TTL	3.0V_{P-P}	1MHz	500ns	2.5 ± 0.2ns	2.5 ± 0.2ns

Document No.	853–0659
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10130
Latch

Dual D-Type Latch

FEATURES

- **Typical propagation delay: 2.5ns**
- **Typical supply current ($-I_{EE}$): 30mA**

DESCRIPTION

The 10130 is a clocked Dual D-Type Latch. Each element can be clocked separately by holding the common clock in the Low-State and using the clock enable inputs for the clocking function. The outputs are latched when the level of the clock is High. All unused inputs must be tied to V_{IL} or V_{EE}.

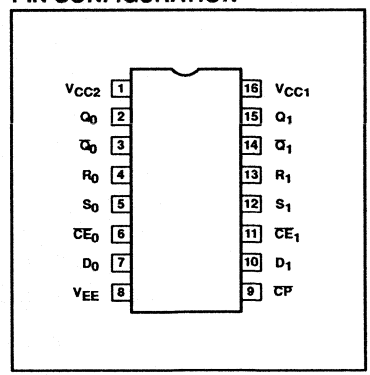
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10130N
16–Pin Ceramic DIP	10130F

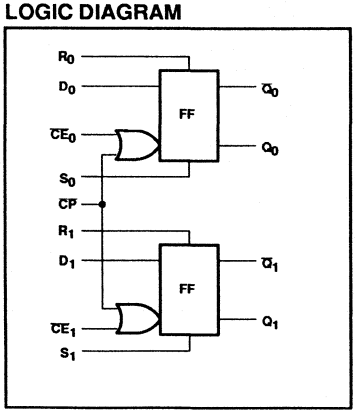
PIN DESCRIPTION

PINS	DESCRIPTION
D_0, D_1	Data Inputs
$\overline{CP}$	Clock Input
$\overline{CE}_0$, $\overline{CE}_1$	Clock Enable Inputs
S_0, S_1	Set Inputs
R_0, R_1	Reset Inputs
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data Outputs

PIN CONFIGURATION

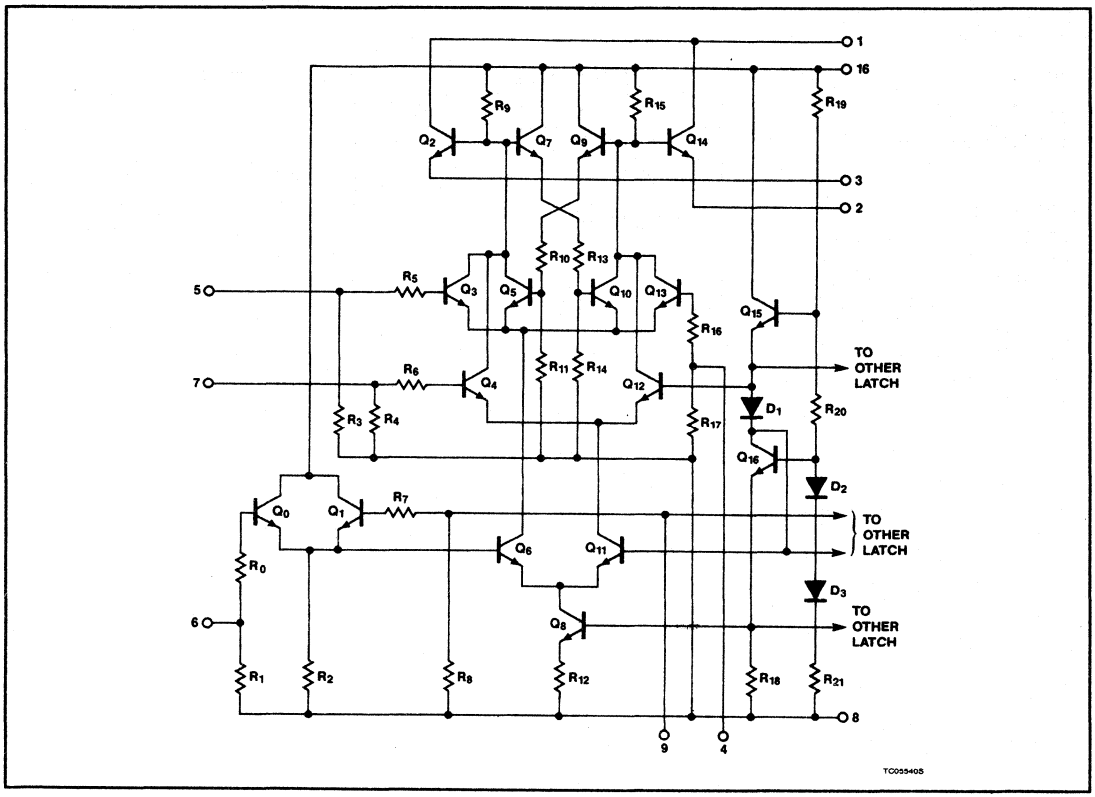


LOGIC DIAGRAM



Latch 10130

SIMPLIFIED SCHEMATIC



FUNCTION TABLES

SYNCHRONOUS OPERATION

INPUTS			OUTPUTS
D_n	$\overline{CP}$	$\overline{C}_E$	Q_{n+1}*
L	L	L	L
L	L	H	Q_n
L	H	L	Q_n
L	H	H	Q_n
H	L	L	H
H	L	H	Q_n
H	H	L	Q_n
H	H	H	Q_n

* R and S = Low

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS
R	S	Q_1
L	L	Q
L	H	H
H	L	L
H	H	N

$\overline{CP}$ or $\overline{C}_E$ = High
H = High voltage level
L = Low voltage level
N = Not allowed

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0 to 0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_n output, apply V_{IHMAX} to each D_n input, one at	–1060		–890	mV
			$T_A = +25°C$	a time, with V_{ILMIN} applied to all other inputs.	–960		–810	mV
			$T_A = +85°C$	For $\overline{Q}_n$ output, apply V_{ILMIN} to all inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_n output, apply V_{IHT} to each D_n input, one at a	–1080			mV
			$T_A = +25°C$	time with V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ output, apply V_{ILT} to each D_n input, one at a time,	–980			mV
			$T_A = +85°C$	with V_{ILMIN} applied to all other inputs.	–910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_n output, apply V_{ILT} to each D_n input, one at a			–1655	mV
			$T_A = +25°C$	time with V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ output, apply V_{IHT} to each D_n input, one at a time,			–1630	mV
			$T_A = +85°C$	with V_{ILMIN} applied to all other inputs.			–1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_n output, apply V_{ILMIN} to all inputs. For $\overline{Q}_n$	–1890		–1675	mV
			$T_A = +25°C$	output, apply V_{IHMAX} to each D_n input, one at a time,	–1850		–1650	mV
			$T_A = +85°C$	with V_{ILMIN} applied to all other inputs.	–1825		–1615	mV
I_{IH}	High level input current	$\overline{CE}_0$, $\overline{CE}_1$ inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under			360	µA
			$T_A = +25°C$	test, one at a time, with V_{ILMIN}			220	µA
			$T_A = +85°C$	applied to all other inputs.			220	µA
		$\overline{CP}$ input	$T_A = -30°C$	Apply V_{IHMAX} to $\overline{CP}$ input			425	µA
			$T_A = +25°C$	with V_{ILMIN} applied			265	µA
			$T_A = +85°C$	to all other inputs.			265	µA
		D_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to each D_n input under			455	µA
			$T_A = +25°C$	test, one at a time with V_{ILMIN}			285	µA
			$T_A = +85°C$	applied to all other inputs.			285	µA
		R_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to S_n and CP inputs and R_n			455	µA
			$T_A = +25°C$	input under test, one at a time with V_{ILMIN}			285	µA
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			285	µA
		S_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to R_n and CP inputs and S_n			455	µA
			$T_A = +25°C$	input under test, one at a time with V_{ILMIN}			285	µA
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			285	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				38	mA
			$T_A = +25°C$			30	35	mA
			$T_A = +85°C$				38	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	T_A = +25°C		0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation			0.230		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.140		V/V

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

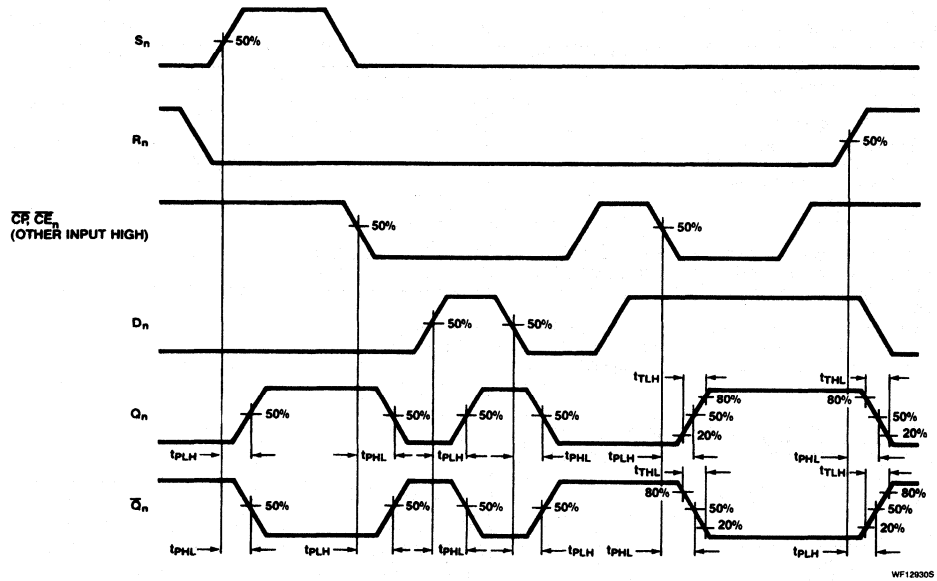
AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = –30°C MIN.	LIMITS T_A = –30°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C TYP.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.00 1.00	3.60 3.60	1.00 1.00	2.50 2.50	3.50 3.50	1.00 1.00	3.80 3.80	ns ns
t_{PLH} t_{PHL}	Propagation delay R_n to Q_n, $\overline{Q}_n$		1.00 1.00	3.60 3.60	1.00 1.00	2.70 2.70	3.50 3.50	1.00 1.00	3.90 3.90	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n, $\overline{Q}_n$		1.00 1.00	3.60 3.60	1.00 1.00	2.70 2.70	3.50 3.50	1.00 1.00	3.90 3.90	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$, $\overline{CE}_n$ to Q_n, $\overline{Q}_n$		1.00 1.00	4.30 4.30	1.00 1.00		4.00 4.00	1.00 1.00	4.10 4.10	ns ns
t_s	Setup time D_n to $\overline{CP}$, $\overline{CE}_n$	Waveform 2	2.50		2.50			2.50		ns
t_h	Hold time D_n to $\overline{CP}$, $\overline{CE}_n$		1.50		1.50			1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	3.60 3.60	1.10 1.10	2.70 2.70	3.50 3.50	1.10 1.10	3.80 3.80	ns ns

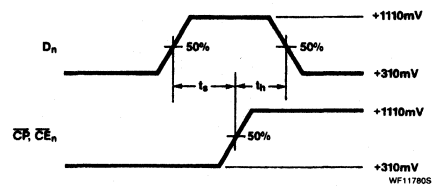
NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

Latch 10130

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times



Waveform 2. Setup and Hold Times

Document No.	853–0660
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10131
Flip-Flop

Dual D-Type Master-Slave Flip-Flop

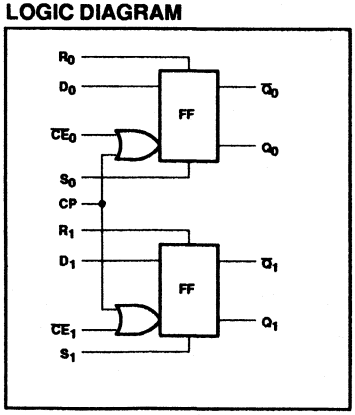
FEATURES

- **Typical propagation delay: 3.0ns**
- **Typical supply current ($-I_{EE}$): 45mA**

DESCRIPTION

The 10131 is a Dual Master-Slave Flip-Flop. Each flip-flop can be clocked separately by holding the common Clock in the Low-State and using the Clock Enable inputs for the clocking function. While the clock is Low, data at the D_n inputs are allowed to enter the master section. The output states of the flip-flops register the data present at the D_n inputs on the rising edge of the Clock. Output data (Q_n) is latched and not affected by changes at the D_n inputs while the Clock (CP) is High. All unused inputs must be tied Low to V_{IL} or V_{EE}.

LOGIC DIAGRAM



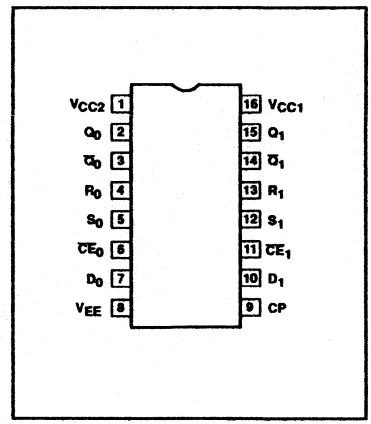
PIN DESCRIPTION

PINS	DESCRIPTION
D_0, D_1	Data Inputs
CP	Clock Input
$\overline{CE}_0$, $\overline{CE}_1$	Clock Enable Inputs
S_0, S_1	Set Inputs
R_0, R_1	Reset Inputs
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data Outputs

ORDERING INFORMATION

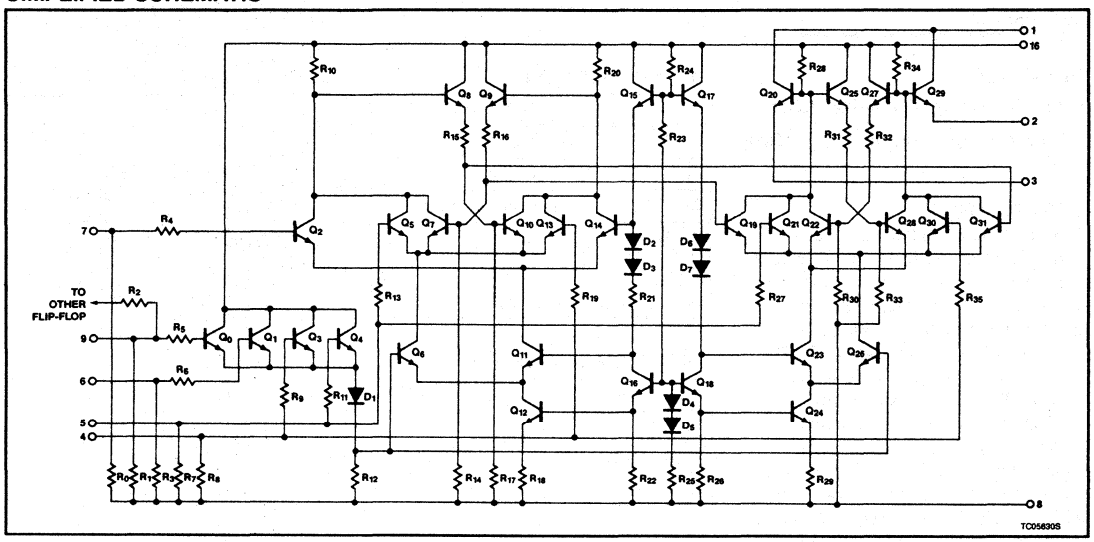
DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10131N
16–Pin Ceramic DIP	10131F
16–Pin SO	10131D

PIN CONFIGURATION



Flip–Flop 10131

SIMPLIFIED SCHEMATIC



FUNCTION TABLES

SYNCHRONOUS OPERATION

INPUTS			OUTPUT
D_n	CP	$\overline{CE}$*	Q_{n+1}**
L	L	L	Q_n
L	L	H	Q_n
L	H	L	L
L	H	H	Q_n
H	L	L	Q_n
H	L	H	Q_n
H	H	L	H
H	H	H	Q_n

* Conditions for CP and $\overline{CE}$ may be interchanged. In this table $\overline{CE}$ is static, while for CP and H represent a transition from Low to High between t_n and t_{n+1}.

** R and S = Low.

ASYNCHRONOUS OPERATION

INPUTS		OUTPUT
R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N

H = High Voltage Level
L = Low Voltage Level
N = Not allowed

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to S_n inputs with	−1060		−890	mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHMAX} to R_n inputs, with	−960		−810	mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to S_n inputs with	−1080			mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to R_n inputs, with	−980			mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to R_n inputs with			−1655	mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to S_n inputs, with			−1630	mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to R_n inputs with	−1890		−1675	mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHMAX} to S_n inputs, with	−1850		−1650	mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.	−1825		−1615	mV
I_{IH}	High level input current	CP input	$T_A = -30°C$	Apply V_{IHMAX} to CP input			425	µA
			$T_A = +25°C$	with V_{ILMIN} applied			265	µA
			$T_A = +85°C$	to all other inputs.			265	µA
		$\overline{CE}_n$ inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			350	µA
			$T_A = +25°C$				220	µA
			$T_A = +85°C$				220	µA
		D_n inputs	$T_A = -30°C$				390	µA
			$T_A = +25°C$				245	µA
			$T_A = +85°C$				245	µA
		R_n inputs	$T_A = -30°C$	For R_n inputs, apply V_{IHMAX} to D_n			525	µA
			$T_A = +25°C$	inputs and to R_n input under test			330	µA
			$T_A = +85°C$	with V_{ILMIN} applied to all other inputs.			330	µA
		S_n inputs	$T_A = -30°C$	For S_n inputs, apply V_{IHMAX} to D_n			525	µA
			$T_A = +25°C$	inputs and to S_n input under test			330	µA
			$T_A = +85°C$	with V_{ILMIN} applied to all other inputs.			330	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				62	mA
			$T_A = +25°C$			45	56	mA
			$T_A = +85°C$				62	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	T_A = +25°C		0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.148		V/V

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

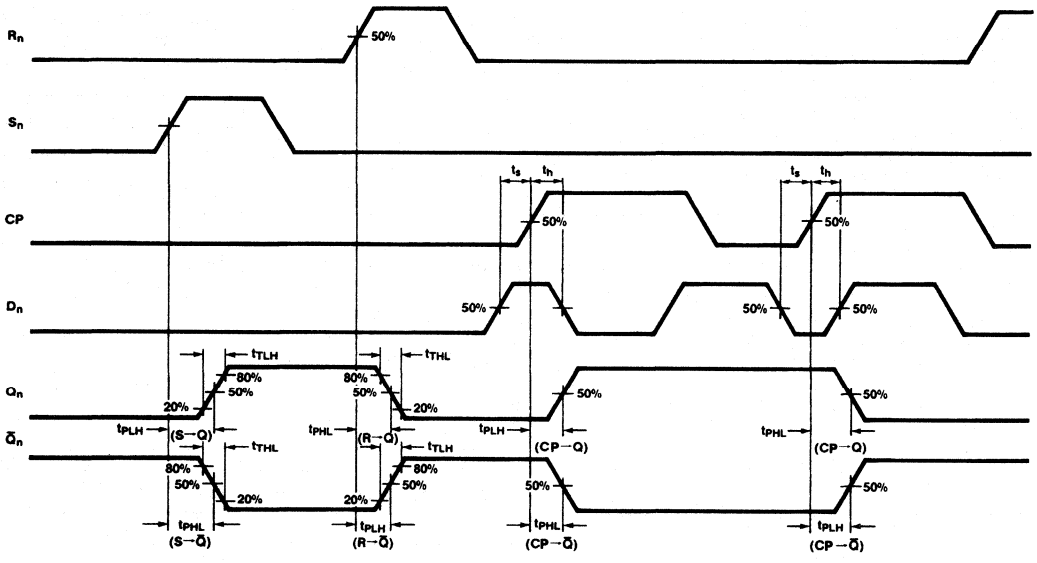
AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = –30°C MIN.	LIMITS T_A = –30°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C TYP.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	125		125	160		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	1.70 1.70	4.60 4.60	1.80 1.80	3.00 3.00	4.50 4.50	1.80 1.80	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay R_n to Q_n, $\overline{Q}_n$		1.70 1.70	4.40 4.40	1.80 1.80	2.80 2.80	4.30 4.30	1.80 1.80	4.80 4.80	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n, $\overline{Q}_n$		1.70 1.70	4.40 4.40	1.80 1.80	2.80 2.80	4.30 4.30	1.80 1.80	4.80 4.80	ns ns
t_s	Setup time D_n to CP	Waveform 2	2.50		2.50			2.50		ns
t_h	Hold time D_n to CP	Waveform 2	1.50		1.50			1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	4.60 4.60	1.10 1.10	2.50 2.50	4.50 4.50	1.10 1.10	4.90 4.90	ns ns

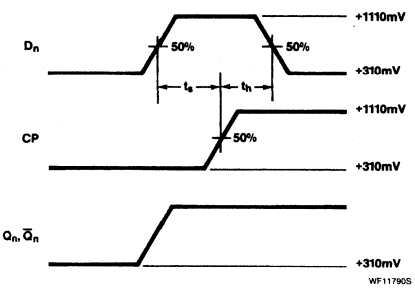
NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

Flip–Flop 10131

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

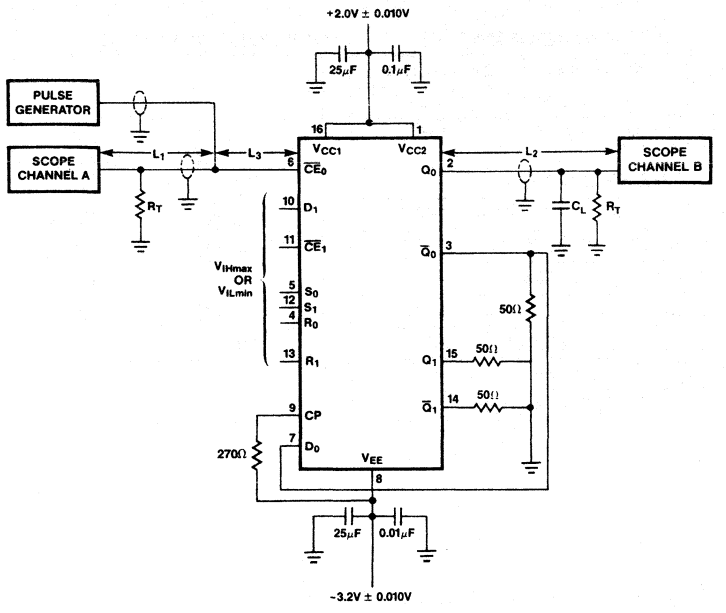


Waveform 2. Setup and Hold Times

Flip–Flop

10131

TOGGLE FREQUENCY TEST CIRCUIT



NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}; 0.01μF and 25μF from GND to V_{EE}. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. R_T = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

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10132
Multiplexer/Latch

Dual 2-Input Multiplexer with Clocked D-Type Latches and Common Reset

FEATURES

- **Typical propagation delay: 3.0ns**
- **Typical supply current ($-I_{EE}$): 44mA**

DESCRIPTION

The 10132 is a Dual 2-Input Multiplexer with Clocked D-type Latches and a Common Reset. The Latch can be clocked by the common Clock (CP) when the Clock Enable input ($\overline{CE}$) is Low or by the Clock Enable input when the common Clock is held in the Low-State. The outputs are latched by the positive transition of the Clock. Any change at the data input will be registered at the output only if the Clock is Low.

Data inputs are selected by a common data Select (S). All unused inputs must be tied Low to V_{IL} or V_{EE}.

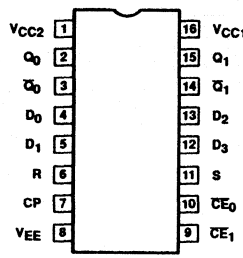
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10132N
16–Pin Ceramic DIP	10132F

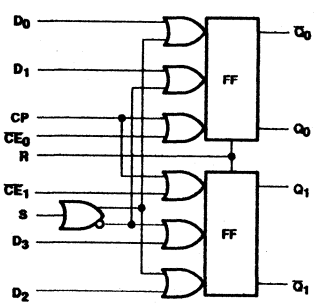
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
CP	Clock Input
$\overline{CE}_0$, $\overline{CE}_1$	Clock Enable Inputs
S	Data Select Input
R	Reset Input
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data Outputs

PIN CONFIGURATION



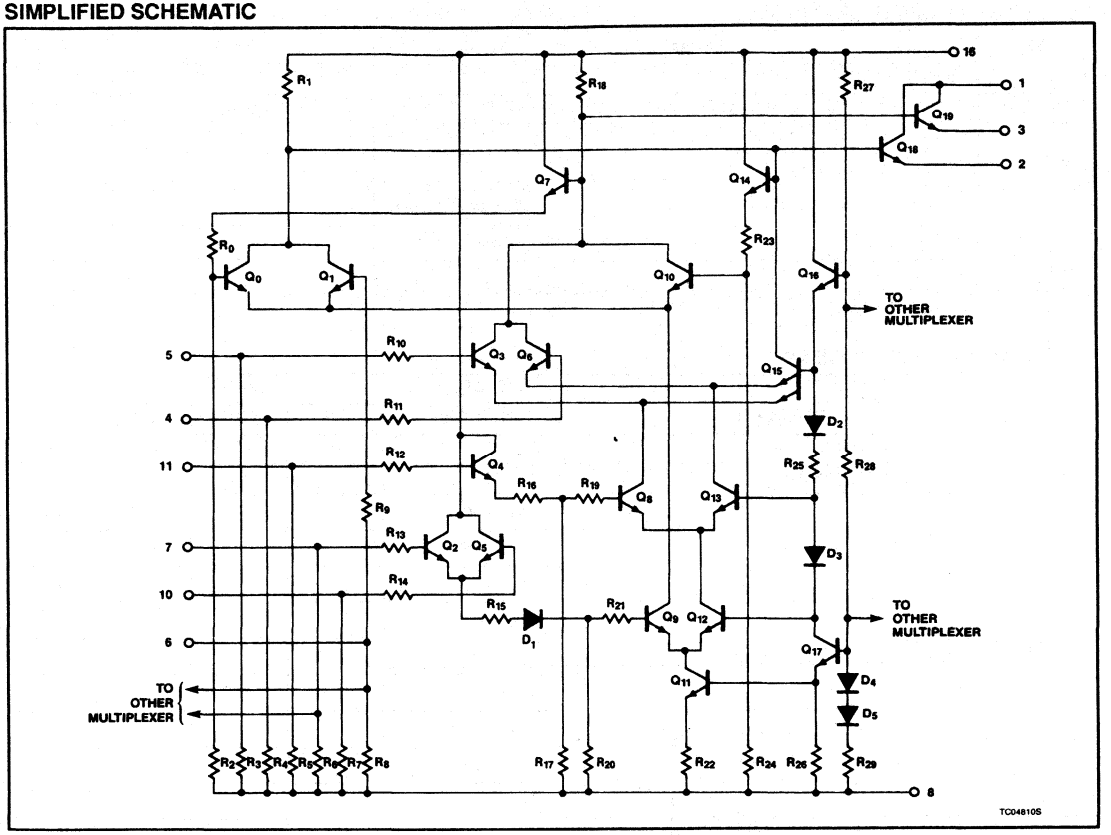
LOGIC DIAGRAM



Multiplexer/Latch

10132

SIMPLIFIED SCHEMATIC



FUNCTION TABLE

INPUTS				OUTPUT
R	S	CP*	$\overline{CE}$*	Q_{n+1}
L	L	L	L	D_0
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
L	H	L	L	D_1
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	X	X	H	L
H	X	H	X	L
H	X	L	L	Q_n

* Conditions for CP and $\overline{CE}$ may be interchanged as indicated in the function table.

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to D_0 input with	−1060		−890	mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$	−960		−810	mV
			$T_A = +85°C$	outputs, apply V_{ILMIN} to all inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to D_0 input with	−1080			mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{ILT} to D_0 input with	−980			mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to D_0 input with			−1655	mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to D_0 input with			−1630	mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to all inputs. For	−1890		−1675	mV
			$T_A = +25°C$	$\overline{Q}_n$ outputs, apply V_{IHMAX} to D_0 input with	−1850		−1650	mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.	−1825		−1615	mV
I_{IH}	High level input current	D_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to D_0 input with V_{ILMIN} applied to all			460	µA
			$T_A = +25°C$	other inputs. Apply V_{IHMAX} to D_1 input and S input			290	µA
			$T_A = +85°C$	with V_{ILMIN} applied to all other inputs.			290	µA
		R input	$T_A = -30°C$	Apply V_{IHMAX} to CP and R			620	µA
			$T_A = +25°C$	inputs with V_{ILMIN} applied			390	µA
			$T_A = +85°C$	to all other inputs.			390	µA
		CP input	$T_A = -30°C$	Apply V_{IHMAX} to CP input			460	µA
			$T_A = +25°C$	with V_{ILMIN} applied			290	µA
			$T_A = +85°C$	to all other inputs.			290	µA
		S, $\overline{CE}_n$ inputs	$T_A = -30°C$	Apply V_{IHMAX} to S or $\overline{CE}_n$ input			425	µA
			$T_A = +25°C$	under test, one at a time, with			265	µA
			$T_A = +85°C$	V_{IHMAX} applied to all other inputs.			265	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				60	mA
			$T_A = +25°C$			44	55	mA
			$T_A = +85°C$				60	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$		0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.148		V/V

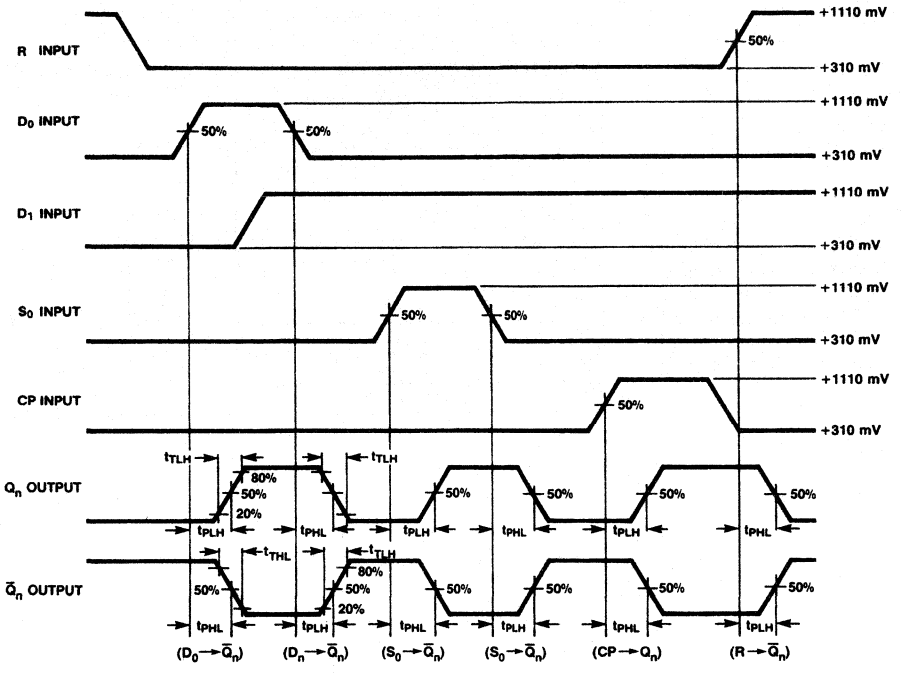
NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS $T_A = -30°C$ MIN.	LIMITS $T_A = -30°C$ MAX.	LIMITS $T_A = +25°C$ MIN.	LIMITS $T_A = +25°C$ TYP.	LIMITS $T_A = +25°C$ MAX.	LIMITS $T_A = +85°C$ MIN.	LIMITS $T_A = +85°C$ MAX.	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1, 2	1.00 1.00	3.60 3.60	1.00 1.00	3.00 3.00	3.30 3.30	1.00 1.00	3.70 3.70	ns ns
t_{PLH} t_{PHL}	Propagation delay R to Q_n, $\overline{Q}_n$		1.00 1.00	4.00 4.00	1.00 1.00		3.80 3.80	1.00 1.00	4.20 4.20	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$		1.00 1.00	6.00 6.00	1.00 1.00		5.70 5.70	1.00 1.00	6.30 6.30	ns ns
t_{PLH} t_{PHL}	Propagation delay S to Q_n, $\overline{Q}_n$		1.00 1.00	4.80 4.80	1.00 1.00		4.60 4.60	1.00 1.00	5.00 5.00	ns ns
t_s	Setup time D_n to CP		2.50		2.50			2.50		ns
t_h	Hold time D_n to CP		1.50		1.50			1.50		ns
t_s	Setup time S to CP		3.50		3.50			3.50		ns
t_h	Hold time S to CP		1.00		1.00			1.00		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.50 1.50	3.70 3.70	1.50 1.50		3.50 3.50	1.50 1.50	3.80 3.80	ns ns

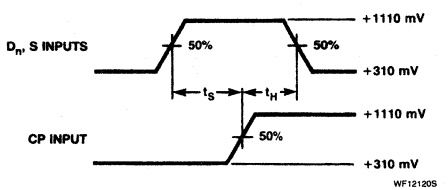
NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



NOTES:
1. Any change on the data input will be registered at the output only if the clock is LOW.
2. Outputs are latched on the positive transition of the clock.
3. The reset inputs is enabled when the clock is HIGH.

Waveform 1. Propagation Delay and Transition Times



NOTES:
1. Any change on the data input will be registered at the output only if the clock is LOW.
2. Outputs are latched on the positive transition of the clock.
3. The reset inputs is enabled when the clock is HIGH.

Waveform 2. Setup and Hold Times

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ECL Products	

10133
Latch

Quad Latch with D-Type Inputs and Enable Outputs

FEATURES

- **Typical propagation delay: 4.0ns**
- **Typical supply current ($-I_{EE}$): 59.6mA**

DESCRIPTION

The 10133 is a Quad Latch with D-Type Inputs and Enable Outputs. Data (D_n) inputs are registered at output while the clock is High. Data inputs are latched by the negative transition of the clock. All unused inputs must be tied Low to V_{IL} or V_{EE}.

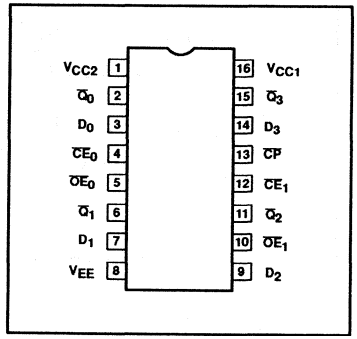
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10133N
16–Pin Ceramic DIP	10133F

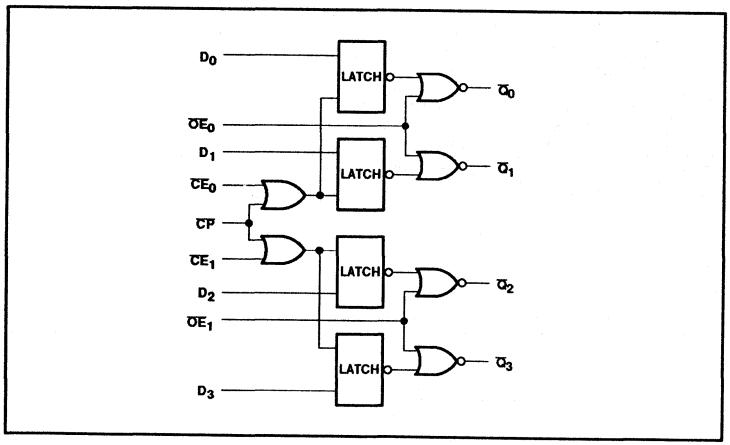
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
$\overline{CP}$	Clock Input
$\overline{CE}_0$, $\overline{CE}_1$	Clock Enable Inputs
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable Inputs
$\overline{Q}_0 - \overline{Q}_3$	Data Outputs

PIN CONFIGURATION



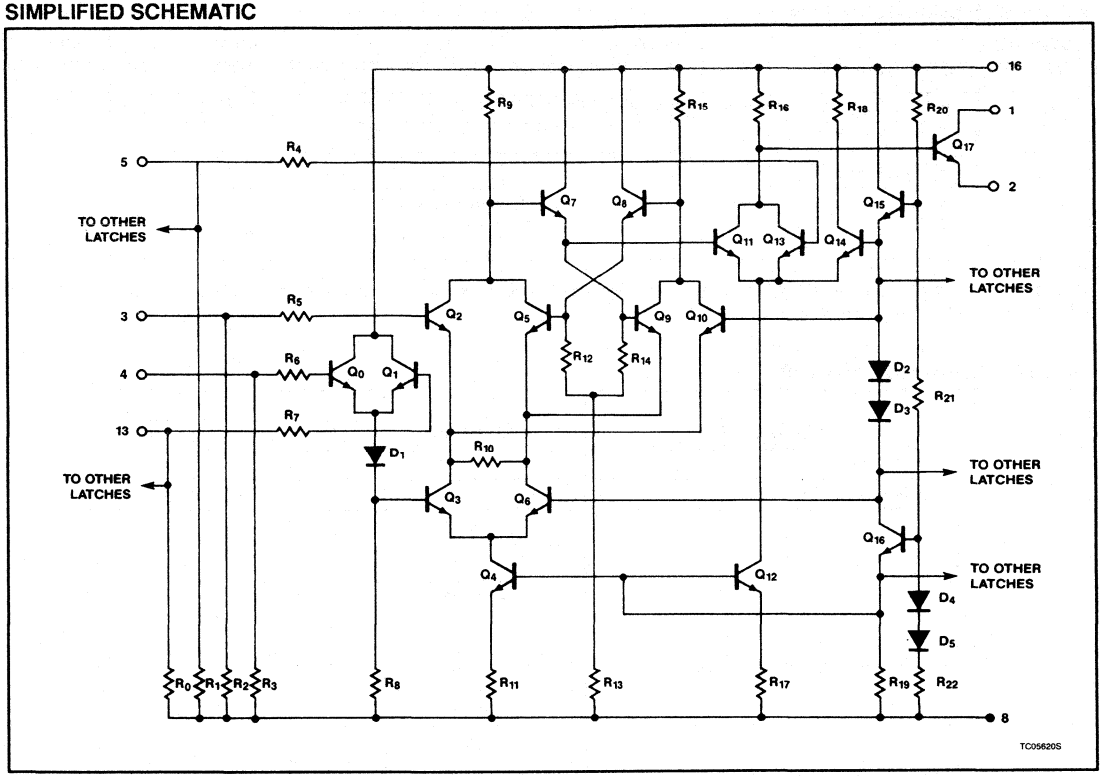
LOGIC DIAGRAM



Latch

10133

SIMPLIFIED SCHEMATIC



FUNCTION TABLES

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CP}$	$\overline{CE}$	$\overline{D_n}$	$\overline{Q}_{n+1}$
H	X	X	X	L
L	L	L	X	$\overline{Q}_n$
L	L	H	L	L
L	H	L	L	L
L	H	H	L	L
L	L	H	H	H
L	H	L	H	H
L	H	H	H	H

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{IHMAX} to each D_n input, one at a time,	–1060		–890	mV
			$T_A = +25°C$	with V_{ILMIN} applied to $\overline{OE}_n$ inputs and	–960		–810	mV
			$T_A = +85°C$	V_{IHMAX} applied to $\overline{CP}$ and $\overline{CE}_n$ inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	Apply V_{IHT} to each D_n input, one at a time,	–1080			mV
			$T_A = +25°C$	with V_{ILMIN} applied to $\overline{OE}_n$ inputs and V_{IHMAX}	–980			mV
			$T_A = +85°C$	applied to $\overline{CP}$ and $\overline{CE}_n$ inputs.	–910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	Apply V_{ILT} to each D_n input, one at a time,			–1655	mV
			$T_A = +25°C$	with V_{IHMAX} applied to $\overline{CP}$ and $\overline{CE}_n$ inputs			–1630	mV
			$T_A = +85°C$	and V_{ILMIN} applied to $\overline{OE}_n$ inputs.			–1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	Apply V_{ILMIN} to each D_n input, one at a time,	–1890		–1675	mV
			$T_A = +25°C$	with V_{IHMAX} applied to $\overline{CP}$ and $\overline{CE}_n$ inputs,	–1850		–1650	mV
			$T_A = +85°C$	and V_{ILMIN} applied to $\overline{OE}_n$ inputs.	–1825		–1615	mV
I_{IH}	High level input current	D_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to the $\overline{CP}$ input and to each			390	µA
			$T_A = +25°C$	D_n input under test, one at a time, with			245	µA
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			245	µA
		$\overline{CE}_n$ inputs	$T_A = -30°C$	Apply V_{IHMAX} to each $\overline{CE}_n$ input under			425	µA
			$T_A = +25°C$	test, one at a time, with V_{ILMIN}			265	µA
			$T_A = +85°C$	applied to all other inputs.			265	µA
		$\overline{CP}$ input	$T_A = -30°C$	Apply V_{IHMAX} to $\overline{CP}$ input			560	µA
			$T_A = +25°C$	with V_{ILMIN} applied			350	µA
			$T_A = +85°C$	to all other inputs.			350	µA
		$\overline{OE}_n$ inputs	$T_A = -30°C$	Apply V_{IHMAX} to the $\overline{CP}$ input and to all D_n			560	µA
			$T_A = +25°C$	inputs and to each $\overline{OE}_n$ input under test, one at			350	µA
			$T_A = +85°C$	a time with V_{ILMIN} applied to all other inputs.			350	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$	Apply V_{ILMIN} to $\overline{CP}$ input.			82	mA
			$T_A = +25°C$			59.6	72	mA
			$T_A = +85°C$				82	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	T_A = +25°C		0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.148		V/V

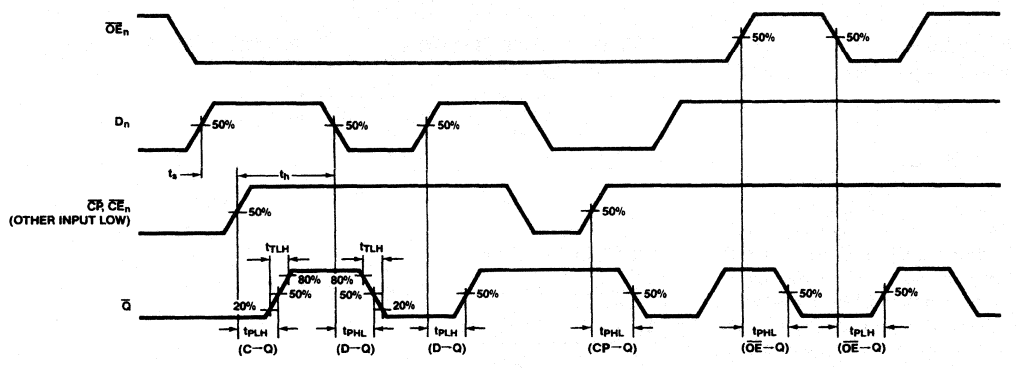
NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = –30°C MIN.	LIMITS T_A = –30°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C TYP.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 1	1.00 1.00	5.60 5.60	1.00 1.00	4.00 4.00	5.40 5.40	1.10 1.10	5.90 5.90	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$, $\overline{CE}_n$ to $\overline{Q}_n$		1.00 1.00	5.40 5.40	1.00 1.00	4.00 4.00	5.40 5.40	1.20 1.20	6.00 6.00	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to $\overline{Q}_n$		1.00 1.00	3.20 3.20	1.00 1.00	2.00 2.00	3.10 3.10	1.00 1.00	3.40 3.40	ns ns
t_s	Setup time D_n to $\overline{CP}$		2.50		2.50	0.70		2.50		ns
t_h	Hold time D_n to $\overline{CP}$		1.50		1.50	0.70		1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.00 1.00	3.60 3.60	1.10 1.10	2.00 2.00	3.50 3.50	1.10 1.10	3.80 3.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0663
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10134
Multiplexer/Latch

Dual 2-Input Multiplexer with Clocked D-Type Latches

FEATURES

- **Typical propagation delay: 3.0ns**
- **Typical supply current ($-I_{EE}$): 42mA**

DESCRIPTION

The 10134 is a Dual 2-Input Multiplexer with Clocked D-Type Latches. Latches can be clocked by the common Clock ($\overline{CP}$) when the Clock Enable input ($\overline{CE}$) is Low or by the Clock Enable input when the common Clock is held in the Low-State. The outputs are latched by the positive transition of the clock. Any change in the data will be registered at the output only if the clock is Low.

Data inputs are selected by two Data Select inputs (S_0, S_1). All unused inputs must be tied Low to V_{IL} or V_{EE}.

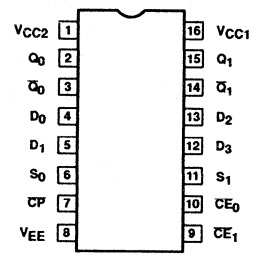
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic DIP	10134N
16-Pin Ceramic DIP	10134F

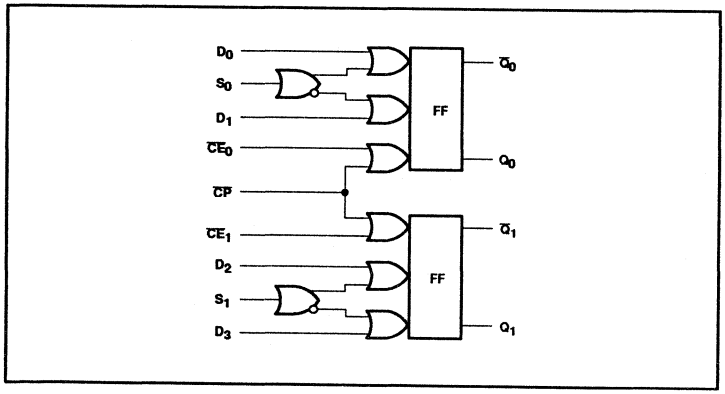
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
$\overline{CP}$	Clock Input
$\overline{CE}_0$, $\overline{CE}_1$	Clock Enable Inputs
S_0, S_1	Select Inputs
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data Outputs

PIN CONFIGURATION



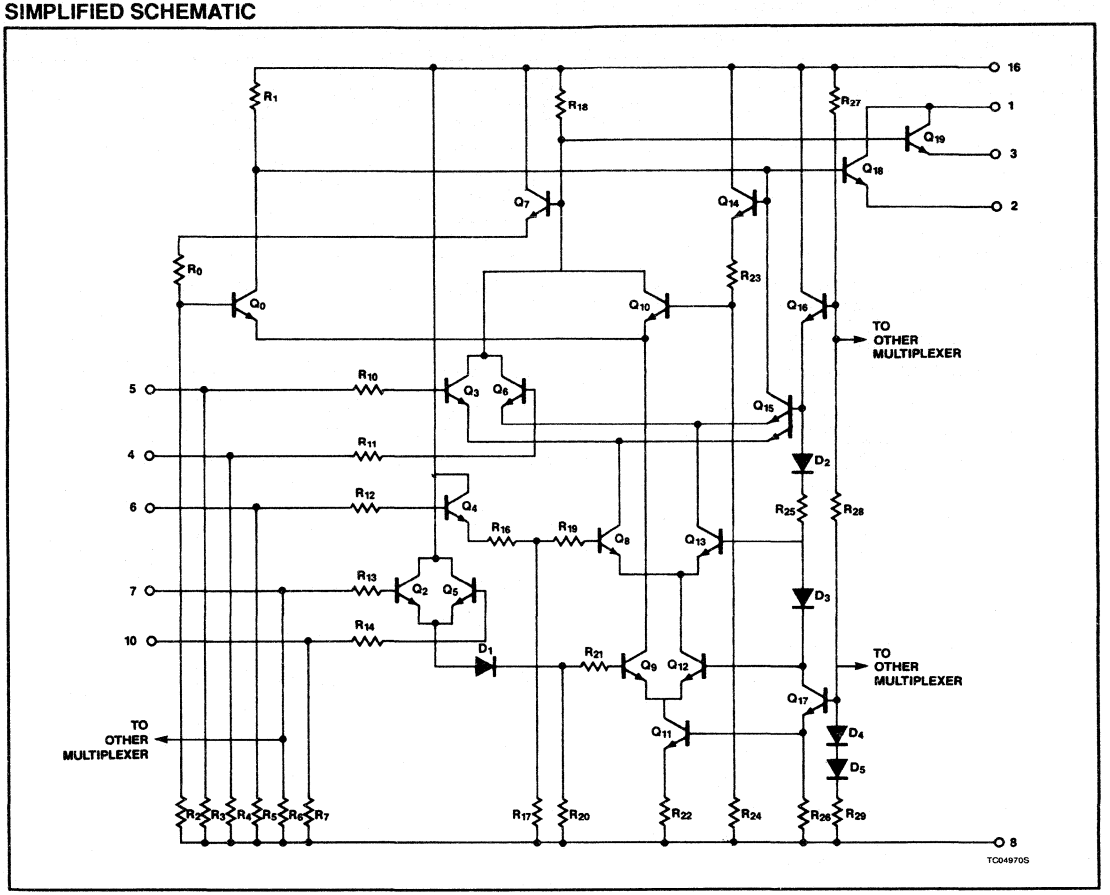
LOGIC DIAGRAM



Multiplexer/Latch

10134

SIMPLIFIED SCHEMATIC



FUNCTION TABLE

INPUTS			OUTPUT
S_n	$\overline{CP}$	$\overline{CE}_n$	Q_{n+1}
L	L	L	D_n
L	L	H	Q_n
L	H	L	Q_n
L	H	H	Q_n
H	L	L	D_2
H	L	H	Q_n
H	H	L	Q_n
H	H	H	Q_n

H = High Voltage Level
L = Low Voltage Level

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_0 output, apply V_{IHMAX} to D_0 input with	–1060		–890	mV
			$T_A = +25°C$	V_{ILMIN} applied to S_0, $\overline{CE}_0$ and $\overline{CP}$ inputs. For	–960		–810	mV
			$T_A = +85°C$	$\overline{Q}_0$ outputs, apply V_{ILMIN} to all inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_0 output, apply V_{IHT} to D_0 input with V_{ILMIN}	–1080			mV
			$T_A = +25°C$	applied to S_0, $\overline{CE}_0$ and $\overline{CP}$ inputs. For $\overline{Q}_0$ outputs, apply V_{ILT} to D_0 input with V_{ILMIN} applied to	–980			mV
			$T_A = +85°C$	S_0, $\overline{CE}_0$, and $\overline{CP}$ inputs.	–910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_0 output, apply V_{ILT} to D_0 input with V_{ILMIN}			–1655	mV
			$T_A = +25°C$	applied to S_0, $\overline{CE}_0$ and $\overline{CP}$ inputs. For $\overline{Q}_0$ outputs, apply V_{IHT} to D_0 input with V_{ILMIN} applied to			–1630	mV
			$T_A = +85°C$	S_0, $\overline{CE}_0$, and $\overline{CP}$ inputs.			–1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_0 output, apply V_{ILMIN} to all inputs. For	–1890		–1675	mV
			$T_A = +25°C$	$\overline{Q}_0$ outputs apply V_{IHMAX} to D_0 input with	–1850		–1650	mV
			$T_A = +85°C$	V_{ILMIN} applied to S_0, $\overline{CE}_0$ and $\overline{CP}$ inputs.	–1825		–1615	mV
I_{IH}	High level input current	D_0 input	$T_A = -30°C$	Apply V_{IHMAX} to D_0 input with			460	µA
			$T_A = +25°C$	V_{ILMIN} applied to S_0 and all			290	µA
			$T_A = +85°C$	other inputs (measure D_0 input only).			290	µA
		D_1 input	$T_A = -30°C$	Apply V_{IHMAX} to D_1 and S_0 inputs			460	µA
			$T_A = +25°C$	with V_{ILMIN} applied to all other			290	µA
			$T_A = +85°C$	inputs (measure D_1 input only).			290	µA
		D_2 input	$T_A = -30°C$	Apply V_{IHMAX} to D_2 input with			460	µA
			$T_A = +25°C$	V_{ILMIN} applied to all other			290	µA
			$T_A = +85°C$	inputs (measure D_2 input only).			290	µA
		D_3 input	$T_A = -30°C$	Apply V_{IHMAX} to D_3 and S_1 inputs			460	µA
			$T_A = +25°C$	with V_{ILMIN} applied to all other			290	µA
			$T_A = +85°C$	inputs (measure D_3 input only).			290	µA
		$\overline{CE}_n$, S_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under			425	µA
			$T_A = +25°C$	test, one at a time, with			265	µA
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			265	µA
		$\overline{CP}$ input	$T_A = -30°C$	Apply V_{IHMAX} to CP input			460	µA
			$T_A = +25°C$	with V_{ILMIN} applied to all			290	µA
			$T_A = +85°C$	other inputs.			290	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with	0.5			µA
			$T_A = +85°C$	V_{IHMAX} applied to all other inputs.	0.3			µA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$			60	mA
		$T_A = +25°C$		42	55	mA
		$T_A = +85°C$			60	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$		0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.148		V/V

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

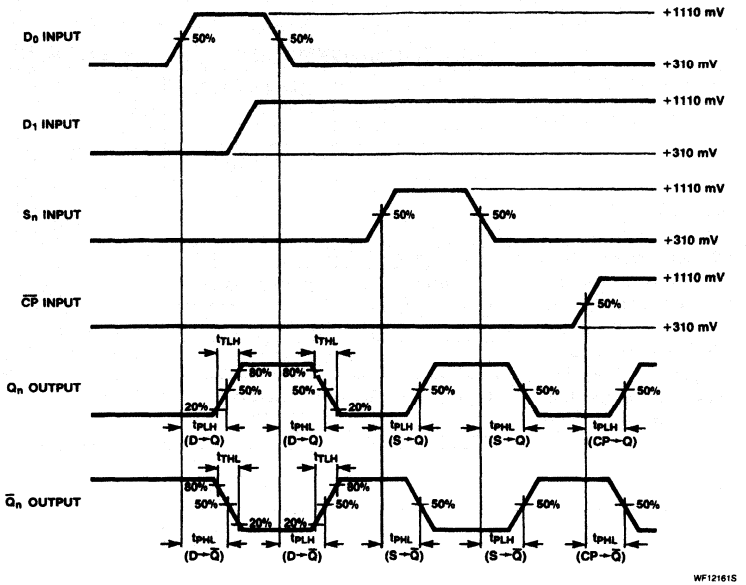
AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = -30°C$ MIN.	LIMITS $T_A = -30°C$ MAX.	LIMITS $T_A = +25°C$ MIN.	LIMITS $T_A = +25°C$ TYP.	LIMITS $T_A = +25°C$ MAX.	LIMITS $T_A = +85°C$ MIN.	LIMITS $T_A = +85°C$ MAX.	UNIT
t_{PLH}	Propagation delay D_n to Q_n	Waveform 1, 2	1.00	3.50	1.00	3.00	3.30	1.00	3.60	ns
t_{PHL}			1.00	3.50	1.00	3.00	3.30	1.00	3.60	ns
t_{PLH}	Propagation delay $\overline{CP}$ to Q_n		1.00	6.00	1.00		5.70	1.00	6.30	ns
t_{PHL}			1.00	6.00	1.00		5.70	1.00	6.30	ns
t_{PLH}	Propagation delay S_n to Q_n		1.00	4.80	1.00		4.60	1.00	5.00	ns
t_{PHL}			1.00	4.80	1.00		4.60	1.00	5.00	ns
t_s	Setup time D_n to $\overline{CP}$		2.50		2.50			2.50		ns
t_h	Hold time D_n to $\overline{CP}$		1.50		1.50			1.50		ns
t_s	Setup time S_n to $\overline{CP}$		3.50		3.50			3.50		ns
t_h	Hold time S_n to $\overline{CP}$		1.00		1.00			1.00		ns
t_{TLH}	Transition time 20% to 80%, 80% to 20%		1.50	3.70	1.50		3.50	1.50	3.80	ns
t_{THL}			1.50	3.70	1.50		3.50	1.50	3.80	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

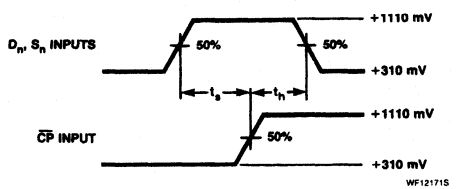
Multiplexer/Latch 10134

AC WAVEFORMS



NOTES:
1. Any change on the data input will be registered at the output only if the clock is LOW.
2. Outputs are latched on the positive transition of the clock.

Waveform 1. Propagation Delays and Transition Times



Waveform 2. Setup and Hold Times

Philips Components

Document No.	853–0664
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10135
Flip-Flop

Dual J-K Master-Slave Flip-Flop

FEATURES

- **Typical propagation delay: 3.0ns**
- **Typical supply current ($-I_{EE}$): 54mA**

DESCRIPTION

The 10135 is a Dual Master-Slave DC coupled J-K Flip-Flop. It contains a common clock and separate J-$\overline{K}$ inputs which do not affect the output when the Clock is static. The outputs of the 10135 register a change on the J or $\overline{K}$ inputs with a positive transition of the Clock. Asynchronous Set (S) and Reset (R) inputs are provided which override the Clock. Unused inputs must be tied Low to V_{IL} or V_{EE}.

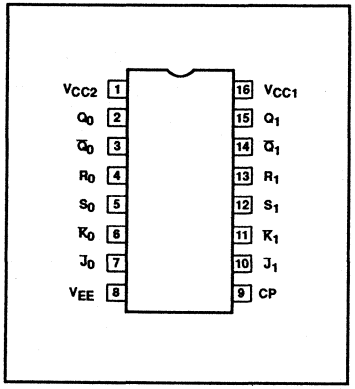
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10135N
16–Pin Ceramic DIP	10135F

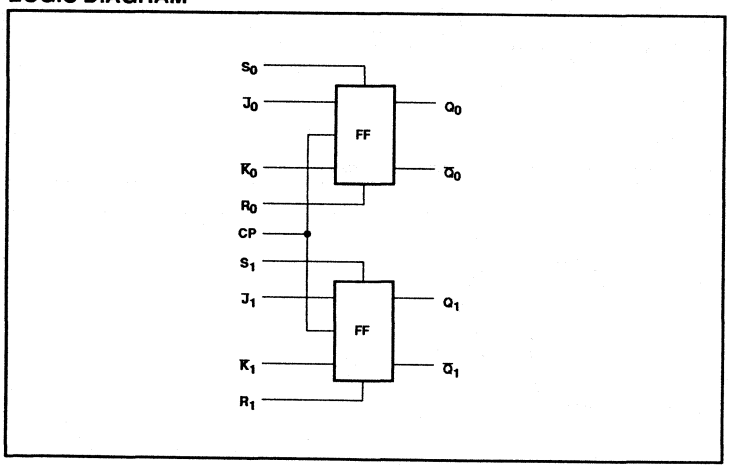
PIN DESCRIPTION

PINS	DESCRIPTION
J_n, $\overline{K}_n$	J, K Inputs
CP	Clock Input
S_n, R_n	Set and Reset Inputs
Q_n, $\overline{Q}_n$	Data Outputs

PIN CONFIGURATION



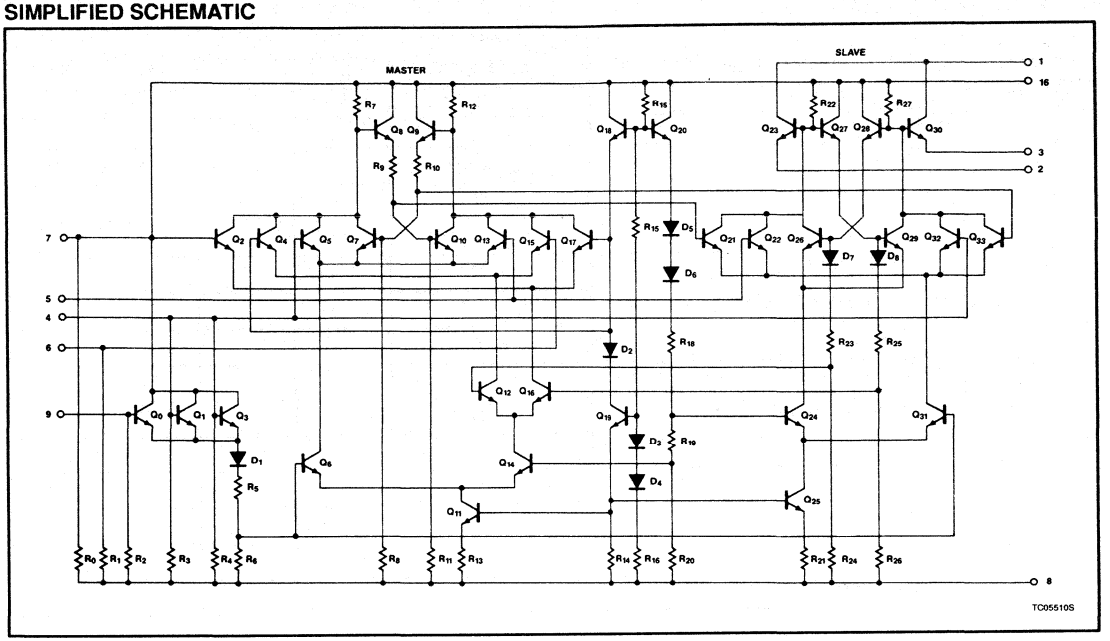
LOGIC DIAGRAM



Flip–Flop

10135

SIMPLIFIED SCHEMATIC



FUNCTION TABLES

INPUTS		OUTPUT
R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	*

* Not allowed.
R and S must be Low.

INPUTS		OUTPUT
J	$\overline{K}$	$\overline{Q}_{n+1}$
L	L	$\overline{Q}_n$
H	L	L
L	H	H
H	H	$\overline{Q}_n$

H = High Voltage Level
L = Low Voltage Level

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to S input with V_{ILMIN}	–1060		–890	mV
			$T_A = +25°C$	applied to R input and all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHMAX} to R input with V_{ILMIN}	–960		–810	mV
			$T_A = +85°C$	applied to S input and and all other inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to S input with V_{ILMIN}	–1080			mV
			$T_A = +25°C$	applied to R input and all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to S input with V_{ILMIN} applied	–980			mV
			$T_A = +85°C$	to R input and all other inputs.	–910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to R input with V_{ILMIN}			–1655	mV
			$T_A = +25°C$	applied to S input and all other inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to S input with V_{ILMIN} applied			–1630	mV
			$T_A = +85°C$	to R input and all other inputs.			–1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to R input with V_{ILMIN}	–1890		–1675	mV
			$T_A = +25°C$	applied to S input and all other inpputs. For Q_n outputs, apply V_{IHMAX} to S input with V_{ILMIN} applied	–1850		–1650	mV
			$T_A = +85°C$	to R input and all other inputs.	–1825		–1615	mV
I_{IH}	High level input current	S, R inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input, under			620	µA
			$T_A = +25°C$	test, one at a time, with V_{ILMIN}			390	µA
			$T_A = +85°C$	applied to all other inputs.			390	µA
		J, K CP inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input, under			425	µA
			$T_A = +25°C$	test, one at a time, with V_{ILMIN}			265	µA
			$T_A = +85°C$	applied to all other inputs.			265	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				75	mA
			$T_A = +25°C$			54	68	mA
			$T_A = +85°C$				75	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

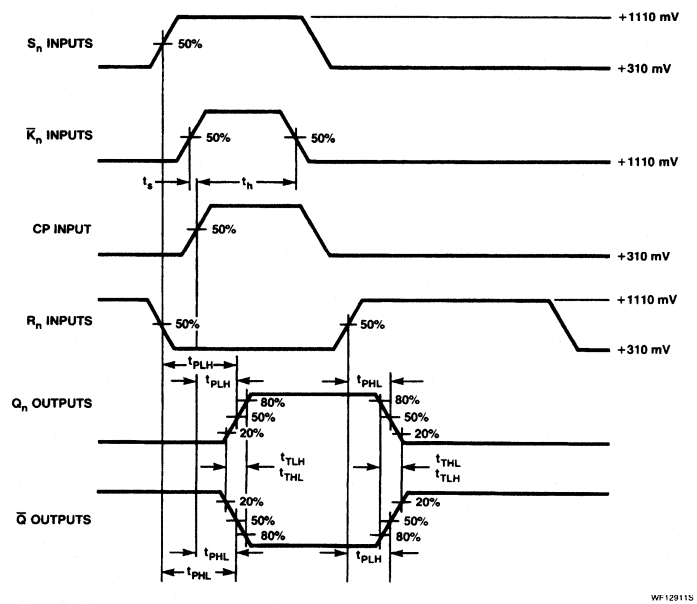
Flip–Flop 10135

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency	Waveform 1	125		125	140		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$		1.80 1.80	5.00 5.00	1.80 1.80	3.00 3.00	4.50 4.50	1.80 1.80	4.60 4.60	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n, $\overline{Q}_n$		1.80 1.80	5.60 5.60	1.80 1.80	3.00 3.00	5.00 5.00	1.80 1.80	5.20 5.20	ns ns
t_{PLH} t_{PHL}	Propagation delay R_n to Q_n, $\overline{Q}_n$		1.80 1.80	5.60 5.60	1.80 1.80	3.00 3.00	5.00 5.00	1.80 1.80	5.20 5.20	ns ns
t_s	Setup time J_n, $\overline{K}_n$ to CP		2.50		2.50	1.00		2.50		ns
t_h	Hold time J_n, $\overline{K}_n$ to CP		1.50		1.50	1.00		1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.10 1.10	4.80 4.80	1.10 1.10	2.00 2.00	4.50 4.50	1.10 1.10	4.70 4.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delays, Setup Times, Hold Times, and Transition Times

Document No.	853–0665
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10136
Universal Counter

Universal Hexadecimal Counter

FEATURES

- **Typical propagation delay: 3.3ns**
- **Typical supply current ($-I_{EE}$): 120mA**

DESCRIPTION

The 10136 is a high-speed Hexadecimal Synchronous Counter that can count up, count down, preset, or stop count at frequencies exceeding 100MHz. The operation mode of the counter is programmed by three control lines (S_0, S_1, and CP) as can be seen in the Function Select Table. In the preset mode (loading step), a clock pulse is needed for the information present on the data inputs (D_0, D_1, D_2, and D_3) to be entered into the counter. $\overline{C}_{OUT}$ goes Low on the terminal count, or when the counter is being preset.

The counter changes state only on the positive-going edge of the clock, so at any other time any other input may change without any result (except for $\overline{C}_{OUT}$).

This binary counter can be used in many applications, such as in computing for high-speed control processors and peripheral controllers. Unused inputs must be tied Low to V_{IL} or V_{EE}.

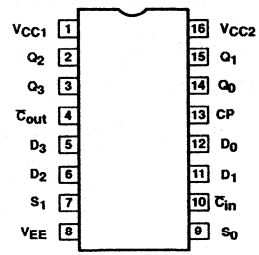
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10136N
16–Pin Ceramic DIP	10136F

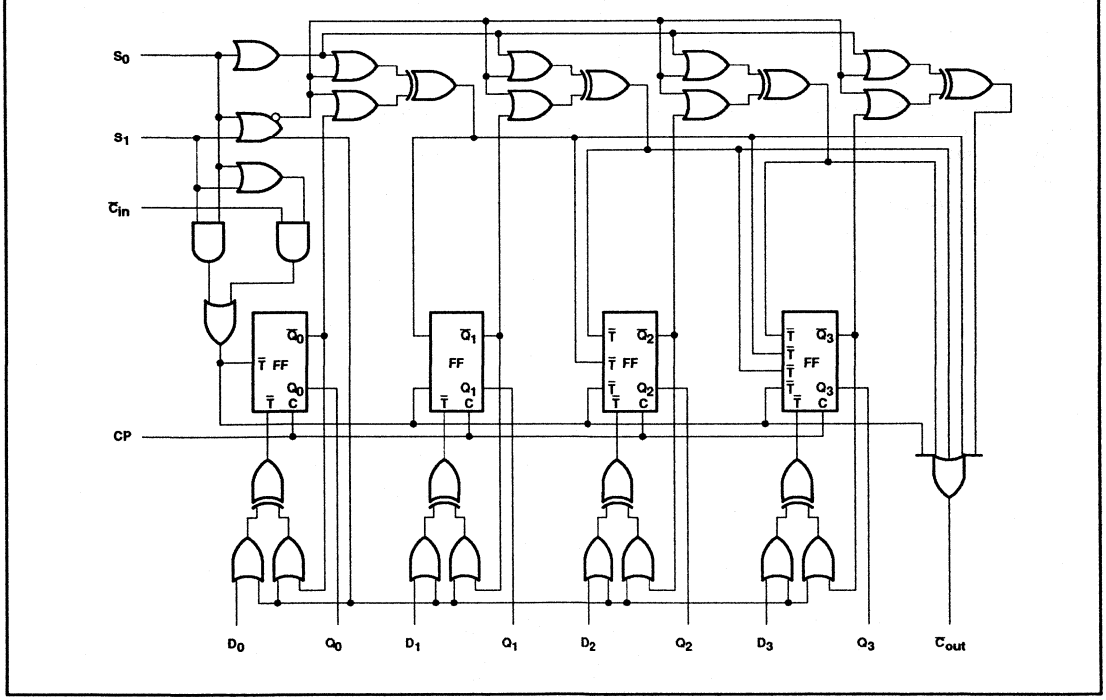
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
CP	Clock Input
$\overline{C}_{IN}$	Carry–in Input
S_0, S_1	Select Inputs
$\overline{C}_{OUT}$	Carry–out Output
$Q_0 - Q_3$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Universal Counter 10136

FUNCTION SELECT TABLE

$\overline{C}_{IN}$	S_0	S_1	OPERATING MODE
X	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
X	H	H	Hold (Stop Count)

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

SEQUENTIAL FUNCTION TABLE

INPUTS								OUTPUTS				
S_0	S_1	D_0	D_1	D_2	D_3	$\overline{C}_{IN}$	CP	Q_0	Q_1	Q_2	Q_3	$\overline{C}_{OUT}$
L	L	L	L	H	H	X	↑	L	L	H	H	L
L	H	X	X	X	X	L	↑	H	L	H	H	H
L	H	X	X	X	X	L	↑	L	H	H	H	H
L	H	X	X	X	X	L	↑	H	H	H	H	L
L	H	X	X	X	X	H	L	H	H	H	H	H
L	H	X	X	X	X	H	↑	H	H	H	H	H
H	H	X	X	X	X	X	↑	H	H	H	H	H
L	L	H	H	L	L	X	↑	H	H	L	L	L
H	L	X	X	X	X	L	↑	L	H	L	L	H
H	L	X	X	X	X	L	↑	H	L	L	L	H
H	L	X	X	X	X	L	↑	L	L	L	L	L
H	L	X	X	X	X	L	↑	H	H	H	H	H

NOTE:
This function table shows logic states assuming inputs vary in the sequence shown from top to bottom.
H = High Voltage Level
L = Low Voltage Level
X = Don't Care
↑ = Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to CP, S_0, and S_1 inputs. After applying V_{IHMAX} to all other inputs,	–1060		–890	mV
			$T_A = +25°C$	change the CP input from V_{ILMIN} to V_{IHMAX}. For $\overline{C}_{OUT}$, apply V_{ILMIN} to CP, $\overline{C}_{IN}$, S_0, and S_1 inputs. After applying V_{IHMAX} to D_n inputs,	–960		–810	mV
			$T_A = +85°C$	change CP from V_{ILMIN} to V_{IHMAX} then change S_0 and $\overline{C}_{IN}$ from V_{ILMIN} to V_{IHMAX}.	–890		–700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_0 output, apply V_{IHT} to D_0 input and V_{ILMIN} to CP, S_0, S_1, and D_1, D_2, and D_3. Raise CP from	–1080			mV
			$T_A = +25°C$	V_{ILMIN} to V_{IHMAX} and measure Q_0. Repeat this process for Q_1, Q_2, and Q_3 by applying V_{IHT} to D_1, D_2, and D_3, respectively, one at a time. For $\overline{C}_{OUT}$, apply	–980			mV
			$T_A = +85°C$	V_{ILMIN} to CP, $\overline{C}_{IN}$, S_0, and S_1 inputs. After applying V_{IHMAX} to D_n inputs change CP from V_{ILMIN} to V_{IHT}, then change S_0 and $\overline{C}_{IN}$ from V_{ILMIN} to V_{IHMAX}.	–910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to D_n inputs and to CP, S_0, and S_1 inputs. Raise CP from V_{ILMIN} to			–1655	mV
			$T_A = +25°C$	V_{IHT} and measure Q_n outputs. For $\overline{C}_{OUT}$, apply V_{ILT} to CP, $\overline{C}_{IN}$, S_0, and S_1 inputs. After applying V_{IHMAX}			–1630	mV
			$T_A = +85°C$	to D_n inputs, change CP from V_{ILMIN} to V_{IHMAX} and measure $\overline{C}_{OUT}$.			–1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to D_n inputs and to CP, S_0, and S_1 inputs. Raise CP from V_{ILMIN} to	–1890		–1675	mV
			$T_A = +25°C$	V_{IHMAX} and measure Q_n outputs. For $\overline{C}_{OUT}$, apply V_{ILMIN} to CP, $\overline{C}_{IN}$, S_0, and S_1 inputs. After applying	–1850		–1650	mV
			$T_A = +85°C$	V_{IHMAX} to D_n inputs, change CP from V_{ILMIN} to V_{IHMAX} and measure $\overline{C}_{OUT}$.	–1825		–1615	mV
I_{IH}	High level input current	D_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input, under test, one at a time, with V_{ILMIN} applied to all other inputs.			350	µA
			$T_A = +25°C$				220	µA
			$T_A = +85°C$				220	µA
		S_1 input	$T_A = -30°C$				425	µA
			$T_A = +25°C$				265	µA
			$T_A = +85°C$				265	µA
		S_0, $\overline{C}_{IN}$ inputs	$T_A = -30°C$				390	µA
			$T_A = +25°C$				245	µA
			$T_A = +85°C$				245	µA
		CP input	$T_A = -30°C$				460	µA
			$T_A = +25°C$				290	µA
			$T_A = +85°C$				290	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
I_{IL}	Low level input current	T_A = –30°C	Apply V_{ILMIN} to each input under	0.5			µA
		T_A = +25°C	test, one at a time, with V_{IHMAX}	0.5			µA
		T_A = +85°C	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	T_A = –30°C				165	mA
		T_A = +25°C			120	150	mA
		T_A = +85°C				165	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	T_A = +25°C			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

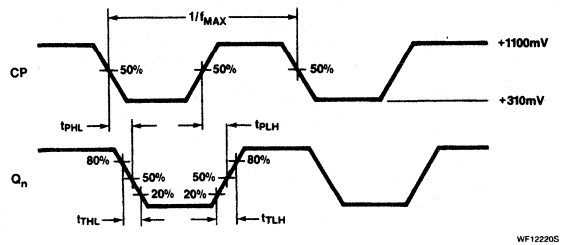
NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 0.010V

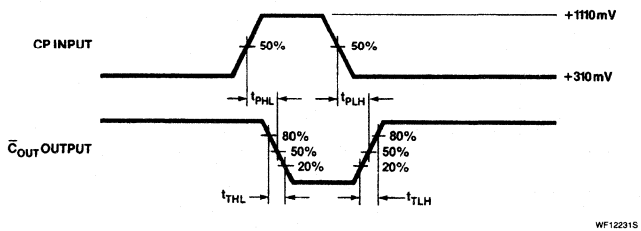
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = –30°C Min	Max	T_A = +25°C Min	Typ	Max	T_A = +85°C Min	Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	125		125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1, 2, 3	0.80 0.80	4.80 4.80	1.00 1.00	3.30 3.30	4.50 4.50	1.40 1.40	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{C}_{OUT}$		2.00 2.00	10.90 10.90	2.50 2.50	7.00 7.00	10.50 10.50	2.50 2.50	11.50 11.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to $\overline{C}_{OUT}$		1.60 1.60	7.40 7.40	1.60 1.60	5.00 5.00	6.90 6.90	1.90 1.90	7.50 7.50	ns ns
t_s	Setup time D_n to CP	Waveform 4	3.50		3.50			3.50		ns
t_h	Hold time CP to D_n		0.00		0.00			0.00		ns
t_s	Setup time S_n to CP		7.50		7.50			7.50		ns
t_h	Hold time CP to S_n		–1.00		–1.00			–1.00		ns
t_s	Setup time $\overline{C}_{IN}$ to CP	Waveform 5	4.50		3.70			4.50		ns
t_h	Hold time CP to $\overline{C}_{IN}$		–1.00		–1.00			–1.00		ns
t_s	Setup time CP to $\overline{C}_{IN}$		–1.00		–1.00			–1.00		ns
t_h	Hold time $\overline{C}_{IN}$ to CP		4.00		3.10			4.00		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1, 2, 3	0.90 0.90	3.30 3.30	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.50 3.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

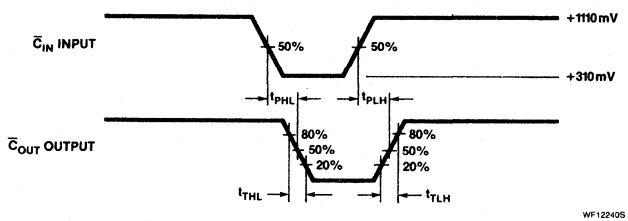
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Clock Input to Outputs and Maximum Clock Frequency

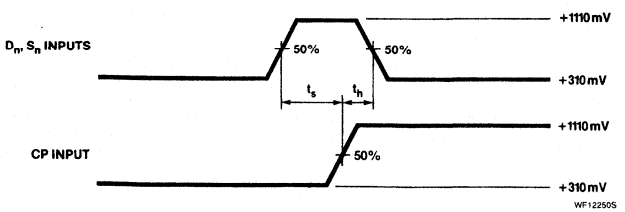


Waveform 2. Propagation Delay and Transition Time for Clock Input to Carry–Out Output

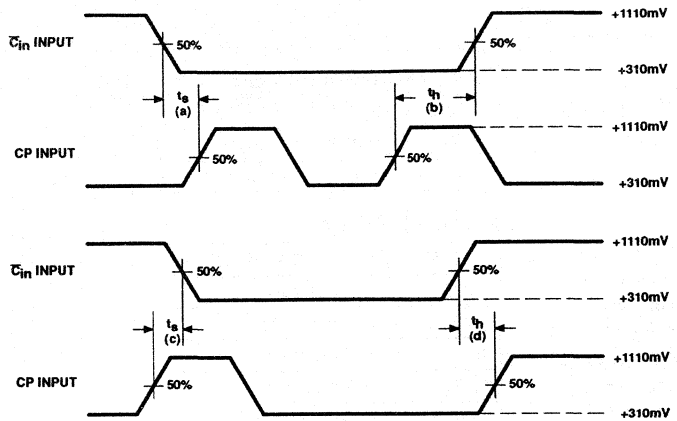


NOTE:
Setup times are the minimum times before the positive transition of the clock pulse (CP) that information must be present at the data input (D) or control input (S).
Hold times are the minimum times after the positive transition of the clock pulse (CP) that information must remain unchanged at the data input (D) or control input (S).

Waveform 3. Propagation Delay and Transition Time for Carry–In Input to Carry–Out Output



Waveform 4. Setup and Hold Times for Data and Select Inputs to Clock Input



NOTES:
(a) is the minimum time to wait to clock the counter after it is enabled.
(b) is the minimum time that the counter may be clocked before it is disabled.
(c) is the minimum time that a clock pulse may be applied with no effect on the state of the counter before it is enabled.
(d) is the minimum time to wait before a clock pulse may be applied with no effect on the state of the counter after is is disabled.
(b) and (c) may be negative numbers.

Waveform 5. Setup and Hold Times for $\overline{C}_{IN}$ to CP

Document No.	853–0666
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10137
Universal Counter

Universal Decade Counter

FEATURES

- **Typical propagation delay: 3.3ns**
- **Typical supply current ($-I_{EE}$): 120mA**

DESCRIPTION

The 10137 is a high-speed Synchronous Decade Counter that can count up, count down, preset, or stop count at frequencies exceeding 100MHz.

The operation mode of the counter is programmed by three control lines (S_0, S_1, and $\overline{C}_{IN}$) as can be seen in the Function Select Table.

In the preset mode (loading step), a clock pulse is needed for the information present on the data inputs (D_0, D_1, D_2, and D_3) to be entered into the counter. $\overline{C}_{OUT}$ goes Low on the terminal count. $\overline{C}_{OUT}$ is partially decoded from Q_0 and Q_1 directly, so in the preset mode the condition of $\overline{C}_{OUT}$ after the clock's positive excursion will depend on the condition fo Q_0 and/or Q_1.

The counter changes state only on the positive-going edge of the clock, so at any other time any other input may change without any result (except for $\overline{C}_{OUT}$). The sequence for counting out of proper states is as shown in the state diagrams. This binary counter can be used in many applications, such as in computing for high-speed control processors and peripheral controllers.

Unused inputs must be tied Low to V_{IL} or V_{EE}.

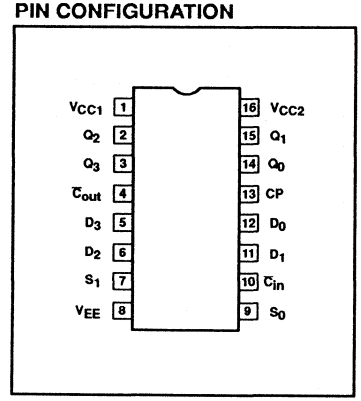
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10137N
16–Pin Ceramic DIP	10137F

PIN DESCRIPTION

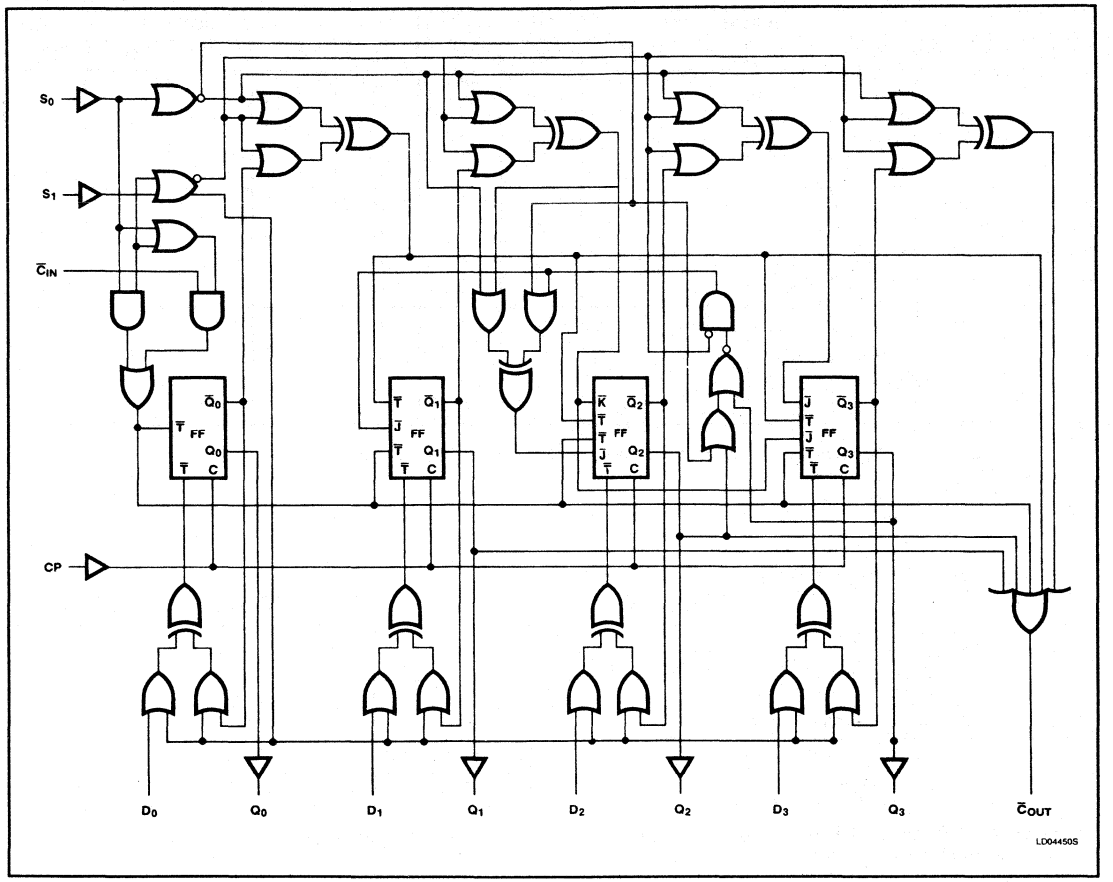
PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
CP	Clock Input
$\overline{C}_{IN}$	Carry–in Input
S_0, S_1	Select Inputs
$\overline{C}_{OUT}$	Carry–out Output
$Q_0 - Q_3$	Data Outputs

PIN CONFIGURATION



Universal Counter 10137

LOGIC DIAGRAM



FUNCTION SELECT TABLE

S_0	S_1	OPERATING MODE
L	L	Preset
L	H	Increment (count up)
H	L	Decrement (count down)
H	H	Hold (stop count)

H = High Voltage Level
L = Low Voltage Level

Universal Counter | 10137

SEQUENTIAL FUNCTION TABLE

INPUTS								OUTPUTS				
S_0	S_1	D_0	D_1	D_2	D_3	$\overline{C}_{IN}$	CP	Q_0	Q_1	Q_2	Q_3	$\overline{C}_{OUT}$
L	L	H	H	H	H	X	↑	H	H	H	L	H
L	H	X	X	X	X	L	↑	L	L	L	H	H
L	H	X	X	X	X	L	↑	H	L	L	H	L
L	H	X	X	X	X	L	↑	L	L	L	L	H
L	H	X	X	X	X	L	↑	H	L	L	L	H
L	H	X	X	X	X	H	L	H	L	L	L	H
L	H	X	X	X	X	H	↑	H	L	L	L	H
H	H	X	X	X	X	X	↑	H	L	L	L	H
L	L	H	H	L	L	X	↑	H	H	L	L	H
H	L	X	X	X	X	L	↑	L	H	L	L	H
H	L	X	X	X	X	L	↑	H	L	L	L	H
H	L	X	X	X	X	L	↑	L	L	L	L	L

NOTE:
This function table shows logic states assuming inputs vary in the sequence shown from top to bottom.
H = High Voltage Level
L = Low Voltage Level
X = Don't Care
↑ = Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 0.010V, T_A = –30°C to +85°C output loading 50Ω to –2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	T_A = –30°C	For Q_n outputs, apply V_{ILMIN} to CP, S_0, and S_1 inputs. After applying V_{IHMAX} to all other inputs, change the CP input from V_{ILMIN} to V_{IHMAX}. For $\overline{C}_{OUT}$, apply V_{ILMIN} to CP, $\overline{C}_{IN}$, S_0, and S_1 inputs. After applying V_{IHMAX} to D_n inputs, change CP from V_{ILMIN} to V_{IHMAX} then change S_0 and $\overline{C}_{IN}$ from V_{ILMIN} to V_{IHMAX}.	–1060		–890	mV
		T_A = +25°C		–960		–810	mV
		T_A = +85°C		–890		–700	mV
V_{OHT}	High level output threshold voltage	T_A = –30°C	For Q_0 output, apply V_{IHT} to D_0 input and V_{ILMIN} to CP, S_0, S_1, and D_1, D_2, and D_3. Raise CP from V_{ILMIN} to V_{IHMAX} and measure Q_0. Repeat this process for Q_1, Q_2, and Q_3 by applying V_{IHT} to D_1, D_2, and D_3, respectively, one at a time. For $\overline{C}_{OUT}$, apply V_{ILMIN} to CP, $\overline{C}_{IN}$, S_0, and S_1 inputs. After applying V_{IHMAX} to D_n inputs, change CP from V_{ILMIN} to V_{IHT}, then change S_0 and $\overline{C}_{IN}$ from V_{ILMIN} to V_{IHMAX}.	–1080			mV
		T_A = +25°C		–980			mV
		T_A = +85°C		–910			mV
V_{OLT}	Low level output threshold voltage	T_A = –30°C	For Q_n outputs, apply V_{ILMIN} to D_n inputs and to CP, S_0, and S_1 inputs. Raise CP from V_{ILMIN} to V_{IHT} and measure Q_n outputs. For $\overline{C}_{OUT}$, apply V_{ILT} to CP, $\overline{C}_{IN}$, S_0, and S_1 inputs. After applying V_{IHMAX} to D_n inputs, change CP from V_{ILMIN} to V_{IHMAX} and measure $\overline{C}_{OUT}$.			–1655	mV
		T_A = +25°C				–1630	mV
		T_A = +85°C				–1595	mV

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to D_n inputs and to CP, S_0, and S_1 inputs. Raise CP from V_{ILMIN} to	−1890		−1675	mV
			$T_A = +25°C$	V_{IHMAX} and measure Q_n outputs. For $\overline{C}_{OUT}$, apply V_{ILMIN} to CP, $\overline{C}_{IN}$, S_0, and S_1 inputs. After applying	−1850		−1650	mV
			$T_A = +85°C$	V_{IHMAX} to D_n inputs, change CP from V_{ILMIN} to V_{IHMAX} and measure $\overline{C}_{OUT}$.	−1825		−1615	mV
I_{IH}	High level input current	D_n inputs	$T_A = -30°C$				350	µA
			$T_A = +25°C$				220	µA
			$T_A = +85°C$				220	µA
		S_0, $\overline{C}_{IN}$ inputs	$T_A = -30°C$				390	µA
			$T_A = +25°C$				245	µA
			$T_A = +85°C$	Apply V_{IHMAX} to each input, under			245	µA
		S_1 input	$T_A = -30°C$	test, one at a time, with V_{IHMAX}			425	µA
			$T_A = +25°C$	applied to all other inputs.			265	µA
			$T_A = +85°C$				265	µA
		CP input	$T_A = -30°C$				460	µA
			$T_A = +25°C$				290	µA
			$T_A = +85°C$				290	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				165	mA
			$T_A = +25°C$			120	150	mA
			$T_A = +85°C$				165	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

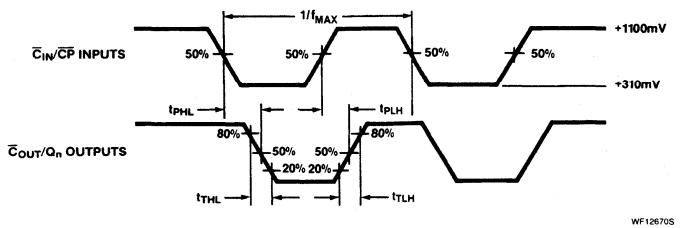
Universal Counter 10137

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

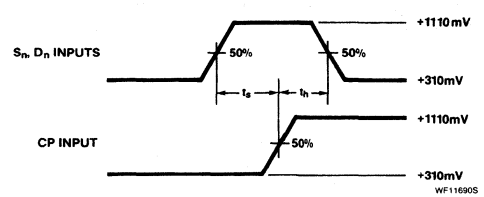
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency	Waveform 1	125		125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1.70 1.70	4.80 4.80	1.70 1.70	3.30 3.30	4.50 4.50	1.70 1.70	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{C}_{OUT}$		2.00 2.00	10.90 10.90	2.50 2.50	7.00 7.00	10.50 10.50	2.50 2.50	11.50 11.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to $\overline{C}_{OUT}$		1.60 1.60	7.40 7.40	1.60 1.60	5.00 5.00	6.90 6.90	1.90 1.90	7.50 7.50	ns ns
t_s	Setup time D_n to CP	Waveform 2	3.50		3.50			3.50		ns
t_h	Hold time CP to D_n		0.00		0.00			0.00		ns
t_s	Setup time S_n to CP		7.50		7.50			7.50		ns
t_h	Hold time CP to S_n		−1.00		−1.00			−1.00		ns
t_s	Setup time $\overline{C}_{IN}$ to CP	Waveform 3	4.50		3.70			4.50		ns
t_h	Hold time CP to $\overline{C}_{IN}$		−1.00		−1.00			−1.00		ns
t_s	Setup time CP to $\overline{C}_{IN}$		−1.00		−1.00			−1.00		ns
t_h	Hold time $\overline{C}_{IN}$ to CP		4.00		3.10			4.00		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	0.90 0.90	3.30 3.30	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.50 3.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

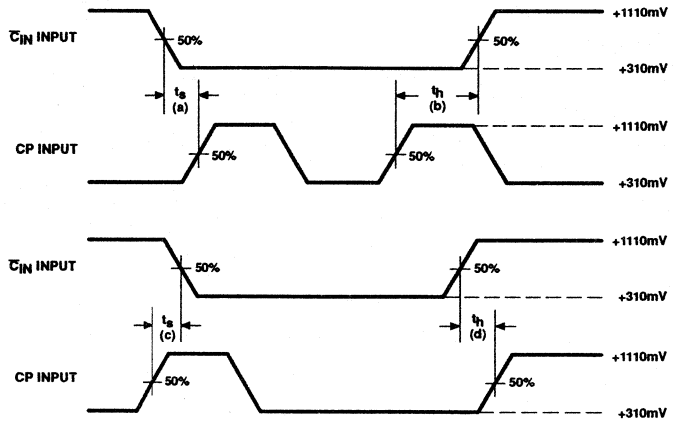
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for CP to Q_n and $\overline{C}_{IN}$ to $\overline{C}_{OUT}$



Waveform 2. Setup and Hold Times for Data and Select to Clock



NOTES:
(a) is the minimum time to wait to clock the counter after it is enabled.
(b) is the minimum time that the counter may be clocked before it is disabled.
(c) is the minimum time that a clock pulse may be applied with no effect on the state of the counter before it is enabled.
(d) is the minimum time to wait before a clock pulse may be applied with no effect on the state of the counter after is is disabled.
(b) and (c) may be negative numbers.

Waveform 3. Setup and Hold Times for $\overline{C}_{IN}$ to CP

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ECL Products	

10141
Shift Register

4-Bit Universal Shift Register

FEATURES

- **Typical propagation delay: 2.9ns**
- **Typical supply current ($-I_{EE}$): 82mA**

DESCRIPTION

The 10141 is a four-bit serial-/parallel-out shift register. Inputs S_0 and S_1 are used to determine the four possible functions of the register, these being no shift, shift left, and parallel entrance of data with no external gating of the clock. The other inputs D_R and D_L are intended for shifting in from the left and the right, while inputs D_0 to D_3 are normal data inputs. All four outputs are capable of driving 50Ω lines. When the register is operating for serial output only, the unused outputs may be left open. All unused inputs must be tied Low to V_{IL} or V_{EE}.

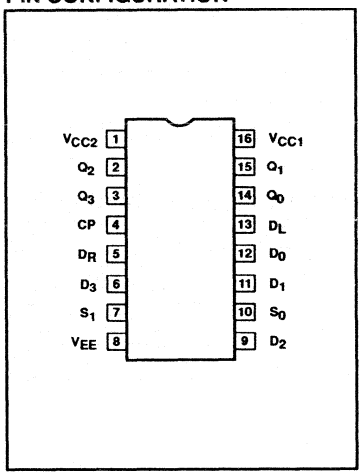
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10141N
16–Pin Ceramic DIP	10141F

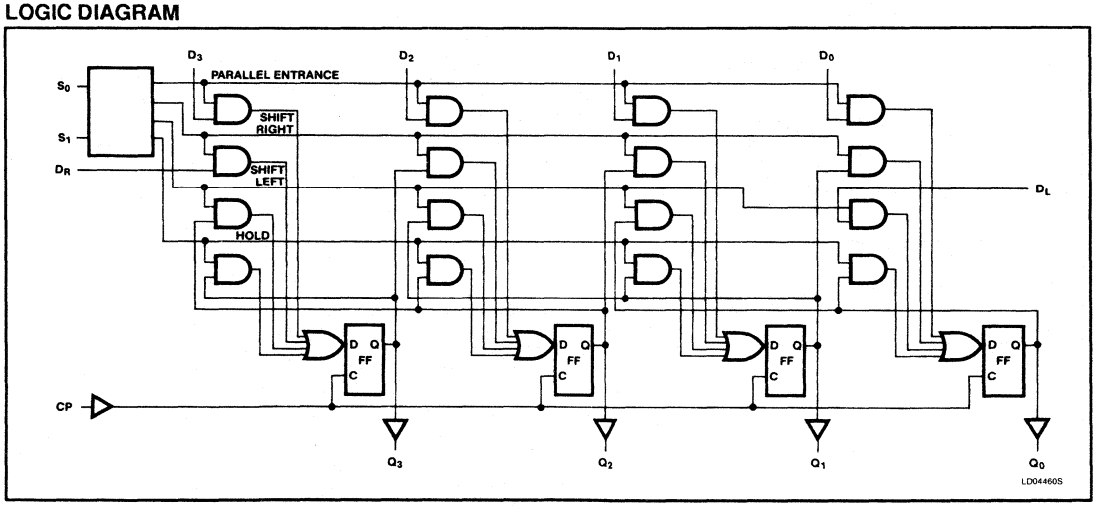
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
CP	Clock Input
S_0, S_1	Select Inputs
D_R	Serial Shift Right Register
D_L	Serial Shift Left Register
$Q_0 - Q_3$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Shift Register | 10141

FUNCTION TABLE

SELECT INPUTS		OPERATION MODE	OUTPUTS			
S_0	S_1		$Q_{0(n+1)}$	$Q_{1(n+1)}$	$Q_{2(n+1)}$	$Q_{3(n+1)}$
L	L	Parallel	D_0	D_1	D_2	D_3
L	H	Shift Right*	Q_{1n}	Q_{2n}	Q_{3n}	D_R
H	L	Shift Left*	D_L	Q_{0n}	Q_{1n}	Q_{2n}
H	H	Stop Shift	Q_{0n}	Q_{1n}	Q_{2n}	Q_{3n}

H = High Voltage Level
L = Low Voltage Level
* Outputs as they exist after pulse at "CP" input with conditions as shown.
Pulse is positive transition of clock (CP) input.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{IHMAX} to D_n inputs and V_{ILMIN} to all	−1060		−890	mV
			$T_A = +25°C$	other inputs. Then raise CP input from V_{ILMIN}	−960		−810	mV
			$T_A = +85°C$	to V_{IHMAX} and measure output.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	Apply V_{IHMAX} to D_n inputs and V_{ILMIN} to all	−1080			mV
			$T_A = +25°C$	other inputs. Then raise CP input from V_{ILMIN}	−980			mV
			$T_A = +85°C$	to V_{IHT} and measure output.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	Apply V_{IHMAX} to all D_n inputs and V_{ILMIN} to all other inputs. Apply a pulse to the CP input from V_{ILMIN} to V_{IHMAX} then back to V_{ILMIN}. Then apply V_{ILMIN} to all D_n inputs, then raise the CP input from V_{ILMIN} to V_{IHT} and measure the output.			−1655	mV
			$T_A = +25°C$				−1630	mV
			$T_A = +85°C$				−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	Apply V_{IHMAX} to CP input	−1890		−1675	mV
			$T_A = +25°C$	with V_{ILMIN} applied to	−1850		−1650	mV
			$T_A = +85°C$	all other inputs.	−1825		−1615	mV
I_{IH}	High level input current	D_n, D_R, D_L inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			350	µA
			$T_A = +25°C$				200	µA
			$T_A = +85°C$				200	µA
		S_0, S_1 inputs	$T_A = -30°C$				390	µA
			$T_A = +25°C$				245	µA
			$T_A = +85°C$				245	µA
		CP input	$T_A = -30°C$	Apply V_{IHMAX} to CP input with V_{ILMIN} applied to all other inputs.			425	µA
			$T_A = +25°C$				265	µA
			$T_A = +85°C$				265	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under test, one at a time, with V_{IHMAX} applied to all other inputs.	0.5			µA
			$T_A = +25°C$		0.5			µA
			$T_A = +85°C$		0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				112	mA
			$T_A = +25°C$			82	102	mA
			$T_A = +85°C$				112	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

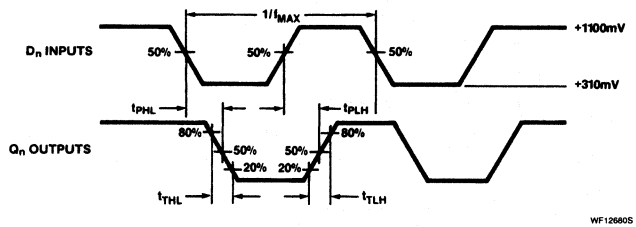
Shift Register 10141

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

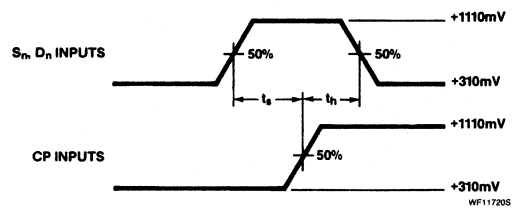
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency	Waveform 1	150		150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.70 1.70	3.90 3.90	1.80 1.80	2.90 2.90	3.80 3.80	2.00 2.00	4.20 4.20	ns ns
t_s	Setup time D_n to CP	Waveform 2	2.50		2.50			2.50		ns
t_h	Hold time CP to D_n		1.50		1.50			1.50		ns
t_s	Setup time S_n to CP		5.50		5.00			5.50		ns
t_h	Hold time CP to S_n		1.50		1.50			1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	3.00 3.00	1.10 1.10	2.00 2.00	3.00 3.00	1.10 1.10	3.00 3.00	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



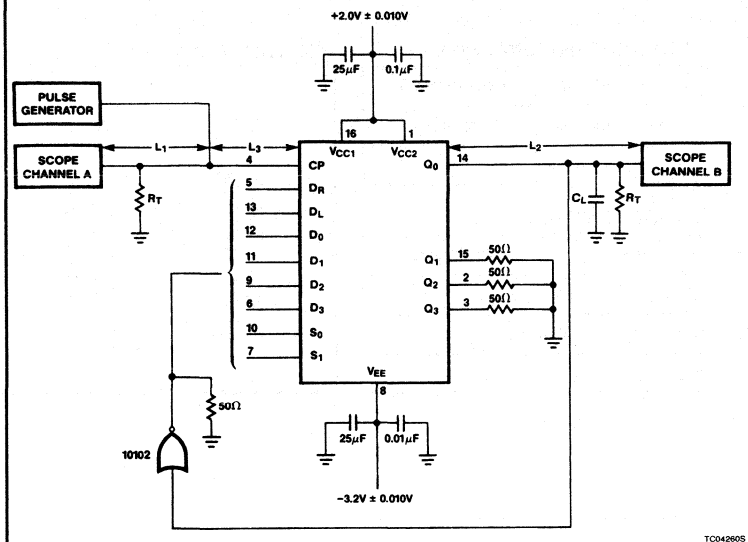
Waveform 1. Propagation Delay and Transition Times for D_n to Q_n and Maximum Clock Frequency



Waveform 2. Setup and Hold Times for Data and Select to Clock

Shift Register 10141

CLOCK FREQUENCY TEST CIRCUIT



NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}, 0.01μF from GND to V_{EE} (0.01 and 0.1uF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 equal length 50Ω impedance lines. L_3 the distance from the DUT pin and the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

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Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10158
Multiplexer

Quad 2-to-1 Multiplexer, Non-Inverting

FEATURES

- **Typical propagation delay: 2.5ns**
- **Typical supply current ($-I_{EE}$): 38mA**

DESCRIPTION

The 10158 is a high-speed, low power, Quad 2-to-1 Multiplexer. With respect to a single control signal (S), it transmits to a common output pin the data present on either of two input pins.

As contrasted with the 10159, the 10158 has no enable input and non-inverting outputs. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage

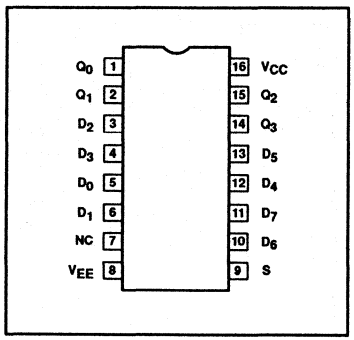
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10158N
16–Pin Ceramic DIP	10158F

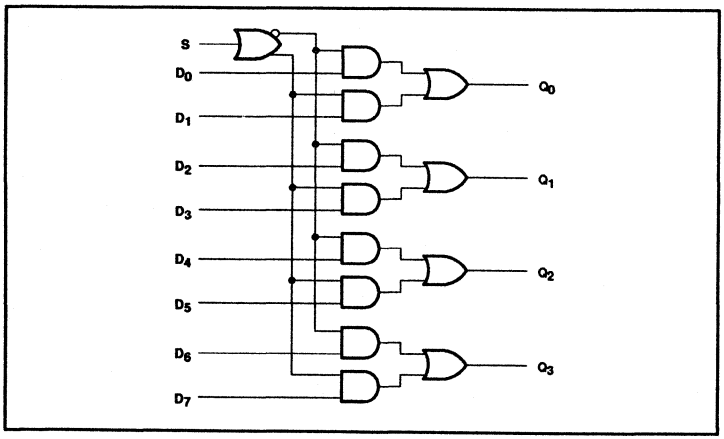
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
S	Select Input
$Q_0 - Q_3$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Multiplexer | 10158

FUNCTION TABLE

INPUTS			OUTPUT
D_0	D_1	S	Q_0
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ground, V_{EE} = −5.2V ± 0.010V, T_A = −30°C to +85°C output loading 50Ω to −2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		T_A = −30°C	For even inputs, apply V_{ILMIN} to S input with	−1060		−890	mV
			T_A = +25°C	V_{IHMAX} applied to all other inputs. For	−960		−810	mV
			T_A = +85°C	odd inputs apply V_{IHMAX} to all inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage		T_A = −30°C	Apply V_{IHT} to D_0 input with V_{ILMIN} applied to S	−1080			mV
			T_A = +25°C	input. Repeat for each even input. Apply V_{IHT} to D_1 input with V_{IHMAX} applied to S input.	−980			mV
			T_A = +85°C	Repeat for each odd input.	−910			mV
V_{OLT}	Low level output threshold voltage		T_A = −30°C	Apply V_{ILT} to D_0 input with V_{ILMIN} applied to S			−1655	mV
			T_A = +25°C	input. Repeat for each even input. Apply V_{ILT} to D_1 input with V_{IHMAX} applied to S input.			−1630	mV
			T_A = +85°C	Repeat for each odd input.			−1595	mV
V_{OL}	Low level output voltage		T_A = −30°C	For even inputs, apply V_{ILMIN} to all inputs.	−1890		−1675	mV
			T_A = +25°C	For odd inputs,, apply V_{IHMAX} to S input	−1850		−1650	mV
			T_A = +85°C	and V_{ILMIN} to all other inputs.	−1825		−1615	mV
I_{IH}	High level input current	S input	T_A = −30°C	Apply V_{IHMAX} to S input			360	µA
			T_A = +25°C	with V_{ILMIN} applied to			225	µA
			T_A = +85°C	all other inputs.			225	µA
		Other inputs	T_A = −30°C	For even inputs, apply V_{IHMAX} to input under test,			400	µA
			T_A = +25°C	one at a time, with V_{ILMIN} applied to all other inputs. For odd inputs, apply V_{IHMAX} to S input and to input			250	µA
			T_A = +85°C	under test, one at a time, with V_{ILMIN} applied to all other inputs.			250	µA
I_{IL}	Low level input current		T_A = −30°C	Apply V_{ILMIN} to each input under	0.5			µA
			T_A = +25°C	test, one at a time, with V_{IHMAX}	0.5			µA
			T_A = +85°C	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		T_A = −30°C				53	mA
			T_A = +25°C			38	46	mA
			T_A = +85°C				53	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		T_A = +25°C			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

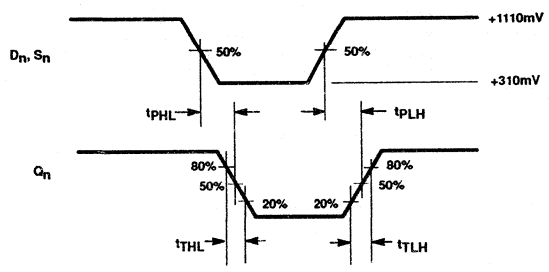
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS V_{CC} = ground, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			T_A = –30°C		T_A = +25°C			T_A = +85°C		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.30	3.10 3.10	1.20	2.50	3.00	1.30	3.20	ns
t_{PLH} t_{PHL}	Propagation delay S to Q_n		2.50	4.80	2.40	3.20	4.50	2.50	4.80	ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.60 1.60	3.40 3.40	1.50 1.50	2.50 2.50	3.30 3.30	1.60 1.60	3.40 3.40	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Philips Components

Document No.	853–0669
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10159
Multiplexer

Quad 2-to-1 Multiplexer, Inverting

FEATURES

- **Typical propagation delay: 2.5ns**
- **Typical supply current ($-I_{EE}$): 42mA**

DESCRIPTION

The 10159 is a high-speed, low power, Quad 2-to-1 Multiplexer.

With respect to a single control signal, (S), it transmits to a common output pin the data present on either of two input pins.

As contrasted with the 10158, the 10159 has a common output enable input ($\overline{OE}$) and inverting outputs.

All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

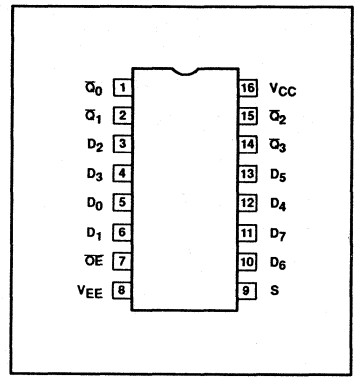
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10159N
16–Pin Ceramic DIP	10159F

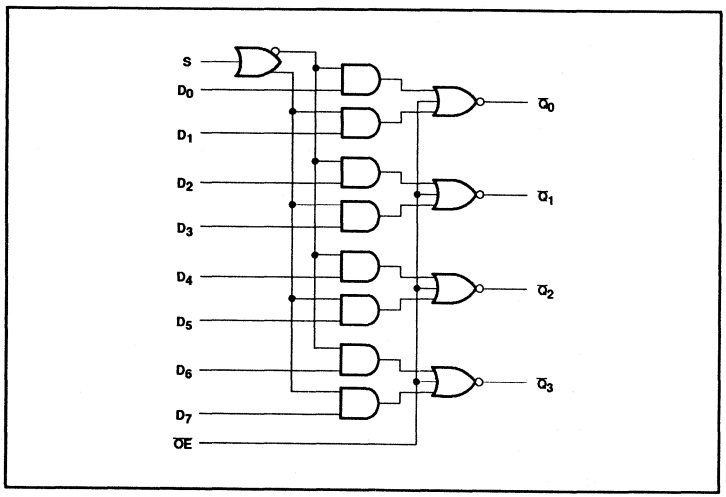
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
S	Select Input
$\overline{OE}$	Output Enable Input
$\overline{Q}_0 - \overline{Q}_3$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Multiplexer | 10159

FUNCTION TABLE

INPUTS				OUTPUT
D_0	D_1	S	$\overline{OE}$	$\overline{Q}_0$
X	X	X	H	L
L	X	L	L	H
H	X	L	L	L
X	L	H	L	H
X	H	H	L	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ground, V_{EE} = –5.2V ± 0.010V, T_A = –30°C to +85°C output loading 50Ω to –2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		T_A = –30°C	For even inputs, apply V_{ILMIN} to all inputs.	–1060		–890	mV
			T_A = +25°C	For odd inputs apply V_{IHMAX} to S input	–960		–810	mV
			T_A = +85°C	and V_{ILMIN} to all other inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage		T_A = –30°C	For even inputs, apply V_{ILT} to S input with V_{ILMIN}	–1080			mV
			T_A = +25°C	applied to all other inputs. For odd inputs, apply	–980			mV
			T_A = +85°C	V_{IHT} to S input with V_{ILMIN} applied to all other inputs.	–910			mV
V_{OLT}	Low level output threshold voltage		T_A = –30°C	Apply V_{IHT} to $\overline{OE}$ input			–1655	mV
			T_A = +25°C	with V_{ILMIN} applied to			–1630	mV
			T_A = +85°C	all other inputs.			–1595	mV
V_{OL}	Low level output voltage		T_A = –30°C	Apply V_{IHMAX} to $\overline{OE}$ input	–1890		–1675	mV
			T_A = +25°C	with V_{ILMIN} applied to	–1850		–1650	mV
			T_A = +85°C	all other inputs.	–1825		–1615	mV
I_{IH}	High level input current	S input	T_A = –30°C	Apply V_{IHMAX} to S input			360	µA
			T_A = +25°C	with V_{ILMIN} applied to			225	µA
			T_A = +85°C	all other inputs.			225	µA
		Other inputs	T_A = –30°C	Apply V_{IHMAX} to $\overline{OE}$ or D_n input under			400	µA
			T_A = +25°C	test, one at a time, with V_{ILMIN} applied			250	µA
			T_A = +85°C	to all other inputs.			250	µA
I_{IL}	Low level input current		T_A = –30°C	Apply V_{ILMIN} to each input under	0.5			µA
			T_A = +25°C	test, one at a time, with V_{IHMAX}	0.5			µA
			T_A = +85°C	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		T_A = –30°C				58	mA
			T_A = +25°C			42	53	mA
			T_A = +85°C				58	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		T_A = +25°C			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

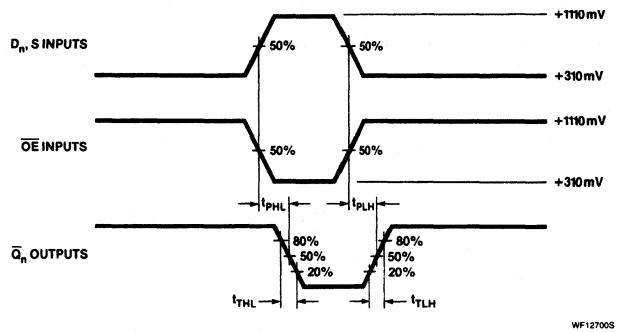
Multiplexer 10159

AC ELECTRICAL CHARACTERISTICS V_{CC} = ground, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			T_A = –30°C		T_A = +25°C			T_A = +85°C		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 1	1.10 1.10	3.80 3.80	1.20 1.20	2.50 2.50	3.30 3.30	1.10 1.10	3.80 3.80	ns ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Q}_n$		1.50 1.50	5.30 5.30	1.50 1.50	3.20 3.20	5.00 5.00	1.50 1.50	5.30 5.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to $\overline{Q}_n$		1.40 1.40	5.30 5.30	1.50 1.50	2.50 2.50	5.00 5.00	1.40 1.40	5.30 5.30	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.00 1.00	3.70 3.70	1.10 1.10	2.50 2.50	3.50 3.50	1.00 1.00	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Philips Components

Document No.	853–0670
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10160
Parity Checker/Generator

12-Bit Parity Checker/Generator

FEATURES

- **Typical propagation delay: 5.0ns**
- **Typical supply current ($-I_{EE}$): 62mA**

DESCRIPTION

The 10160 is a 12-bit Parity Checker or Generator. The output goes High when and odd number on inputs are High. If parity detection or generation is required for less than 12 bits, all unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

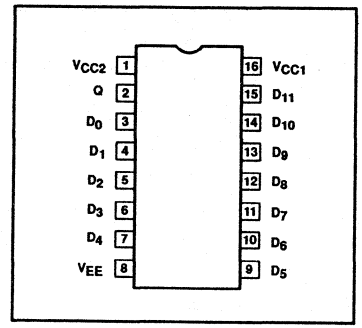
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10160N
16–Pin Ceramic DIP	10160F

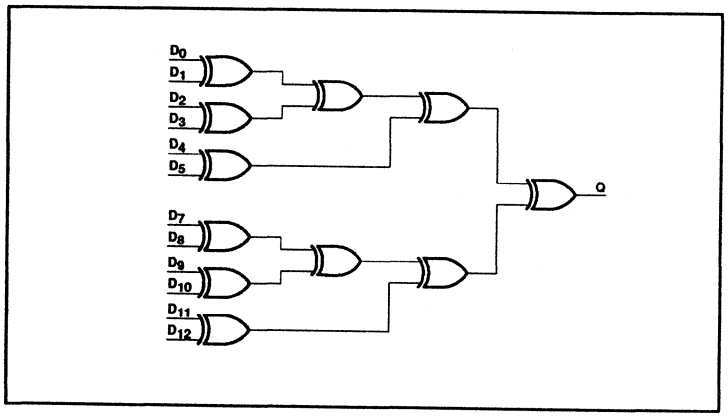
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_{11}$	Data Inputs
Q	Data Output

PIN CONFIGURATION



LOGIC DIAGRAM



Parity Checker/Generator 10160

FUNCTION TABLE

SUM OF INPUTS AT HIGH STATE	Q
Odd	H
Even	L

H = High Voltage Level
L = Low Voltage Level

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

Parity Checker/Generator 10160

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{IHMAX} to each input,	−1060		−890	mV
			$T_A = +25°C$	one at a time with V_{ILMIN}	−960		−810	mV
			$T_A = +85°C$	applied to all other inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	Apply V_{IHT} to each input,	−1080			mV
			$T_A = +25°C$	one at a time with V_{ILMIN}	−980			mV
			$T_A = +85°C$	applied to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	Apply V_{ILT} to each input,			−1655	mV
			$T_A = +25°C$	one at a time with V_{ILMIN}			−1630	mV
			$T_A = +85°C$	applied to all other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	Apply V_{IHMAX} to all inputs	−1890		−1675	mV
			$T_A = +25°C$	or apply V_{ILMIN} to all inputs.	−1850		−1650	mV
			$T_A = +85°C$		−1825		−1615	mV
I_{IH}	High level input current	Input pins 3, 6, 7, 11 12, 15	$T_A = -30°C$				425	µA
			$T_A = +25°C$	Apply V_{IHMAX} to each input under			265	µA
			$T_A = +85°C$	test, one at a time, with V_{ILMIN}			265	µA
		Other inputs	$T_A = -30°C$	applied to all other inputs.			350	µA
			$T_A = +25°C$				220	µA
			$T_A = +85°C$				220	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$	Apply V_{IHMAX} to input			86	mA
			$T_A = +25°C$	pins 4, 5, 9, 10, 13, 14		62	78	mA
			$T_A = +85°C$	and V_{ILMIN} to all other pins.			86	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

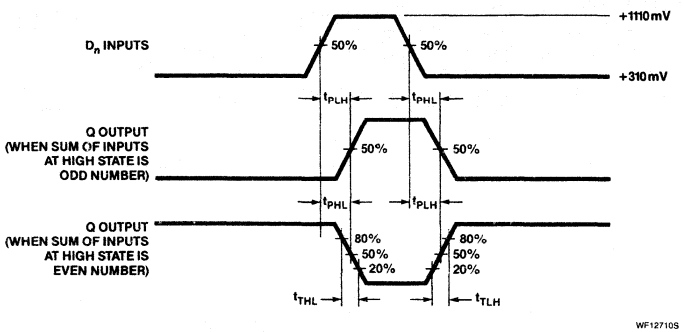
Parity Checker/Generator 10160

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay $A_0 - A_{11}$ to Q_n	Waveform 1	1.80 1.80	8.10 8.10	2.00 2.00	5.00 5.00	7.50 7.50	2.00 2.00	8.00 8.00	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.10 1.10	3.50 3.50	1.10 1.10	2.00 2.00	3.30 3.30	1.00 1.00	3.50 3.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0671
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10161
Decoder

1-of-8 Decoder with 3 Enable Inputs (Active-LOW Outputs)

FEATURES

- **Typical propagation delay: 4.0ns**
- **Typical supply current ($-I_{EE}$): 61mA**

DESCRIPTION

The 10161 accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually-exclusive Active-LOW outputs ($Q_0 - Q_7$). The device features two Active-LOW enable inputs. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

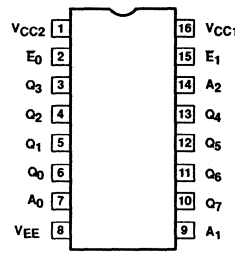
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10161N
16–Pin Ceramic DIP	10161F

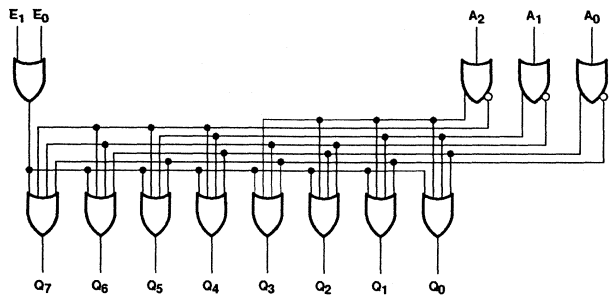
PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_2$	Address Inputs
$\overline{E}_0$, $\overline{E}_1$	Enabled Inputs (Active–LOW)
$Q_0 - Q_7$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



A_0 to A_2: binary inputs; $\overline{E}_0$, $\overline{E}_1$: enable inputs; Q_0 to Q_7: coded outputs

Decoder | 10161

FUNCTION TABLE

ENABLE INPUTS		BINARY INPUTS			DECIMAL OUTPUTS							
E_0	E_1	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
H	H	X	X	X	H	H	H	H	H	H	H	H
L	H	X	X	X	H	H	H	H	H	H	H	H
H	L	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to $\overline{E}_0$ input,	−1060		−890	mV
		$T_A = +25°C$	with V_{ILMIN} applied	−960		−810	mV
		$T_A = +85°C$	to all other inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{IHT} to $\overline{E}_0$ input,	−1080			mV
		$T_A = +25°C$	with V_{ILMIN} applied	−980			mV
		$T_A = +85°C$	to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Using V_{IHMAX} and V_{ILMIN}, apply a functional			−1655	mV
		$T_A = +25°C$	pattern as indicated in the Function Table, substituting V_{IHT} for V_{IHMAX} and V_{ILT} for			−1630	mV
		$T_A = +85°C$	V_{ILMIN} on one input at a time and measure V_{OLT} on the respective output.			−1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	Using V_{IHMAX} and V_{ILMIN}, apply a functional	−1890		−1675	mV
		$T_A = +25°C$	pattern as indicated in the Function Table,	−1850		−1650	mV
		$T_A = +85°C$	and measure V_{OL} on the respective output.	−1825		−1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under			350	µA
		$T_A = +25°C$	test, one at a time, with V_{ILMIN}			220	µA
		$T_A = +85°C$	applied to all other inputs.			220	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
		$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
		$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$	Apply V_{IHMAX} to pins			84	mA
		$T_A = +25°C$	2, 7, 9, 14, 15 and		61	76	mA
		$T_A = +85°C$	V_{ILMIN} to all other inputs.			84	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation	$T_A = +25°C$			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation	$T_A = +25°C$			0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

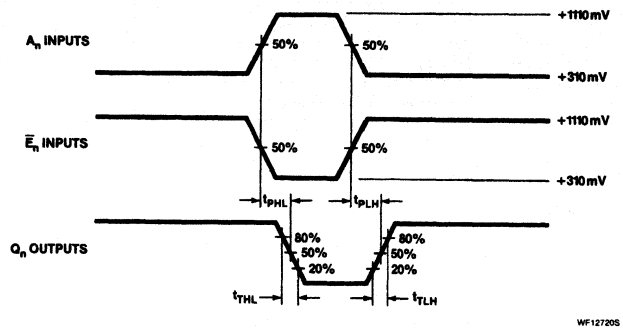
Decoder 10161

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH}	Propagation delay	Waveform 1	1.50	6.20	1.50	4.00	6.00	1.50	6.40	ns
t_{PHL}	$\overline{E}_n$, A_n to Q_n		1.50	6.20	1.50	4.00	6.00	1.50	6.40	ns
t_{TLH}	Transition time		1.00	3.30	1.10	2.00	3.30	1.10	3.50	ns
t_{THL}	20% to 80%, 80% to 20%		1.00	3.30	1.10	2.00	3.30	1.10	3.50	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



NOTE:
Output waveform (a) or (b) depends on particular input and output under test.

Waveform 1. Propagation Delay and Transition Times

Document No.	853–0672
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10162
Decoder

1-of-8 Decoder with 2 Enable Inputs (Active-HIGH Outputs)

FEATURES

- **Typical propagation delay: 4.0ns**
- **Typical supply current ($-I_{EE}$): 61mA**

DESCRIPTION

The 10162 accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually-exclusive Active-HIGH outputs ($Q_0 - Q_7$). The device features two Active-LOW enable inputs. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

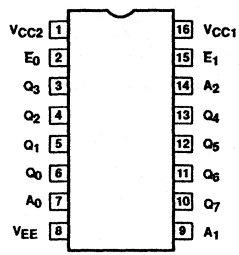
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic DIP	10162N
16-Pin Ceramic DIP	10162F

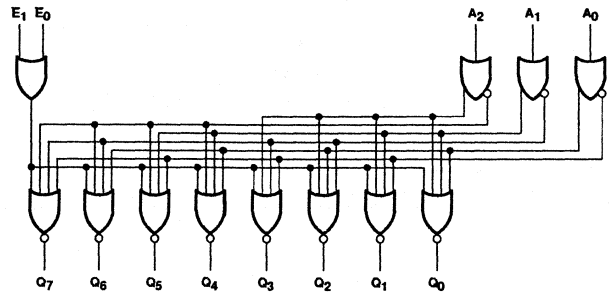
PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_2$	Address Inputs
$\overline{E}_0$, $\overline{E}_1$	Enable Inputs (Active-LOW)
$Q_0 - Q_7$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



A_0 to A_2: binary inputs; $\overline{E}_0$, $\overline{E}_1$: enable inputs; Q_0 to Q_7: coded outputs

Decoder 10162

FUNCTION TABLE

ENABLE INPUTS		BINARY INPUTS			DECIMAL OUTPUTS							
$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
H	H	X	X	X	L	L	L	L	L	L	L	L
L	H	X	X	X	L	L	L	L	L	L	L	L
H	L	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	L	L	L	L	H	L	L	L	L
L	L	L	L	H	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Apply V_{IHMAX} and V_{ILMIN}, apply a functional	−1060		−890	mV
		$T_A = +25°C$	pattern as indicated in the Function Table	−960		−810	mV
		$T_A = +85°C$	and measure V_{OH} on the respective outputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{IHMAX} and V_{ILMIN}, apply a functional	−1080			mV
		$T_A = +25°C$	pattern as indicated in the Function Table, substituting V_{IHT} for V_{IHMAX} and V_{ILT} for	−980			mV
		$T_A = +85°C$	V_{ILMIN} on one input at a time and measure V_{OHT} on the respective output.	−910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Apply V_{ILMIN} to $\overline{E}_0$ input			−1655	mV
		$T_A = +25°C$	and V_{IHT} to $\overline{E}_1$ input. Apply V_{ILMIN}			−1630	mV
		$T_A = +85°C$	to $\overline{E}_1$ input and V_{IHT} to $\overline{E}_0$ input.			−1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to $\overline{E}_0$ input and	−1890		−1675	mV
		$T_A = +25°C$	V_{ILMIN} to $\overline{E}_1$ input. Apply	−1850		−1650	mV
		$T_A = +85°C$	V_{IHMAX} to all inputs.	−1825		−1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under			350	µA
		$T_A = +25°C$	test, one at a time, with V_{ILMIN}			220	µA
		$T_A = +85°C$	applied to all other inputs.			220	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
		$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
		$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				84	mA
		$T_A = +25°C$			61	76	mA
		$T_A = +85°C$				84	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

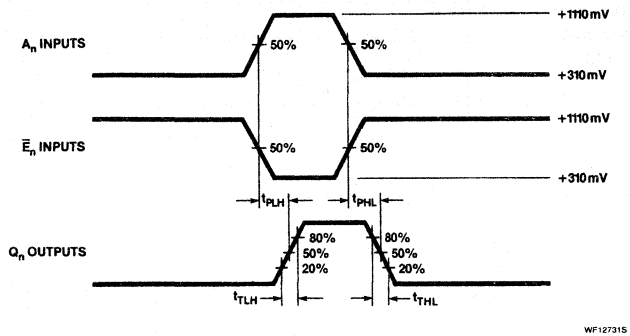
Decoder 10162

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay E_n, A_n to Q_n	Waveform 1	1.50 1.50	6.20 6.20	1.50 1.50	4.00 4.00	6.00 6.00	1.50 1.50	6.40 6.40	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.00 1.00	3.30 3.30	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.50 3.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0673
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10164
Multiplexer

8-Input Multiplexer with Enable Input

FEATURES

- **Typical propagation delay: 3.0ns**
- **Typical supply current ($-I_{EE}$): 60mA**

DESCRIPTION

The 10164 performs 8-input multiplexing with enable input. The output goes LOW when not enabled, thus permitting expansion of multiplexers by wire-ORing. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

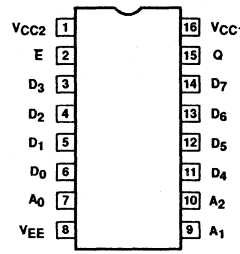
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10164N
16–Pin Ceramic DIP	10164F
16–Pin SO	10164D

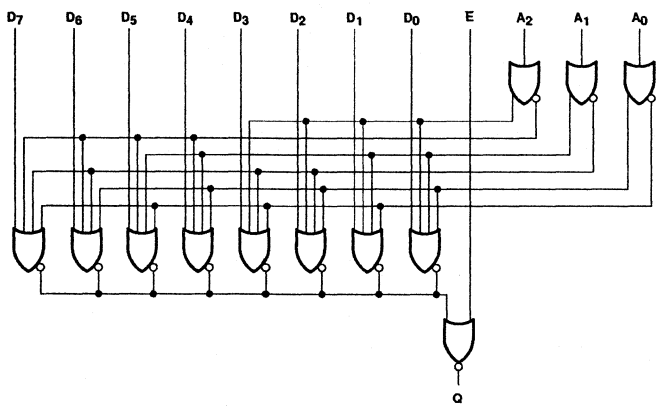
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
$A_0 - A_2$	Address Inputs
$\overline{E}$	Enable Input
Q	Data Output

PIN CONFIGURATION



LOGIC DIAGRAM



A_0 to A_2 = address inputs; D_0 to D_7 = data inputs; E = enable input

Multiplexer 10164

FUNCTION TABLE

INPUTS												OUTPUT
A_0	A_1	A_2	$\overline{E}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q
L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	H	X	X	X	X	X	X	X	H
H	L	L	L	X	L	X	X	X	X	X	X	L
H	L	L	L	X	H	X	X	X	X	X	X	H
L	H	L	L	X	X	L	X	X	X	X	X	L
L	H	L	L	X	X	H	X	X	X	X	X	H
H	H	L	L	X	X	X	L	X	X	X	X	L
H	H	L	L	X	X	X	H	X	X	X	X	H
L	L	H	L	X	X	X	X	L	X	X	X	L
L	L	H	L	X	X	X	X	H	X	X	X	H
H	L	H	L	X	X	X	X	X	L	X	X	L
H	L	H	L	X	X	X	X	X	H	X	X	H
L	H	H	L	X	X	X	X	X	X	L	X	L
L	H	H	L	X	X	X	X	X	X	H	X	H
H	H	H	L	X	X	X	X	X	X	X	L	L
H	H	H	L	X	X	X	X	X	X	X	H	H
X	X	X	H	X	X	X	X	X	X	X	X	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Using V_{IHMAX} and V_{ILMIN}, apply a functional	−1060		−890	mV
		$T_A = +25°C$	pattern as indicated in the Function Table	−960		−810	mV
		$T_A = +85°C$	and measure V_{OH} on the output.	−890		−700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{ILT} to $\overline{E}$ input and apply a functional	−1080			mV
		$T_A = +25°C$	pattern using V_{IHMAX} and V_{ILMIN} as indicated in the Function Table and	−980			mV
		$T_A = +85°C$	measure V_{OHT} on the output.	−910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Apply V_{IHT} to $\overline{E}$ input			−1655	mV
		$T_A = +25°C$	with V_{IHMAX} applied			−1630	mV
		$T_A = +85°C$	to all other inputs.			−1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to all inputs. Apply	−1890		−1675	mV
		$T_A = +25°C$	V_{IHMAX} to $\overline{E}$ input. with V_{ILMIN}	−1850		−1650	mV
		$T_A = +85°C$	applied to all other inputs.	−1825		−1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IMAX} to each input under			425	µA
		$T_A = +25°C$	test, one at a time, with V_{ILMIN}			265	µA
		$T_A = +85°C$	applied to all other inputs.			265	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
		$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
		$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				83	mA
		$T_A = +25°C$			60	75	mA
		$T_A = +85°C$				83	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

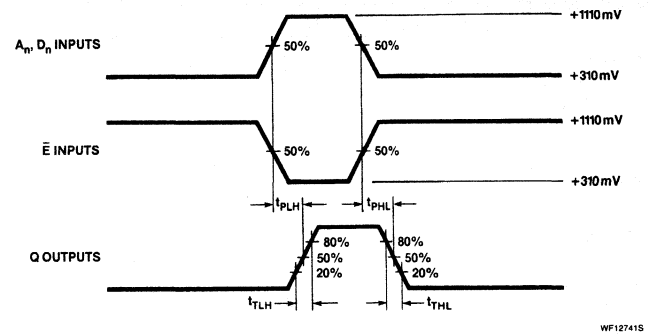
Multiplexer 10164

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q	Waveform 1	1.50 1.50	4.70 4.70	1.50 1.50	3.00 3.00	4.50 4.50	1.60 1.60	4.80 4.80	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q		1.90 1.90	6.30 6.30	2.00 2.00	4.00 4.00	6.00 6.00	2.20 2.20	6.50 6.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\bar{E}$ to Q		0.90 0.90	3.30 3.30	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.10 3.10	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		0.90 0.90	3.30 3.30	1.10 1.10	2.00 2.00	3.30 3.30	1.20 1.20	3.60 3.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Address and Data Input to Outputs

Document No.	853–0674
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10165
Priority Encoder/Latch

8-Input Priority Encoder

FEATURES

- **Typical propagation delay: 4.5ns**
- **Typical supply current ($-I_{EE}$): 105mA**

DESCRIPTION

The 10165 is able to encode eight inputs to binary coded outputs. Each output is stored in a D-type latch which allows synchronous operation. When the clock input is Low the outputs follow the inputs and latch when the clock goes High. The output code is that of the highest order input so that any input of lower priority is ignored.

The input is active when High (e.g., the three binary outputs are Low when input D_0 is High). Output Q_3 is High when any input is High, which allows direct extension into another priority encoder when more than 8 inputs are used.

The device can be used in many applications, such as testing systems and checking system status in control processors processors and peripheral controllers. It can also be used to generate binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

All unused inputs must be tied Low to V_{IL} or V_{EE}.

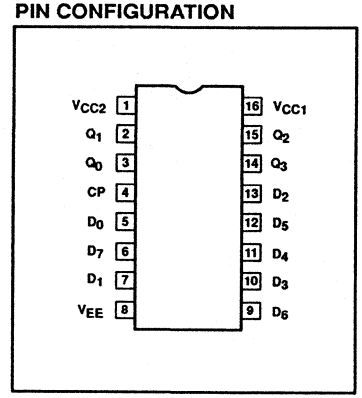
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10165N
16–Pin Ceramic DIP	10165F

PIN DESCRIPTION

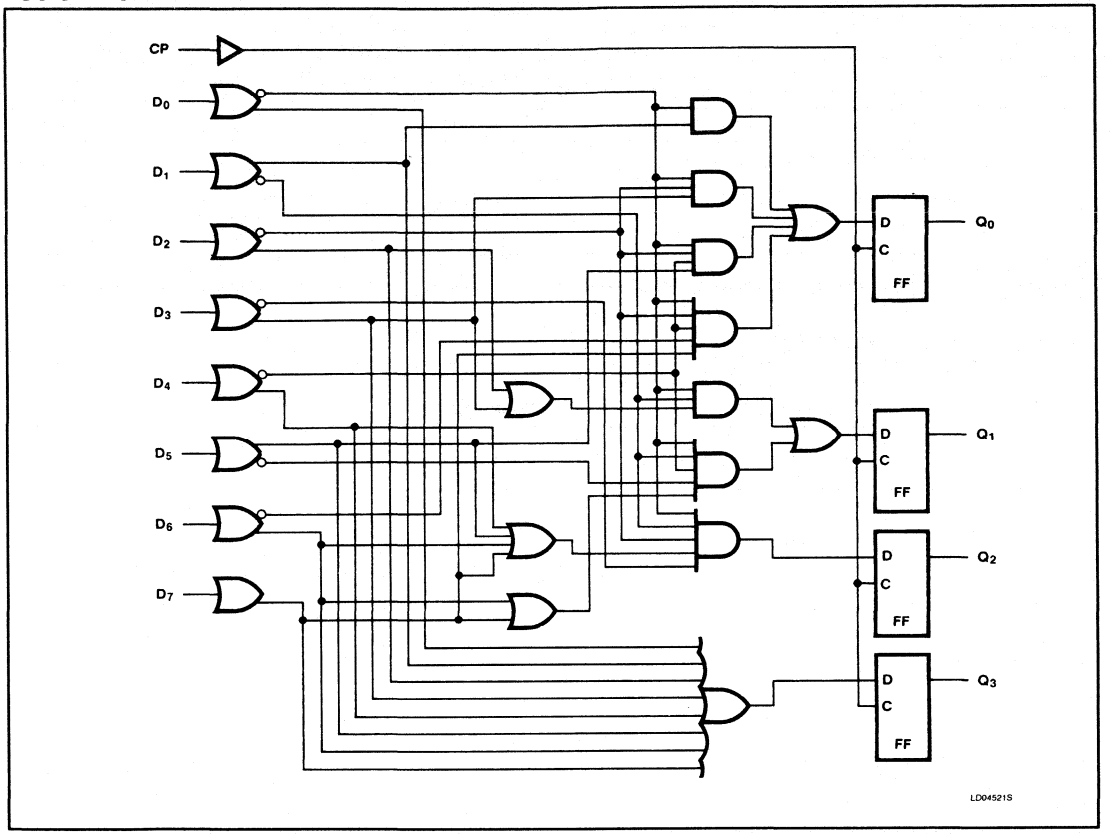
PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
CP	Clock Input
$Q_0 - Q_3$	Data Outputs

PIN CONFIGURATION



Priority Encoder/Latch 10165

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								OUTPUTS			
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q_3	Q_2	Q_1	Q_0
H	X	X	X	X	X	X	X	H	L	L	L
L	H	X	X	X	X	X	X	H	L	L	H
L	L	H	X	X	X	X	X	H	L	H	L
L	L	L	H	X	X	X	X	H	L	H	H
L	L	L	L	H	X	X	X	H	H	L	L
L	L	L	L	L	H	X	X	H	H	L	H
L	L	L	L	L	L	H	X	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to D_7 input	−1060		−890	mV
		$T_A = +25°C$	with V_{ILMIN} applied to	−960		−810	mV
		$T_A = +85°C$	all other inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{IHT} to D_7 input	−1080			mV
		$T_A = +25°C$	with V_{ILMIN} applied to	−980			mV
		$T_A = +85°C$	all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Apply V_{ILT} to CP input			−1655	mV
		$T_A = +25°C$	with V_{ILMIN} applied			−1630	mV
		$T_A = +85°C$	to all other inputs.			−1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$		−1890		−1675	mV
		$T_A = +25°C$	Apply V_{ILMIN} to all inputs.	−1850		−1650	mV
		$T_A = +85°C$		−1825		−1615	mV
I_{IH}	High level input current — CP Input	$T_A = -30°C$	Apply V_{IHMAX} to CP input			390	µA
		$T_A = +25°C$	with V_{ILMIN} applied			245	µA
		$T_A = +85°C$	to all other inputs.			245	µA
	High level input current — Other Inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under			350	µA
		$T_A = +25°C$	test, one at a time, with V_{ILMIN}			220	µA
		$T_A = +85°C$	applied to all other inputs.			220	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
		$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
		$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				144	mA
		$T_A = +25°C$			105	131	mA
		$T_A = +85°C$				144	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

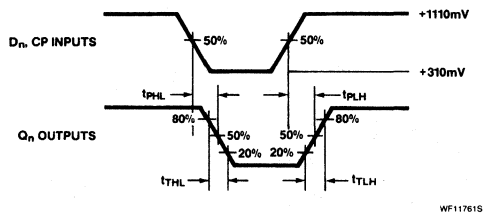
Priority Encoder/Latch 10165

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

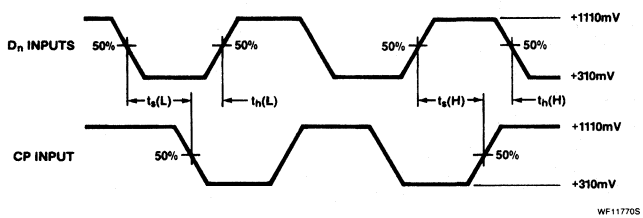
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	2.00 2.00	7.00 7.00	3.00 3.00	4.50 4.50	7.00 7.00	2.00 2.00	8.00 8.00	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1.50 1.50	4.50 4.50	2.00 2.00	4.50 4.50	4.00 4.00	1.50 1.50	4.50 4.50	ns ns
$t_s(H)$ $t_s(L)$	Setup time D_n to CP	Waveform 2	6.00 6.00		6.00 6.00	3.40 3.00		6.00 6.00		ns ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		1.00 1.00		1.00 1.00	−2.30 −2.70		1.00 1.00		ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.10 1.10	3.50 3.50	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.50 3.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Data to Output



Waveform 2. Setup and Hold Times for Data to Clock

Document No.	853–0675
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10171
Decoder

Dual 1-of-4 Decoder with One Common and Two Individual Inputs (Active-LOW Outputs)

FEATURES

- **Typical propagation delay: 4.0ns**
- **Typical supply current ($-I_{EE}$): 65mA**

DESCRIPTION

The 10171 is a Dual 1-of-4 Decoder with common address inputs, one common ($\overline{E}$) and two individual enable ($\overline{E}_0$, $\overline{E}_1$) inputs.

The common enable ($\overline{E}$), when High, forces all outputs High. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

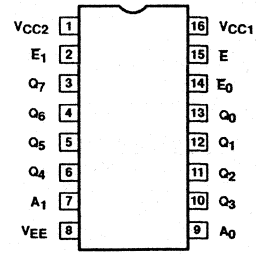
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10171N
16–Pin Ceramic DIP	10171F

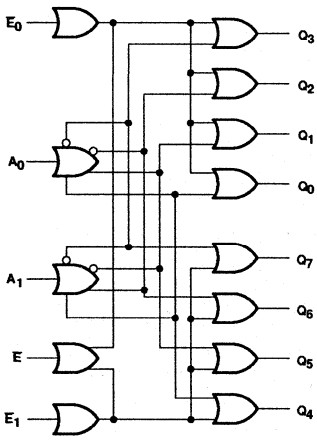
PIN DESCRIPTION

PINS	DESCRIPTION
A_0, A_1	Address Inputs
$\overline{E}$, $\overline{E}_0$, $\overline{E}_1$	Enable Inputs
$Q_0 - Q_7$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Decoder 10171

FUNCTION TABLE

ENABLE INPUTS			INPUTS		OUTPUTS							
$\overline{E}$	$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	Q_4	Q_5	Q_6	Q_7	Q_0	Q_1	Q_2	Q_3
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	X	X	X	X	H	H	H	H	H	H	H	H

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to $\overline{E}$ input	−1060		−890	mV
		$T_A = +25°C$	with V_{ILMIN} applied to	−960		−810	mV
		$T_A = +85°C$	all other inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{IHT} to $\overline{E}$ input	−1080			mV
		$T_A = +25°C$	with V_{ILMIN} applied to	−980			mV
		$T_A = +85°C$	all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	For Q_0 and Q_4 outputs, apply V_{ILT} to $\overline{E}$			−1655	mV
		$T_A = +25°C$	input with V_{ILMIN} applied to all other inputs. Apply functional pattern to A_0 and A_1 for			−1630	mV
		$T_A = +85°C$	other output combinations.			−1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	For Q_0 and Q_4 outputs, apply V_{ILMIN} to	−1890		−1675	mV
		$T_A = +25°C$	all inputs. Apply functional pattern to A_0	−1850		−1650	mV
		$T_A = +85°C$	and A_1 for other output combinations.	−1825		−1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under			350	µA
		$T_A = +25°C$	test, one at a time, with V_{ILMIN}			220	µA
		$T_A = +85°C$	applied to all other inputs.			220	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
		$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
		$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$	Apply V_{IHMAX} to inputs.			85	mA
		$T_A = +25°C$			65	77	mA
		$T_A = +85°C$				85	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation	$T_A = +25°C$			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation	$T_A = +25°C$			0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

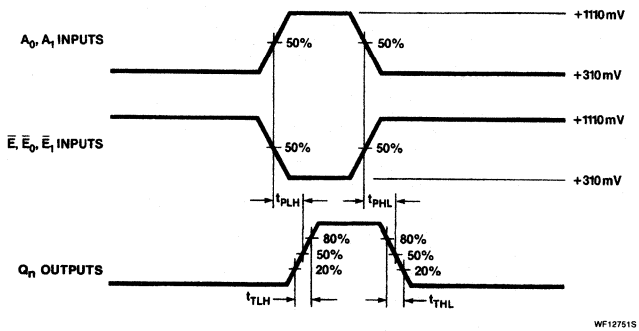
Decoder 10171

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_0, A_1 to Q_n	Waveform 1	1.50 1.50	6.20 6.20	1.50 1.50	4.00 4.00	6.00 6.00	1.50 1.50	6.40 6.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$, $\overline{E}_0$, $\overline{E}_1$ to Q_n		1.50 1.50	6.20 6.20	1.50 1.50	4.00 4.00	6.00 6.00	1.50 1.50	6.40 6.40	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.00 1.00	3.30 3.30	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.40 3.40	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Address to Output

Document No.	853–0676
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10172
Decoder

Dual 1-of-4 Decoder with One Common and Two Individual Inputs (Active-HIGH Outputs)

FEATURES

- **Typical propagation delay: 4.0ns**
- **Typical supply current ($-I_{EE}$): 62mA**

DESCRIPTION

The 10172 is a Dual 1-of -4 Decoder with common address inputs, one common and two individual enable (E_0, E_1) inputs. The common Enable ($\overline{E}$), when High, forces all outputs Low. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

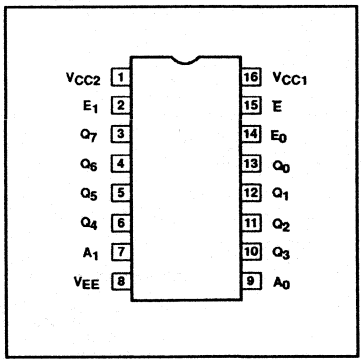
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10172N
16–Pin Ceramic DIP	10172F

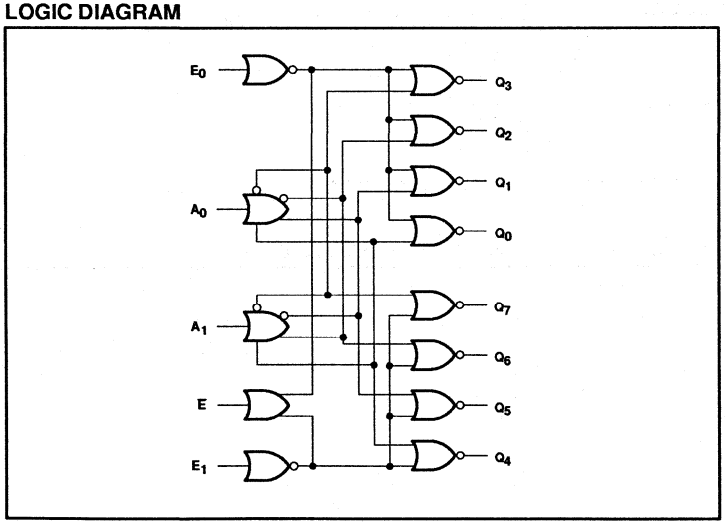
PIN DESCRIPTION

PINS	DESCRIPTION
A_0, A_1	Address Inputs
$\overline{E}$, E_0, E_1	Enable Inputs
$Q_0 - Q_7$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Decoder 10172

FUNCTION TABLE

ENABLE INPUTS			INPUTS		OUTPUTS							
$\overline{E}$	E_1	E_0	A_1	A_2	Q_4	Q_5	Q_6	Q_7	Q_0	Q_1	Q_2	Q_3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	L	L	L	L	H	L	L	L
H	X	X	X	X	L	L	L	L	L	L	L	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	For Q_0 and Q_4 outputs, apply V_{IHMAX}	−1060		−890	mV
		$T_A = +25°C$	to E_0 and E_1 inputs with V_{ILMIN} applied	−960		−810	mV
		$T_A = +85°C$	to all other inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	For Q_0 output, apply V_{IHT}	−1080			mV
		$T_A = +25°C$	to E_1 input with V_{ILMIN}	−980			mV
		$T_A = +85°C$	applied to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Apply V_{IHT} to $\overline{E}$ input			−1655	mV
		$T_A = +25°C$	with V_{ILMIN} applied to all			−1630	mV
		$T_A = +85°C$	other inputs.			−1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to $\overline{E}$ input	−1890		−1675	mV
		$T_A = +25°C$	with V_{ILMIN} applied to	−1850		−1650	mV
		$T_A = +85°C$	all other inputs.	−1825		−1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under			350	µA
		$T_A = +25°C$	test, one at a time, with V_{ILMIN}			220	µA
		$T_A = +85°C$	applied to all other inputs.			220	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
		$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
		$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				85	mA
		$T_A = +25°C$			62	77	mA
		$T_A = +85°C$				85	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

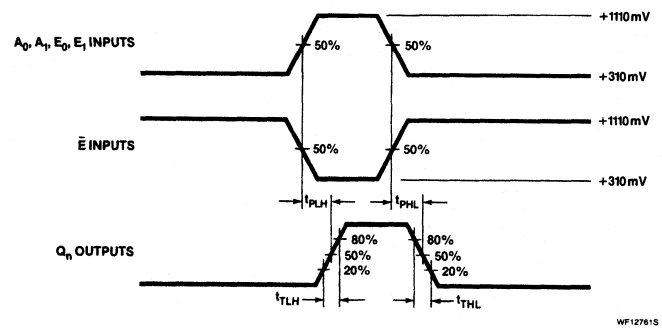
Decoder 10172

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, E_n to Q_n	Waveform 1	1.50 1.50	6.20 6.20	1.50 1.50	4.00 4.00	6.00 6.00	1.50 1.50	6.40 6.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\bar{E}$ to Q_n		1.50 1.50	6.20 6.20	1.50 1.50	4.00 4.00	6.00 6.00	1.50 1.50	6.40 6.40	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.00 1.00	3.30 3.30	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.40 3.40	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Address and Enable Inputs to Outputs

Document No.	853–0677
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10173
Multiplexer/Latch

Quad 2-Input Multiplexer with Latched Outputs

FEATURES

- **Typical propagation delay: 2.5ns**
- **Typical supply current ($-I_{EE}$): 53mA**

DESCRIPTION

The 10173 is a quad 2-input multiplexer with latched outputs. Each multiplexer has two inputs, selected by the common Select (S) input. Outputs are latched when the clock is High. All unused inputs must be tied Low to V_{IL} or V_{EE}.

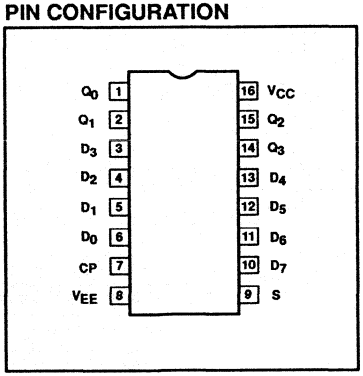
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10173N
16–Pin Ceramic DIP	10173F

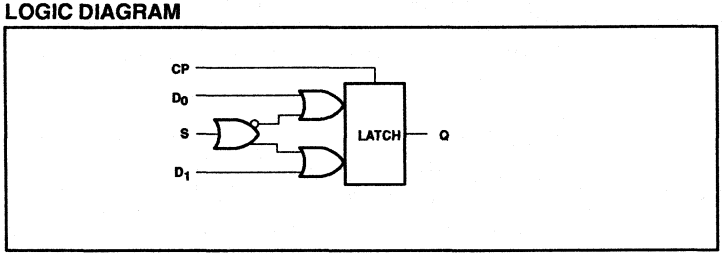
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
S	Select Input
CP	Clock Input
$Q_0 - Q_3$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
S	CP	Q_{n+1}
H	L	D_0
L	L	D_1
X	H	Q_n

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ground, V_{EE} = –5.2V ± 0.010V, T_A = –30°C to +85°C output loading 50Ω to –2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		T_A = –30°C	Apply V_{IHMAX} to D_1 input	–1060		–890	mV
			T_A = +25°C	with V_{ILMIN} applied to D_0,	–960		–810	mV
			T_A = +85°C	CP and S inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage		T_A = –30°C	Apply V_{IHT} to D_1 input	–1080			mV
			T_A = +25°C	with V_{ILMIN} applied to D_0,	–980			mV
			T_A = +85°C	CP and S inputs.	–910			mV
V_{OLT}	Low level output threshold voltage		T_A = –30°C	Apply V_{ILT} to D_1 input			–1655	mV
			T_A = +25°C	with V_{ILMIN} applied to all			–1630	mV
			T_A = +85°C	other inputs.			–1595	mV
V_{OL}	Low level output voltage		T_A = –30°C		–1890		–1675	mV
			T_A = +25°C	Apply V_{ILMIN} to all inputs.	–1850		–1650	mV
			T_A = +85°C		–1825		–1615	mV
I_{IH}	High level input current	D_n inputs	T_A = –30°C	Apply V_{IHMAX} to each input under			470	µA
			T_A = +25°C	test, one at a time, with V_{ILMIN}			295	µA
			T_A = +85°C	applied to all other inputs.			295	µA
		S, CP inputs	T_A = –30°C	Apply V_{IHMAX} to S and CP inputs			400	µA
			T_A = +25°C	under test, one at a time, with			250	µA
			T_A = +85°C	V_{ILMIN} applied to all other inputs.			250	µA
I_{IL}	Low level input current		T_A = –30°C	Apply V_{ILMIN} to each input	0.5			µA
			T_A = +25°C	one at a time, with V_{IHMAX}	0.5			µA
			T_A = +85°C	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		T_A = –30°C				73	mA
			T_A = +25°C			53	66	mA
			T_A = +85°C				73	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		T_A = +25°C			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

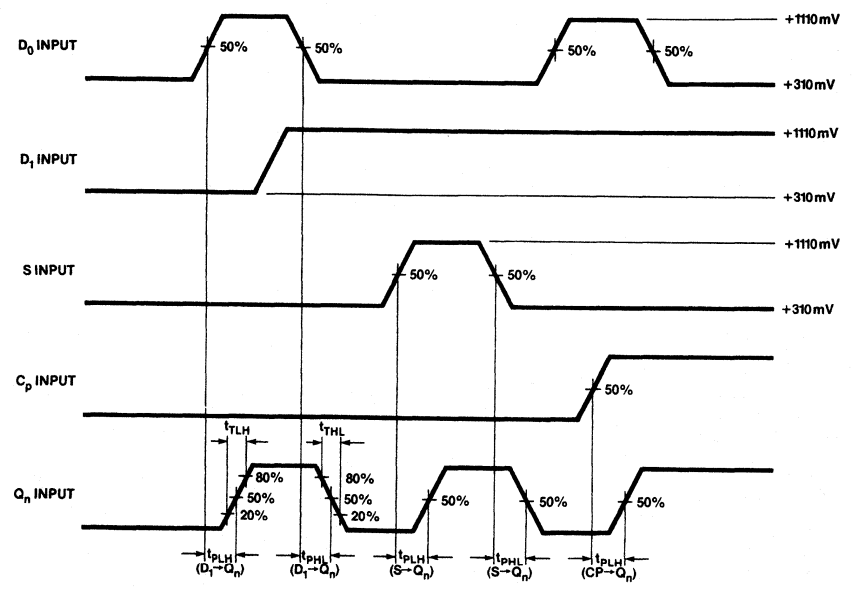
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS V_{CC} = ground, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			T_A = –30°C		T_A = +25°C			T_A = +85°C		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	0.80 0.80	3.70 3.70	1.00 1.00	2.50 2.50	3.50 3.50	1.10 1.10	5.30 5.30	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1.60 1.60	7.20 7.20	1.60 1.60	4.50 4.50	6.80 6.80	1.40 1.40	6.80 6.80	ns ns
t_{PLH} t_{PHL}	Propagation delay S to Q_n		1.10 1.10	6.20 6.20	1.30 1.30	3.50 3.50	5.70 5.70	1.20 1.20	6.70 6.70	ns ns
t_s	Setup time D_n to CP	Waveform 2	2.00		2.00	1.50		2.00		ns
t_h	Hold time D_n to CP		2.50		2.50	0		2.50		ns
t_s	Setup time S to CP		3.00		3.00	2.50		3.00		ns
t_h	Hold time S to CP		1.50		1.50	0.50		1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.20 1.20	4.00 4.00	1.50 1.50	2.00 2.00	3.50 3.50	1.40 1.40	4.00 4.00	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

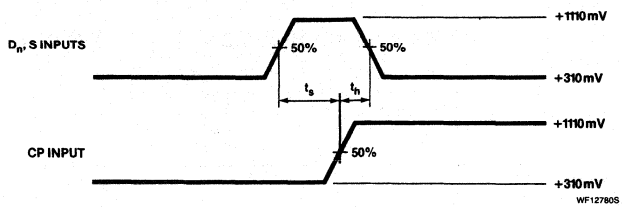
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Data to Output

Multiplexer/Latch 10173

AC WAVEFORMS



Waveform 2. Setup and Hold Times for Data and Select to Clock

Document No.	853–0680
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10174
Multiplexer

Dual 4-to-1 Multiplexer (with Output Enable)

FEATURES

- **Typical propagation delay: 3.5ns**
- **Typical supply current ($-I_{EE}$): 58mA**

DESCRIPTION

The 10174 is a Dual 4-to-1 Multiplexer with output enable input. The 10174 performs two 4-input multiplexer functions. The output of each multiplexer reflects one of the 4 data inputs determined by the states on the two select inputs. An enable input is provided for easy bit expansion by wire-ORing several multiplexers. Each output will go Low with the enable input in the High state. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

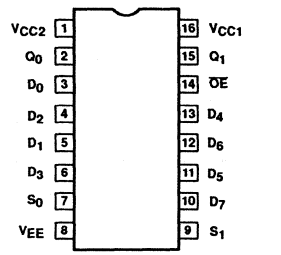
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10174N
16–Pin Ceramic DIP	10174F

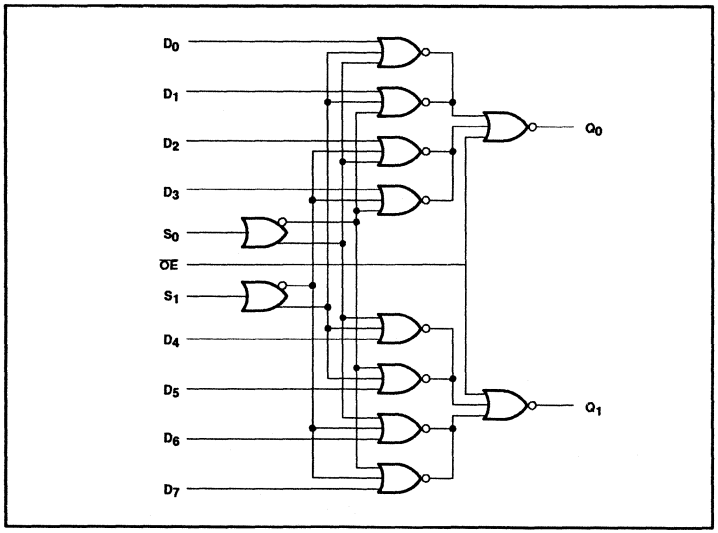
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
S_0, S_1	Select Inputs
$\overline{OE}$	Output Enable Input
Q_0, Q_1	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Multiplexer | 10174

FUNCTION TABLE

INPUTS			OUTPUTS	
S_0	S_1	$\overline{OE}$	Q_0	Q_1
L	L	L	D_0	D_4
H	L	L	D_1	D_5
L	H	L	D_2	D_6
H	H	L	D_3	D_7
X	X	H	L	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{IHMAX} to D_0 and D_4	−1060		−890	mV
			$T_A = +25°C$	inputs, with V_{ILMIN} applied	−960		−810	mV
			$T_A = +85°C$	to all other inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	Apply V_{IHT} to D_0 input, with V_{ILMIN} applied to	−1080			mV
			$T_A = +25°C$	all other inputs. Measure Q_0. Apply V_{IHT} to	−980			mV
			$T_A = +85°C$	D_4 input, with V_{ILMIN} applied to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	Apply V_{IHT} to $\overline{OE}$ input			−1655	mV
			$T_A = +25°C$	with V_{ILMIN} applied to all			−1630	mV
			$T_A = +85°C$	other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	Apply V_{IHMAX} to $\overline{OE}$ input	−1890		−1675	mV
			$T_A = +25°C$	with V_{ILMIN} applied to all	−1850		−1650	mV
			$T_A = +85°C$	other inputs.	−1825		−1615	mV
I_{IH}	High level input current	Other inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under			350	µA
			$T_A = +25°C$	test, one at a time, with V_{ILMIN}			220	µA
			$T_A = +85°C$	applied to all other inputs.			220	µA
		$\overline{OE}$ input	$T_A = -30°C$	Apply V_{IHMAX} to $\overline{OE}$ input			525	µA
			$T_A = +25°C$	with V_{ILMIN} applied to all			310	µA
			$T_A = +85°C$	other inputs.			330	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				80	mA
			$T_A = +25°C$			58	73	mA
			$T_A = +85°C$				80	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

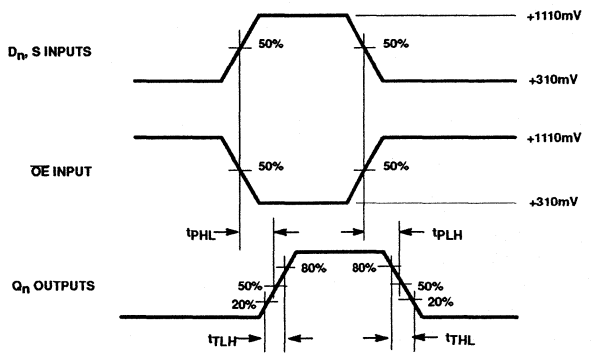
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.40 1.40	4.80 4.80	1.50 1.50	3.50 3.50	4.50 4.50	1.40 1.40	4.80 4.80	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n		1.90 1.90	6.40 6.40	2.00 2.00	5.00 5.00	6.00 6.00	2.10 2.10	6.40 6.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n		1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	2.90 2.90	0.90 0.90	3.20 3.20	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.00 1.00	3.40 3.40	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.60 3.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0679
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10175
Latch

Quint D-Latch with Common Reset and 2 Wired-OR Common Clock Inputs

FEATURES

- **Typical propagation delay: 2.5ns**
- **Typical supply current ($-I_{EE}$): 78mA**

DESCRIPTION

The 10175 includes five D-latches with common reset and two wired-OR common clock inputs. When the clock is in the High state, any change of the data input does not affect the output state. When the clock is in the Low state, any change of the data input is transferred at the output. The outputs are latched on the positive transition of the clock. The reset input is enabled only when the Clock is High. All unused inputs must be tied Low to V_{IL} or V_{EE}.

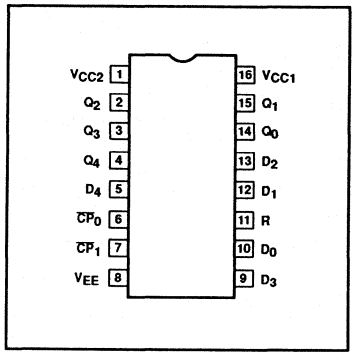
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10175N
16–Pin Ceramic DIP	10175F

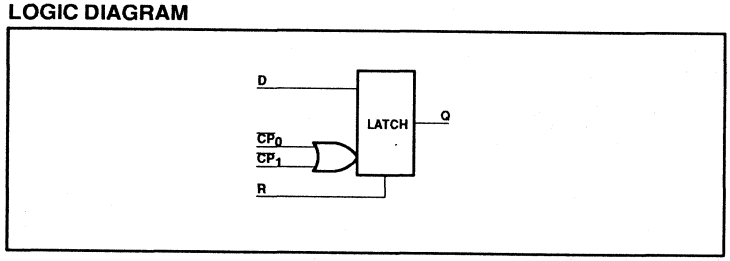
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_4$	Data Inputs
$\overline{CP}_0$, $\overline{CP}_1$	Clock Inputs
R	Reset Input
$Q_0 - Q_4$	Data Outputs

PIN CONFIGURATION

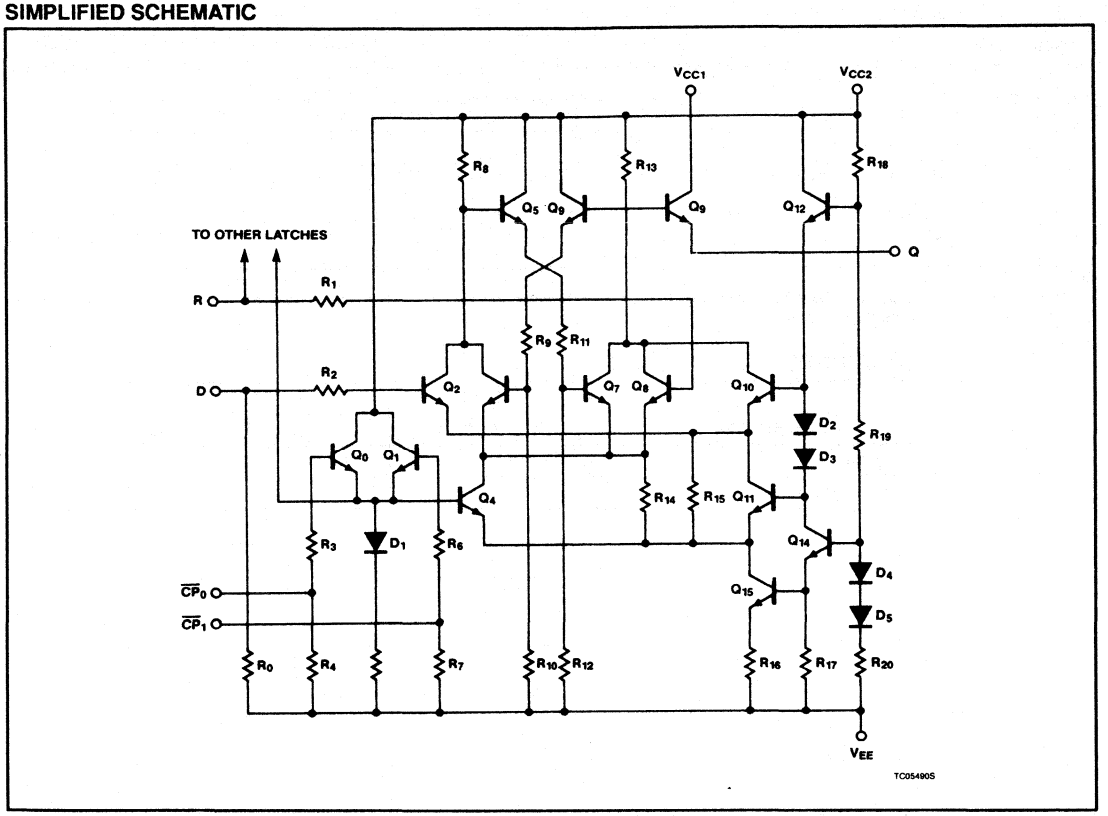


LOGIC DIAGRAM



Latch 10175

SIMPLIFIED SCHEMATIC



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{CP}_0$	$\overline{CP}_1$	R	D	Q_{n+1}
L	L	X	L	L
L	L	X	H	H
H	X	L	X	Q_n
X	H	L	X	Q_n
H	X	H	X	L
X	H	H	X	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 0.010V, T_A = –30°C to +85°C output loading 50Ω to –2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		T_A = –30°C	Apply V_{IHMAX} to each D_n	–1060		–890	mV
			T_A = +25°C	input, with V_{ILMIN} applied	–960		–810	mV
			T_A = +85°C	to all other inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage		T_A = –30°C	Apply V_{IHT} to each D_n, one	–1080			mV
			T_A = +25°C	at a time, with V_{ILMIN} applied	–980			mV
			T_A = +85°C	to all other inputs.	–910			mV
V_{OLT}	Low level output threshold voltage		T_A = –30°C	Apply V_{ILT} to each input, one			–1655	mV
			T_A = +25°C	at a time, with V_{ILMIN} applied			–1630	mV
			T_A = +85°C	to all other inputs.			–1595	mV
V_{OL}	Low level output voltage		T_A = –30°C		–1890		–1675	mV
			T_A = +25°C	Apply V_{ILMIN} to all inputs.	–1850		–1650	mV
			T_A = +85°C		–1825		–1615	mV
I_{IH}	High level input current	Other inputs	T_A = –30°C	Apply V_{IHMAX} to each input under			480	µA
			T_A = +25°C	test, one at a time, with V_{ILMIN}			290	µA
			T_A = +85°C	applied to all other inputs.			290	µA
		R input	T_A = –30°C	Apply V_{IHMAX} to R input			1000	µA
			T_A = +25°C	with V_{ILMIN} applied to all			650	µA
			T_A = +85°C	other inputs.			650	µA
I_{IL}	Low level input current		T_A = –30°C	Apply V_{ILMIN} to each input under	0.5			µA
			T_A = +25°C	test, one at a time, with V_{IHMAX}	0.5			µA
			T_A = +85°C	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		T_A = –30°C				107	mA
			T_A = +25°C			78	97	mA
			T_A = +85°C				107	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		T_A = +25°C			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

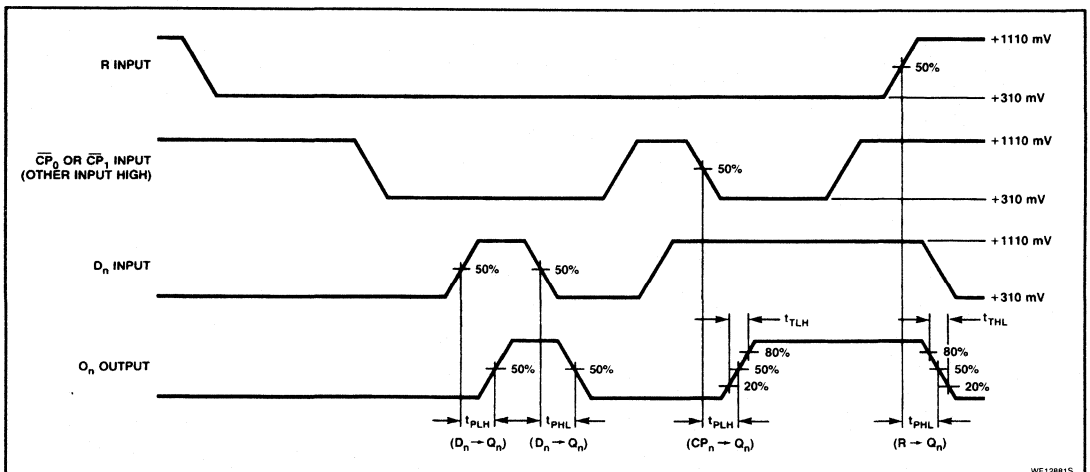
Latch 10175

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

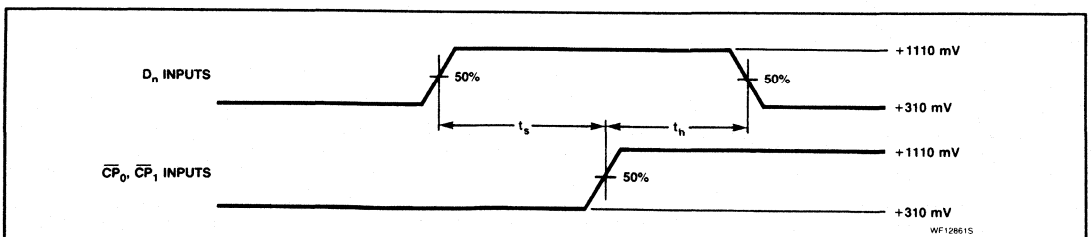
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	3.60 3.60	1.00 1.00	2.50 2.50	3.50 3.50	1.00 1.00	3.60 3.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_n		1.00 1.00	4.70 4.70	1.00 1.00		4.30 4.30	1.00 1.00	4.40 4.40	ns ns
t_{PLH} t_{PHL}	Propagation delay R to Q_n		1.00 1.00	4.00 4.00	1.00 1.00		3.90 3.90	1.00 1.00	4.20 4.20	ns ns
t_s	Setup time D_n to $\overline{CP}_n$	Waveform 2	2.50		2.50			2.50		ns
t_h	Hold time D_n to $\overline{CP}_n$	Waveform 2	1.50		1.50			1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	3.60 3.60	1.10 1.10		3.50 3.50	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times



Waveform 2. Setup and Hold Times for Data to Clock

Document No.	853–0678
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10176
Flip-Flop

Hex D-Type Master-Slave Flip-Flop

FEATURES

- **Typical propagation delay: 150MHz**
- **Typical supply current ($-I_{EE}$): 88mA**

DESCRIPTION

The 10176 includes six high-speed master-slave D-type flip-flops with one common input Clock for all six. Data enters into the master during the Low-State of the clock and is transferred to the slave during the positive-going Clock transition. Due to the master-slave structure of the device, a change in the information present at the data (D_n) input will not modify the output information at any other time. All unused inputs must be tied Low to V_{IL} or V_{EE}.

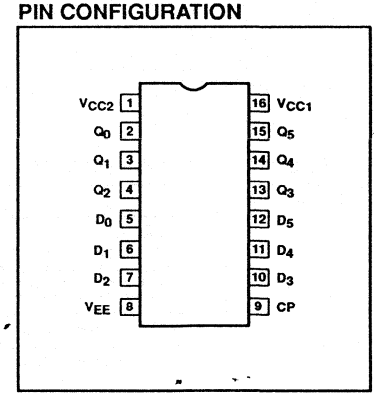
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic DIP	10176N
16-Pin Ceramic DIP	10176F

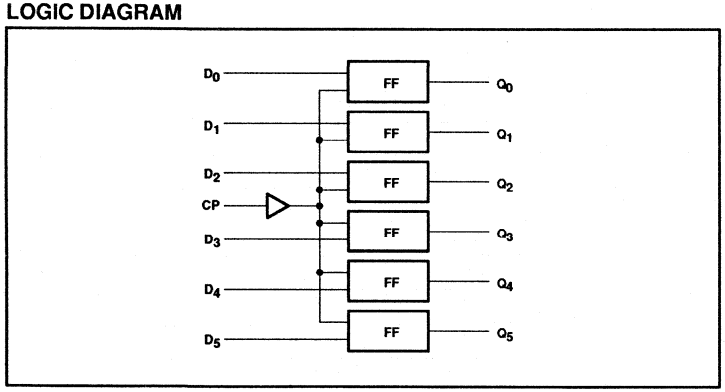
PIN DESCRIPTION

PINS	DESCRIPTION
D_0 - D_5	Data Inputs
CP	Clock Input
Q_0 - Q_5	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Flip–Flop 10176

FUNCTION TABLE

INPUTS		OUTPUTS
CP	D_n	Q_{n+1}
L	X	Q_n
H	L	L
H	H	H

H = High Voltage Level = 1
L = Low Voltage Level = 0
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 0.010V, T_A = –30°C to +85°C output loading 50Ω to –2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		T_A = –30°C	Apply V_{ILMIN} to CP input with V_{IHMAX}	–1060		–890	mV
			T_A = +25°C	applied to all other inputs. Raise CP from	–960		–810	mV
			T_A = +85°C	V_{ILMIN} to V_{IHMAX} and measure V_{OH}.	–890		–700	mV
V_{OHT}	High level output threshold voltage		T_A = –30°C	Apply V_{ILMIN} to CP input with V_{IHMAX}	–1080			mV
			T_A = +25°C	applied to all other inputs. Raise CP from	–980			mV
			T_A = +85°C	V_{ILMIN} to V_{IHT} and measure V_{OHT}.	–910			mV
V_{OLT}	Low level output threshold voltage		T_A = –30°C	Apply V_{ILMIN} to all inputs. Raise			–1655	mV
			T_A = +25°C	CP input from V_{ILMIN} to			–1630	mV
			T_A = +85°C	V_{IHT} and measure V_{OLT}.			–1595	mV
V_{OL}	Low level output voltage		T_A = –30°C	Apply V_{ILMIN} to all inputs. Raise	–1890		–1675	mV
			T_A = +25°C	CP input from V_{ILMIN} to	–1850		–1650	mV
			T_A = +85°C	V_{IHMAX}. Measure V_{OL}.	–1825		–1615	mV
I_{IH}	High level input current	Other inputs	T_A = –30°C	Apply V_{IHMAX} to each D_n input under			350	µA
			T_A = +25°C	test, one at a time, with V_{ILMIN}			220	µA
			T_A = +85°C	applied to all other inputs.			220	µA
		CP input	T_A = –30°C	Apply V_{IHMAX} to CP input			495	µA
			T_A = +25°C	with V_{ILMIN} applied to all			310	µA
			T_A = +85°C	other inputs.			310	µA
I_{IL}	Low level input current		T_A = –30°C	Apply V_{ILMIN} to each input under	0.5			µA
			T_A = +25°C	test, one at a time, with V_{IHMAX}	0.5			µA
			T_A = +85°C	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		T_A = –30°C				121	mA
			T_A = +25°C			88	101	mA
			T_A = +85°C				121	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		T_A = +25°C			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

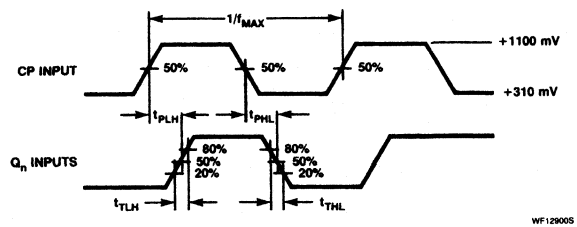
Flip–Flop 10176

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

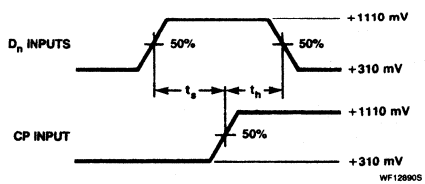
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency	Waveform 1	125		125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1.60 1.60	4.60 4.60	1.60 1.60		4.50 4.50	1.60 1.60	5.00 5.00	ns ns
t_s	Setup time D_n to CP	Waveform 2	2.50		2.50			2.50		ns
t_h	Hold time D_n to CP	Waveform 2	1.50		1.50			1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	4.10 4.10	1.10 1.10		4.00 4.00	1.10 1.10	4.40 4.40	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for CP to Q_n



Waveform 2. Setup and Hold Times for D_n to CP

Document No.	853–0681
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10179
Look-Ahead Carry Block

FEATURES
- **Typical propagation delay: 2.3ns**
- **Typical supply current ($-I_{EE}$): 58mA**

DESCRIPTION
The 10179 is a Look-Ahead Carry Block. It can be used in conjunction with the 10181 4-bit arithmetic/logic unit to perform a high order look-ahead carry, in applications requiring high-speed arithmetic operation on long words. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

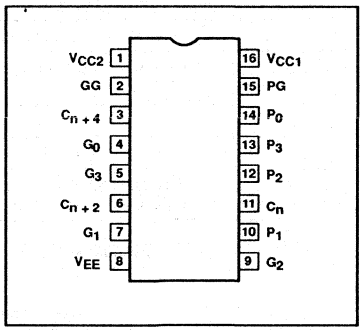
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10179N
16–Pin Ceramic DIP	10179F

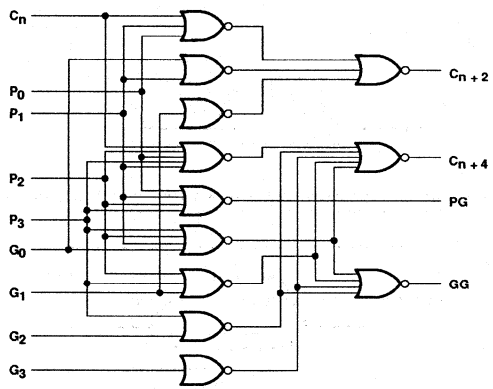
PIN DESCRIPTION

PINS	DESCRIPTION
C_n	Carry Input
$P_0 - P_3$	Carry Propagate Inputs
$G_0 - G_3$	Carry Generate Inputs
C_{n+2}, C_{n+4}	Carry Outputs
PG	Carry Propagate Output
GG	Carry Generate Output

PIN CONFIGURATION



LOGIC DIAGRAM



LOGIC FUNCTIONS
$PG = P_1 + P_2 + P_3 + P_4$, $P_n = P_{n-1}$
$G_G = G_4 (G_3 + P_4) (G_2 + P_3 + P_4) (G_1 + P_2 + P_3 + P_4)$, $G_n = G_{n-1}$, $P_n = P_{n-1}$
$C_{n+2} = G_2 (G_1 + P_2) (C_n + P_1 + P_2)$, $G_n = G_{n-1}$, $P_n = P_{n-1}$
$C_{n+4} = G_4 (G_3 + P_4) (G_2 + G_3 + P_4) (G_1 + P_2 + P_3 + P_4) (C_n + P_1 + P_2 + P_3 + P_4)$, $G_n = G_{n-1}$, $P_n = P_{n-1}$
The overall carry function is invariant with the polarity (positive or negative) of the logic if the P and G inputs are interchanged.

Look–Ahead Carry Block 10179

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For GG output, apply V_{IHMAX}	–1060		–890	mV
			$T_A = +25°C$	to all G_n inputs with V_{ILMIN}	–960		–810	mV
			$T_A = +85°C$	applied to all other inputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For GG output, apply V_{IHT} to each	–1080			mV
			$T_A = +25°C$	G_n input, one at a time, V_{IHMAX}	–980			mV
			$T_A = +85°C$	applied to all other G_n inputs.	–910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For GG output, apply V_{ILT}			–1655	mV
			$T_A = +25°C$	to G_3 input with V_{IHMAX}			–1630	mV
			$T_A = +85°C$	applied to all other inputs.			–1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For GG output, apply V_{ILMIN}	–1890		–1675	mV
			$T_A = +25°C$	to all G_n inputs with V_{IHMAX}	–1850		–1650	mV
			$T_A = +85°C$	applied to all other inputs.	–1825		–1615	mV
I_{IH}	High level input current	G_0, G_1, C_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			430	µA
			$T_A = +25°C$				270	µA
			$T_A = +85°C$				270	µA
		G_2, G_3 inputs	$T_A = -30°C$				360	µA
			$T_A = +25°C$				225	µA
			$T_A = +85°C$				225	µA
		P_0 input	$T_A = -30°C$	Apply V_{IHMAX} to P_0 input with V_{ILMIN} applied to all other inputs.			565	µA
			$T_A = +25°C$				355	µA
			$T_A = +85°C$				355	µA
		P_1, P_3 inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			700	µA
			$T_A = +25°C$				440	µA
			$T_A = +85°C$				440	µA
		P_2 input	$T_A = -30°C$	Apply V_{IHMAX} to P_3 input with V_{ILMIN} applied to all other inputs.			630	µA
			$T_A = +25°C$				395	µA
			$T_A = +85°C$				395	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under test, one at a time, with V_{IHMAX} applied to all other inputs.	0.5			µA
			$T_A = +25°C$		0.5			µA
			$T_A = +85°C$		0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				79	mA
			$T_A = +25°C$			58	72	mA
			$T_A = +85°C$				79	mA

Look–Ahead Carry Block 10179

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	T_A = +25°C		0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.148		V/V

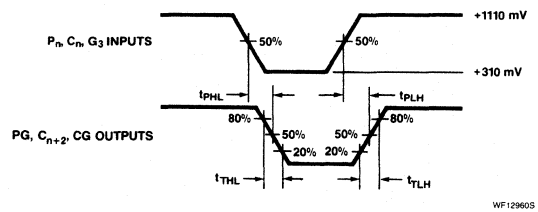
NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = –30°C MIN.	LIMITS T_A = –30°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C TYP.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH}	Propagation delay P_n to PG	Waveform 1	1.00	3.70	1.00	2.30	3.50	1.00	3.90	ns
t_{PHL}			1.00	3.70	1.00	1.80	3.50	1.00	3.90	ns
t_{PLH}	Propagation delay C_n to C_{n+2}		1.00	5.80	1.00	3.00	4.50	1.00	6.10	ns
t_{PHL}			1.00	5.80	1.00	3.00	4.50	1.00	6.10	ns
t_{PLH}	Propagation delay G_n to GG		1.00	5.80	1.00	3.20	5.50	1.00	6.10	ns
t_{PHL}			1.00	5.80	1.00	3.20	5.50	1.00	6.10	ns
t_{TLH}	Transition time 20% to 80%, 80% to 20%		1.30	3.50	1.30	2.50	3.50	1.30	3.50	ns
t_{THL}			1.30	3.50	1.30	2.50	3.50	1.30	3.50	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0682
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10180
Adder/Subtractor

Dual 2-Bit Adder/Subtractor

FEATURES

- **Typical propagation delay: A_n, B_n to C_{OUT} 4.5ns**
- **Typical supply current ($-I_{EE}$): 70mA**

DESCRIPTION

The 10180 is a high-speed, low power, general purpose adder/subtractor. Inputs for each adder are: Carry-in (C_{0IN}, C_{1IN}), Operand A (A_0, A_1), Operand B (B_0, B_1). Outputs are Sum (F_0, F_1), $\overline{\text{Sum}}$ ($\overline{F_0}$, $\overline{F_1}$) and Carry-out (C_{0OUT}, C_{1OUT}). Common select inputs act as controlled lines to invert A or B for subtraction. A very high-speed operation is possible with Operand in the Sum or Carryout propagation delay of 4.5ns, and Carry-in to Carry-out propagation delay of 2.2ns. The 10180 is designed to be used in special purpose adder/subtractor or in high-speed multiplier arrays.

All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

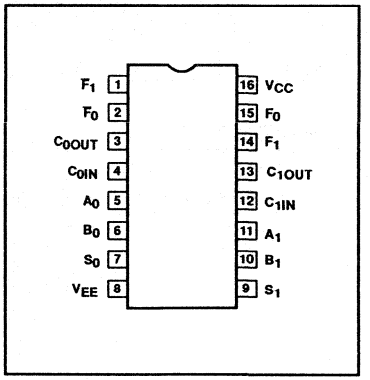
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic DIP	10180N
16-Pin Ceramic DIP	10180F

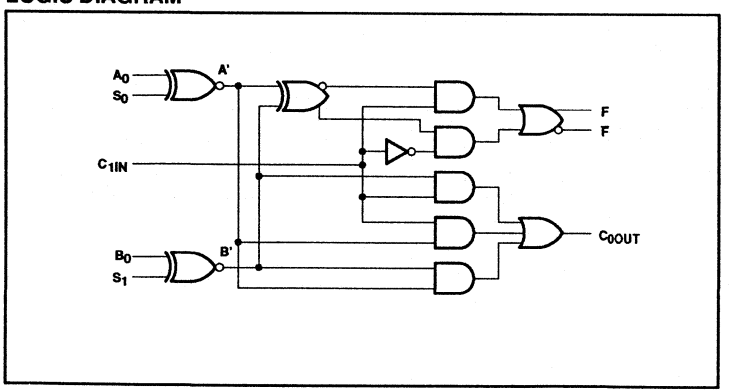
PIN DESCRIPTION

PINS	DESCRIPTION
A_0, A_1	A Operand Inputs
B_0, B_1	B Operand Inputs
S_0, S_1	Select Inputs
C_{0IN}, C_{1IN}	Carry-in Inputs
C_{0OUT}, C_{1OUT}	Carry-out Outputs
F_0, $\overline{F_0}$, F_1, $\overline{F_1}$	Sum Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Adder/Subtractor 10180

FUNCTION SELECT TABLE

INPUTS		OUTPUTS
S_0	S_1	FUNCTIONS F
H	H	$A + B + C_{IN}$
H	L	$C_{IN} + A - B$
L	H	$C_{IN} + B - A$
L	L	$C_{IN} - A - B$

H = High Voltage Level
L = Low Voltage Level
$A' = \overline{A \oplus S_0} = A \odot S_0$
$B' = \overline{B \oplus S_1} = B \odot S_1$
Both positive and negative logic:
$F = \overline{C}_{IN} (\overline{A}\,'B\,' + A\,'\overline{B}\,') + C_{IN} (A\,'B' + \overline{A}\,'\overline{B}\,')$
$C_{OUT} = C_{IN}A\,' + C_{IN}\,B\,' + A\,'B'$

FUNCTION TABLE

FUNCTION	INPUTS					OUTPUTS		
	S_0	S_1	A	B	C_{IN}	F	F	C_{OUT}
ADD $(A + B + C_1)$	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT $(C_1 + A - B)$	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	L
	H	L	H	L	L	L	H	H
	H	L	H	L	H	H	L	H
	H	L	H	H	L	H	L	L
	H	L	H	H	H	L	H	H
Reverse SUBTRACT $(C_1 + B - A)$	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	L	H	H
	L	H	L	H	H	H	L	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	L
	L	H	H	H	L	H	L	L
	L	H	H	H	H	L	H	H
$(C_1 - A - B)$	L	L	L	L	L	L	H	H
	L	L	L	L	H	H	L	H
	L	L	L	H	L	H	L	L
	L	L	L	H	H	L	H	H
	L	L	H	L	L	H	L	L
	L	L	H	L	H	L	H	H
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ground, V_{EE} = –5.2V ± 0.010V, T_A = –30°C to +85°C output loading with 50Ω to –2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		T_A = –30°C	Using V_{IHMAX} and V_{ILMIN}, apply a functional	–1060		–890	mV
			T_A = +25°C	pattern as indicated in the FUNCTION TABLE	–960		–810	mV
			T_A = +85°C	and measure V_{OH} on the respective outputs.	–890		–700	mV
V_{OHT}	High level output threshold voltage		T_A = –30°C	Apply V_{IHT} or V_{ILT} to one input at a time while	–1080			mV
			T_A = +25°C	applying V_{IHMAX} or V_{ILMIN} to all other inputs in accordance with the FUNCTION TABLE and	–980			mV
			T_A = +85°C	measure V_{OHT} on the respective outputs.	–910			mV
V_{OLT}	Low level output threshold voltage		T_A = –30°C	Apply V_{ILT} or V_{IHT} to one input at a time while			–1655	mV
			T_A = +25°C	applying V_{IHMAX} or V_{ILMIN} to all other inputs in accordance with the FUNCTION TABLE and			–1630	mV
			T_A = +85°C	measure V_{OLT} on the respective outputs.			–1595	mV
V_{OL}	Low level output voltage		T_A = –30°C	Using V_{IHMAX} and V_{ILMIN}, apply a functional	–1890		–1675	mV
			T_A = +25°C	pattern as indicated in the FUNCTION TABLE	–1850		–1650	mV
			T_A = +85°C	and measure V_{OL} on the respective outputs.	–1825		–1615	mV
I_{IH}	High level input current	C_{0IN}, C_{1IN} outputs	T_A = –30°C				590	µA
			T_A = +25°C				370	µA
			T_A = +85°C				370	µA
		A_0, A_1, B_0, B_1 inputs	T_A = –30°C	Apply V_{IHMAX} to each input under			350	µA
			T_A = +25°C	test, one at a time, with V_{ILMIN}			220	µA
			T_A = +85°C	applied to all other inputs.			220	µA
		S_0, S_1 inputs	T_A = –30°C				460	µA
			T_A = +25°C				290	µA
			T_A = +85°C				290	µA
I_{IL}	Low level input current		T_A = –30°C	Apply V_{ILMIN} to each input under	0.5			µA
			T_A = +25°C	test, one at a time, with V_{IHMAX}	0.5			µA
			T_A = +85°C	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		T_A = –30°C				95	mA
			T_A = +25°C			70	86	mA
			T_A = +85°C				95	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		T_A = +25°C			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

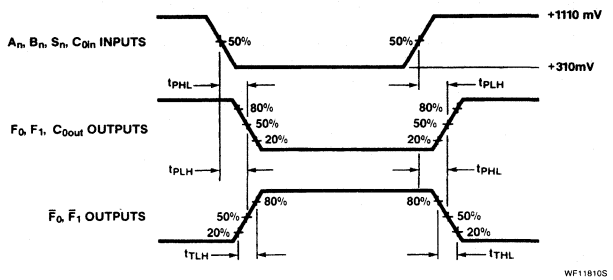
Adder/Subtractor 10180

AC ELECTRICAL CHARACTERISTICS V_{CC} = ground, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			T_A = –30°C		T_A = +25°C			T_A = +85°C		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_0, A_1, B_0, B_1 to F_0, F_1	Waveform 1	1.30 1.30	5.80 5.80	1.30 1.30	4.50 4.50	5.40 5.40	1.10 1.10	5.80 5.80	ns ns
t_{PLH} t_{PHL}	Propagation delay C_{0IN} to C_{0OUT}		1.00 1.00	3.40 3.40	1.00 1.00	2.20 2.20	3.30 3.30	0.90 0.90	3.60 3.60	ns ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to $\overline{F}_0$, $\overline{F}_1$		1.30 1.30	5.80 5.80	1.30 1.30	4.50 4.50	5.40 5.40	1.10 1.10	5.80 5.80	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.00 1.00	3.80 3.80	1.10 1.10	2.40 2.40	3.70 3.70	1.10 1.10	3.90 3.90	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Operands, Selects, and Carry–in Inputs to Carry–out and Sum Outputs

Document No.	853–0683
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10181
Arithmetic Unit

4-Bit Arithmetic Logic Unit/Function Generator

FEATURES

- **Typical propagation delay: 4.2ns**
- **Typical supply current ($-I_{EE}$): 130mA**

DESCRIPTION

The 10181 is a high-speed, Arithmetic Logic Unit. If performs 16 logic operations and 16 arithmetic operations on two 4-bit words. Arithmetic or logic mode of operation is selected by the mode control (M). Arithmetic logic operations are selected by a 4-bit select input (S_0 - S_3) in accordance with the function table. The device provides a group Carry Propagate (PG) and a Carry Generate (GG) for high-speed operations on very long words, using a 10179 as a high order look-ahead carry block. The internal carry is enabled while the mode control input (M) is Low (arithmetic operation).

All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

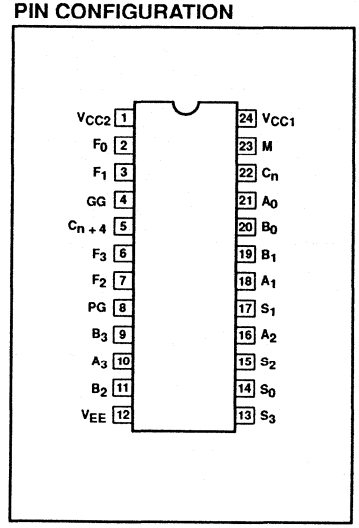
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic DIP	10181N
24-Pin Ceramic DIP	10181F

PIN DESCRIPTION

PINS	DESCRIPTION
M	Mode Control Input
$A_0 - A_3$, $B_0 - B_3$	Operand Inputs
$S_0 - S_3$	Function Select Inputs
C_n	Carry Inputs
$F_0 - F_3$	Data Outputs
C_{n+4}	Carry Output
GG	Carry Generate Output
PG	Carry Propagate Output

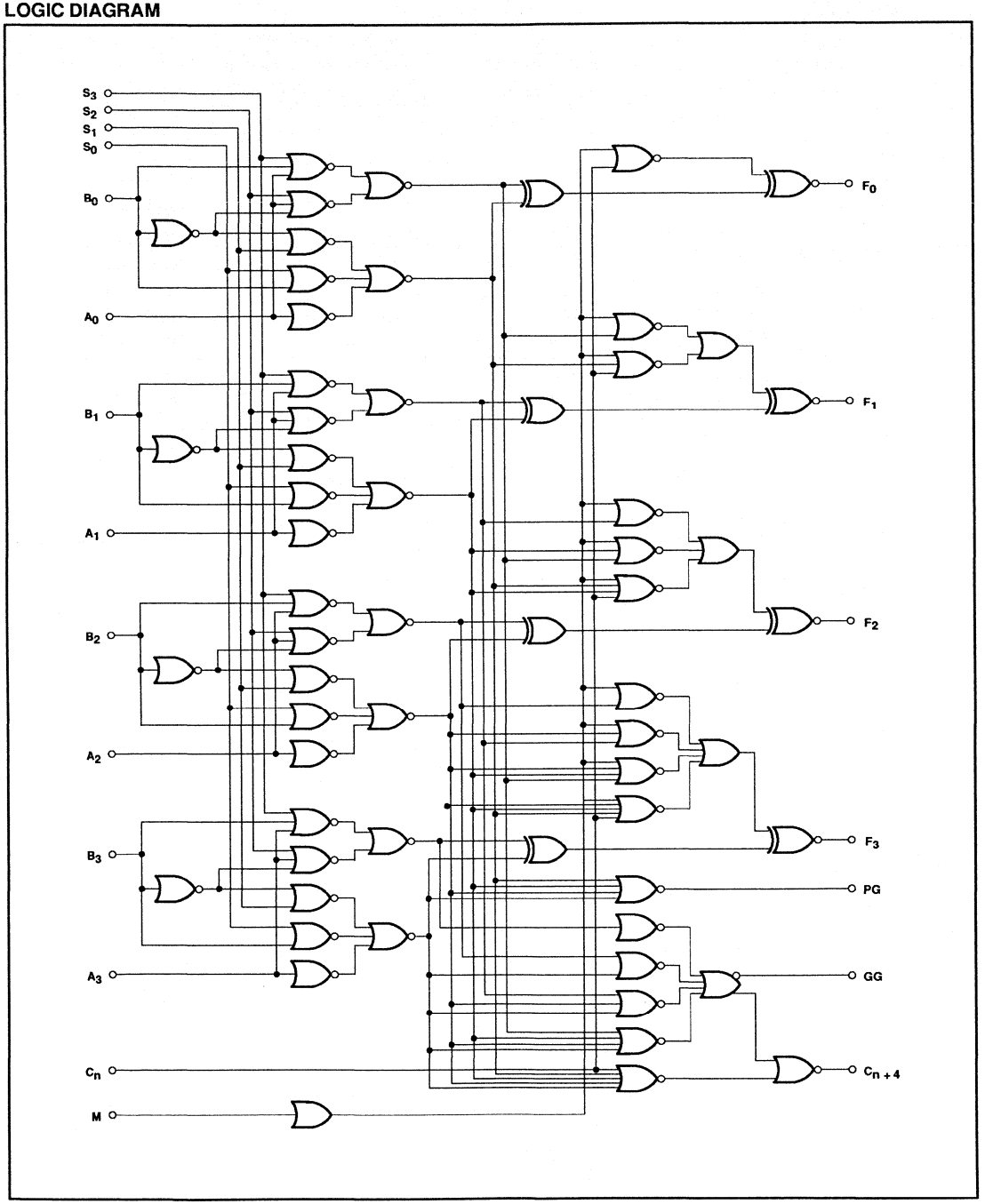
PIN CONFIGURATION



Arithmetic Unit

10181

LOGIC DIAGRAM



FUNCTION TABLE

FUNCTION SELECT INPUTS				OUTPUT FUNCTION F		
				M = HIGH (Logic Mode)	M = LOW (Arithmetic Mode)	
S_3	S_2	S_1	S_0	C_n = H or L	C_n = LOW	C_n = HIGH
L	L	L	L	$\overline{A}$	A	A plus 1
L	L	L	H	$\overline{A} + \overline{B}$	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
L	L	H	L	$\overline{A} + B$	A plus AB	A plus AB plus 1
L	L	H	H	HIGH	A plus A (2 times A)	A plus A plus 1
L	H	L	L	$\overline{A}\,\overline{B}$	A + B	(A + B) plus 1
L	H	L	H	$\overline{B}$	(A + B) plus $A\overline{B}$	(A + B) plus $A\overline{B}$ plus 1
L	H	H	L	$\overline{A \oplus B}$	A plus B	A plus B plus 1
L	H	H	H	$A + \overline{B}$	(A + B) plus A	(A + B) plus A plus 1
H	L	L	L	$\overline{A}B$	$A + \overline{B}$	$(A + \overline{B})$ plus 1
H	L	L	H	$A \oplus B$	A minus B minus 1	A minus B
H	L	H	L	B	$(A + \overline{B})$ plus AB	$(A + \overline{B})$ plus AB plus 1
H	L	H	H	A + B	$(A + \overline{B})$ plus A	$(A + \overline{B})$ plus A plus 1
H	H	L	L	LOW	– 1 (2's complement)	Zero
H	H	L	H	$A\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
H	H	H	L	AB	AB minus 1	AB
H	H	H	H	A	A minus 1	A

H = High Voltage Level
L = Low Voltage Level

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	All input/output combinations in accordance with the Functional Table. Input conditions: V_{ILMIN}, V_{IHMAX} (for V_{OH} and V_{OL}) or V_{ILT}, V_{IHT} (for V_{OHT} and V_{OLT}). Only one input at a time should be at V_{IHT} or V_{ILT}. Al other inputs should be at V_{IHMAX} or V_{ILMIN} curing test.	–1060		–890	mV
			$T_A = +25°C$		–960		–810	mV
			$T_A = +85°C$		–890		–700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$		–1080			mV
			$T_A = +25°C$		–980			mV
			$T_A = +85°C$		–910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$				–1655	mV
			$T_A = +25°C$				–1630	mV
			$T_A = +85°C$				–1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$		–1890		–1675	mV
			$T_A = +25°C$		–1850		–1650	mV
			$T_A = +85°C$		–1825		–1615	mV
I_{IH}	High level input current	A_n inputs	$T_A = -30°C$				350	µA
			$T_A = +25°C$				220	µA
			$T_A = +85°C$				220	µA
		B_n inputs	$T_A = -30°C$				390	µA
			$T_A = +25°C$				245	µA
			$T_A = +85°C$				245	µA
		S_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			425	µA
			$T_A = +25°C$				265	µA
			$T_A = +85°C$				265	µA
		C_n input	$T_A = -30°C$	Apply V_{IHMAX} to C_n input with V_{ILMIN} applied to all other inputs.			460	µA
			$T_A = +25°C$				290	µA
			$T_A = +85°C$				290	µA
		M input	$T_A = -30°C$	Apply V_{IHMAX} to M input with V_{ILMIN} applied to all other inputs.			320	µA
			$T_A = +25°C$				200	µA
			$T_A = +85°C$				200	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under test, one at a time, with V_{IHMAX} applied to all other inputs.	0.5			µA
			$T_A = +25°C$		0.5			µA
			$T_A = +85°C$		0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$	Apply V_{IHMAX} to all inputs.			150	mA
			$T_A = +25°C$			130	145	mA
			$T_A = +85°C$				150	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	T_A = +25°C		0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation			0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.148		V/V

NOTES:

4. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
5. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
6. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, V_{EE} = −5.2V ± 0.010V

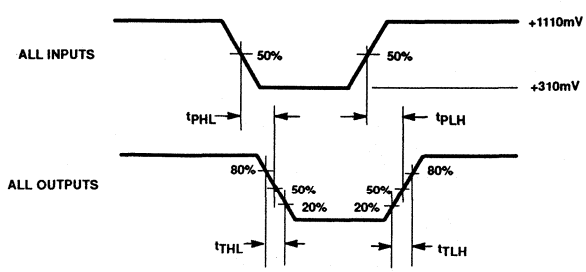
SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS T_A = −30°C MIN.	LIMITS T_A = −30°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C TYP.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Waveform 1 A_0, A_1, A_2, A_3	1.00 1.00	5.10 5.10	1.10 1.10	3.10 3.10	5.00 5.00	1.10 1.10	5.40 5.40	ns ns
t_{TLH} t_{THL}	Transition time[2] C_n to C_{n+4}	Waveform 1 A_0, A_1, A_2, A_3	1.00 1.00	3.20 3.20	1.00 1.00	2.00 2.00	3.00 3.00	1.00 1.00	3.20 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to F_1	Waveform 1 A_0	1.70 1.70	7.20 7.20	2.00 2.00	4.50 4.50	7.00 7.00	2.00 2.00	7.50 7.50	ns ns
t_{TLH} t_{THL}	Transition time[2] C_n to F_1	Waveform 1 A_0	1.30 1.30	5.30 5.30	1.50 1.50	3.00 3.00	5.00 5.00	1.50 1.50	5.30 5.30	ns ns
t_{PLH} t_{PHL}	Propagation delay A_1 to F_1	Waveform 1	2.60 2.60	10.40 10.40	3.00 3.00	6.50 6.50	10.00 10.00	3.00 3.00	10.80 10.80	ns ns
t_{TLH} t_{THL}	Transition time[2] A_1 to F_1	Waveform 1	1.30 1.30	5.40 5.40	1.50 1.50	3.00 3.00	5.00 5.00	1.50 1.50	5.30 5.30	ns ns
t_{PLH} t_{PHL}	Propagation delay A_1 to PG	Waveform 1 S_0, S_3	1.60 1.60	7.00 7.00	2.00 2.00	5.00 5.00	6.50 6.50	2.00 2.00	7.00 7.00	ns ns
t_{TLH} t_{THL}	Transition time[2] A_1 to PG	Waveform 1 S_0, S_3	0.80 0.80	3.70 3.70	1.10 1.10	2.00 2.00	3.50 3.50	1.10 1.10	3.80 3.80	ns ns
t_{PLH} t_{PHL}	Propagation delay A_1 to GG	Waveform 1 A_0, A_2, A_3, C_n	1.10 1.10	7.40 7.40	2.00 2.00	4.50 4.50	7.00 7.00	1.30 1.30	7.70 7.70	ns ns
t_{TLH} t_{THL}	Transition time[2] A_1 to GG	Waveform 1 A_0, A_2, A_3, C_n	1.20 1.20	5.10 5.10	1.50 1.50	4.00 4.00	5.00 5.00	1.20 1.20	5.30 5.30	ns ns
t_{PLH} t_{PHL}	Propagation delay A_1 to C_{n+4}	Waveform 1 A_0, A_2, A_3, C_n	1.70 1.70	7.30 7.30	2.00 2.00	5.00 5.00	7.00 7.00	2.00 2.00	7.80 7.80	ns ns
t_{TLH} t_{THL}	Transition time[2] A_1 to C_{n+4}	Waveform 1 A_0, A_2, A_3, C_n	1.00 1.00	3.10 3.10	1.00 1.00	2.00 2.00	3.00 3.00	1.00 1.00	3.20 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay B_1 to F_1	Waveform 1 S_3, C_n	2.70 2.70	11.30 11.30	3.00 3.00	8.00 8.00	11.00 11.00	3.00 3.00	11.90 11.90	ns ns
t_{TLH} t_{THL}	Transition time[2] B_1 to F_1	Waveform 1 S_3, C_n	1.20 1.20	5.30 5.30	1.50 1.50	3.50 3.50	5.00 5.00	1.50 1.50	5.30 5.30	ns ns
t_{PLH} t_{PHL}	Propagation delay B_1 to PG	Waveform 1 S_0, S_3	1.60 1.60	7.70 7.70	2.00 2.00	6.00 6.00	7.50 7.50	2.00 2.00	8.00 8.00	ns ns
t_{TLH} t_{THL}	Transition time[2] B_1 to PG	Waveform 1 S_0, S_3	1.00 1.00	3.60 3.60	1.00 1.00	2.00 2.00	3.50 3.50	1.10 1.10	3.90 3.90	ns ns

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS							UNIT
			T_A = –30°C		T_A = +25°C			T_A = +85°C		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay B_1 to GG	Waveform 1 S_3, C_n	1.70 1.70	8.20 8.20	2.00 2.00	6.00 6.00	8.00 8.00	2.00 2.00	8.60 8.60	ns ns
t_{TLH} t_{THL}	Transition time[2] B_1 to GG	Waveform 1 S_3, C_n	1.40 1.40	5.20 5.20	1.50 1.50	3.00 3.00	5.00 5.00	1.20 1.20	5.40 5.40	ns ns
t_{PLH} t_{PHL}	Propagation delay B_1 to C_{n+4}	Waveform 1 S_3, C_n	1.80 1.80	8.20 8.20	2.00 2.00	6.00 6.00	8.00 8.00	2.00 2.00	8.70 8.70	ns ns
t_{TLH} t_{THL}	Transition time[2] B_1 to C_{n+4}	Waveform 1 S_3, C_n	0.90 0.90	3.10 3.10	1.00 1.00	2.00 2.00	3.00 3.00	1.00 1.00	3.20 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay M to F_1	Waveform 1	2.40 2.40	10.30 10.30	3.00 3.00	6.50 6.50	10.00 10.00	3.00 3.00	10.80 10.80	ns ns
t_{TLH} t_{THL}	Transition time[2] M to F_1	Waveform 1	1.10 1.10	5.10 5.10	1.50 1.50	4.00 4.00	5.00 5.00	1.50 1.50	5.30 5.30	ns ns
t_{PLH} t_{PHL}	Propagation delay S_1 to F_1	Waveform 1 A_1, B_1	2.50 2.50	10.70 10.70	3.00 3.00	6.50 6.50	10.00 10.00	3.00 3.00	10.80 10.80	ns ns
t_{TLH} t_{THL}	Transition time[2] S_1 to F_1	Waveform 1 A_3, B_3	1.00 1.00	5.40 5.40	1.50 1.50	3.00 3.00	5.00 5.00	1.50 1.50	5.40 5.40	ns ns
t_{PLH} t_{PHL}	Propagation delay S_1 to PG	Waveform 1 A_3, B_3	1.70 1.70	8.30 8.30	2.00 2.00	6.00 6.00	8.00 8.00	2.00 2.00	8.40 8.40	ns ns
t_{TLH} t_{THL}	Transition time[2] S_1 to PG	Waveform 1 A_3, B_3	0.80 0.80	5.10 5.10	1.10 1.10	3.00 3.00	5.00 5.00	1.10 1.10	5.20 5.20	ns ns
t_{PLH} t_{PHL}	Propagation delay S_1 to C_{n+4}	Waveform 1 A_3, B_3	1.60 1.60	9.30 9.30	2.00 2.00	6.00 6.00	9.00 9.00	2.00 2.00	9.90 9.90	ns ns
t_{TLH} t_{THL}	Transition time[2] S_1 to C_{n+4}	Waveform 1 A_3, B_3	0.90 0.90	5.30 5.30	1.10 1.10	3.00 3.00	5.00 5.00	1.00 1.00	5.20 5.20	ns ns
t_{PLH} t_{PHL}	Propagation delay S_1 to GG	Waveform 1 A_3, B_3	1.50 1.50	9.60 9.60	2.00 2.00	6.00 6.00	9.00 9.00	1.90 1.90	9.70 9.70	ns ns
t_{TLH} t_{THL}	Transition time[2] S_1 to GG	Waveform 1 A_3, B_3	0.80 0.80	6.20 6.20	0.80 0.80	3.00 3.00	6.00 6.00	0.80 0.80	6.50 6.50	ns ns

NOTES:
1. Apply 1110mV to pins listed with 310mV applied to all other inputs.
2. All transition times are from 20% to 80% and 80% to 20% (refer to Waveform 1).
3. For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

Document No.	853–0684
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10188
Hex Buffer

Hex Buffer with Enable (Non-Inverting)

FEATURES

- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 33mA**

DESCRIPTION

The 10188 includes six buffers offering individual inputs and outputs and a common Enable input, driving all outputs Low. Each input is connected to V_{EE} via a pull-down resistor resulting in high input impedance and eliminating the need for connecting unused inputs Low.

Due to open emitter outputs the 10188 features OR capability with high fan-out for driving 50Ω lines.

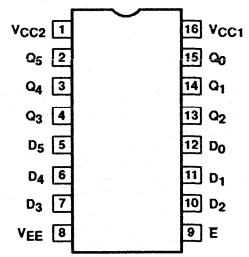
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10188N
16–Pin Ceramic DIP	10188F
16–Pin SO	10188D

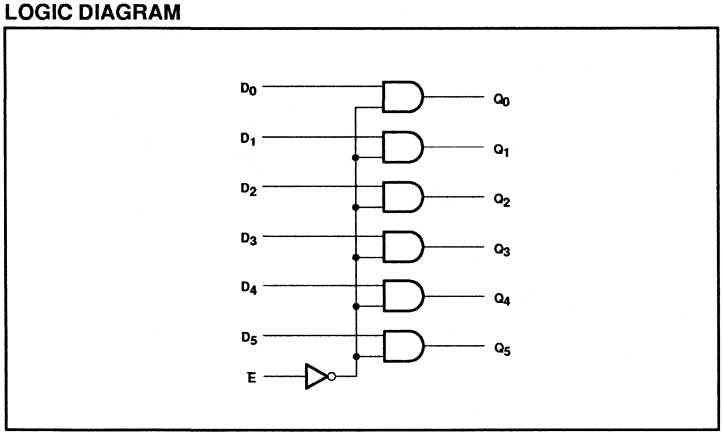
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
$\overline{E}$	Common Enable Input
$Q_0 - Q_5$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Hex Buffer | 10188

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{E}$	D_n	Q_n
L	L	L
L	H	H
H	X	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{ILMIN} to $\overline{E}$ input	−1060		−890	mV
			$T_A = +25°C$	with V_{IHMAX} applied to	−960		−810	mV
			$T_A = +85°C$	all other inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	Apply V_{ILT} to $\overline{E}$ input	−1080			mV
			$T_A = +25°C$	with V_{IHMAX} applied to	−980			mV
			$T_A = +85°C$	all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	Apply V_{IHT} to $\overline{E}$ input			−1655	mV
			$T_A = +25°C$	with V_{IHMAX} applied to			−1630	mV
			$T_A = +85°C$	all other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$		−1890		−1675	mV
			$T_A = +25°C$	Apply V_{ILMIN} to all inputs.	−1850		−1650	mV
			$T_A = +85°C$		−1825		−1615	mV
I_{IH}	High level input current	Other inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under			425	µA
			$T_A = +25°C$	test, one at a time, with V_{ILMIN}			265	µA
			$T_A = +85°C$	applied to all other inputs.			265	µA
		$\overline{E}$ input	$T_A = -30°C$	Apply V_{IHMAX} to $\overline{E}$ input			460	µA
			$T_A = +25°C$	with V_{ILMIN} applied to			290	µA
			$T_A = +85°C$	all other inputs.			290	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				46	mA
			$T_A = +25°C$			33	42	mA
			$T_A = +85°C$				46	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

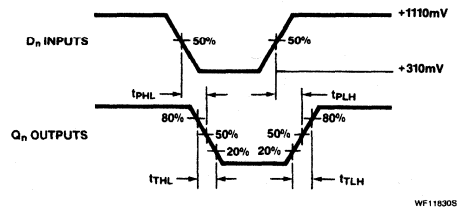
Hex Buffer 10188

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

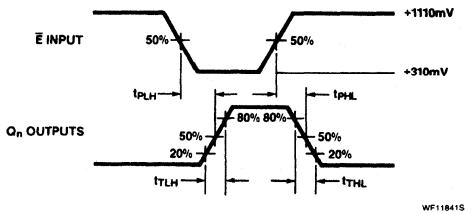
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			Min	Max	Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	3.30 3.30	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n		1.10 1.10	3.90 3.90	1.10 1.10	2.50 2.50	3.50 3.50	1.10 1.10	3.90 3.90	ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.10 1.10	3.70 3.70	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Data to Output



Waveform 2. Propagation Delay and Transition Times for Enable to Output

Document No.	853–0685
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10189
Inverter

Hex Inverter with Enable

FEATURES

- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 30mA**

DESCRIPTION

The 10189 includes six inverters offering individual inputs and outputs and a common enable input, driving all outputs Low. Each input is connected to V_{EE} via a pull-down resistor resulting in high input impedance and eliminating the need for tying unused inputs Low.

Due to open emitter outputs, the 10189 features OR capability with high fan-out for driving 50Ω lines.

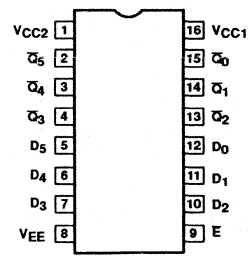
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10189N
16–Pin Ceramic DIP	10189F

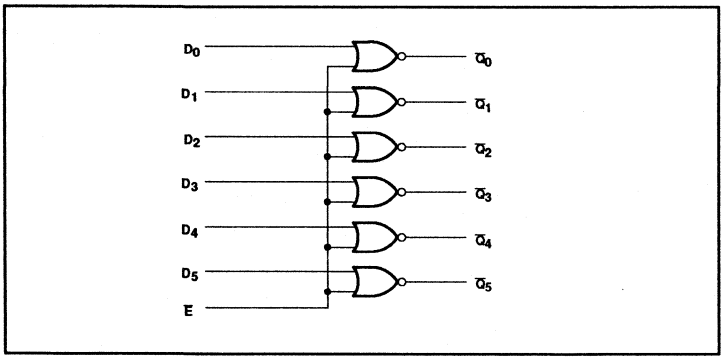
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
$\overline{E}$	Common Enable Input
$\overline{Q}_0 - \overline{Q}_5$	Data Outputs

PIN CONFIGURATION



LOGIC DIAGRAM



Inverter | 10189

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	Apply V_{ILMIN} to all inputs.	−1060		−890	mV
			$T_A = +25°C$		−960		−810	mV
			$T_A = +85°C$		−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	Apply V_{ILT} to each D_n input, one at a time, with V_{ILMIN} applied to $\overline{E}$ input and V_{IHMAX} applied to all other inputs.	−1080			mV
			$T_A = +25°C$		−980			mV
			$T_A = +85°C$		−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	Apply V_{IHT} to each D_n input, one at a time, with V_{ILMIN} applied to $\overline{E}$ input and V_{ILMIN} applied to all other inputs.			−1655	mV
			$T_A = +25°C$				−1630	mV
			$T_A = +85°C$				−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	Apply V_{IHMAX} to all D_n inputs with V_{ILMIN} applied to $\overline{E}$ input.	−1890		−1675	mV
			$T_A = +25°C$		−1850		−1650	mV
			$T_A = +85°C$		−1825		−1615	mV
I_{IH}	High level input current	Other inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			425	µA
			$T_A = +25°C$				265	µA
			$T_A = +85°C$				265	µA
		$\overline{E}$ input	$T_A = -30°C$	Apply V_{IHMAX} to $\overline{E}$ input with V_{ILMIN} applied to all other inputs.			890	µA
			$T_A = +25°C$				555	µA
			$T_A = +85°C$				555	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under test, one at a time, with V_{IHMAX} applied to all other inputs.	0.5			µA
			$T_A = +25°C$		0.5			µA
			$T_A = +85°C$		0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				44	mA
			$T_A = +25°C$			30	40	mA
			$T_A = +85°C$				44	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

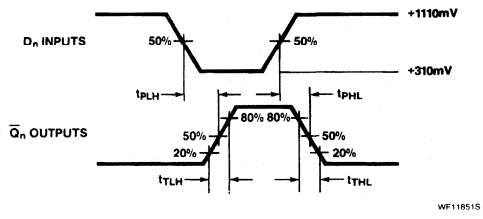
Inverter 10189

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

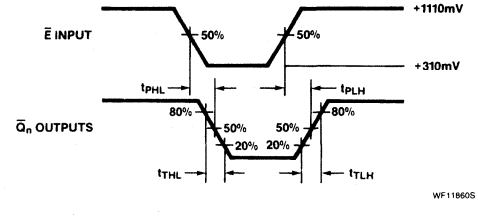
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 1	1.00 1.00	3.30 3.30	1.00 1.00	2.00 2.00	2.90 2.90	1.00 1.00	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Q}_n$	Waveform 2	1.10 1.10	3.90 3.90	1.10 1.10	2.50 2.50	3.50 3.50	1.10 1.10	3.90 3.90	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1, 2	1.10 1.10	3.60 3.60	1.10 1.10	2.00 2.00	3.30 3.30	1.10 1.10	3.70 3.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Data to Output



Waveform 2. Propagation Delay and Transition Times for Enable to Output

Document No.	853–0686
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10192
Bus Driver

Quad Open Collector Bus Driver

FEATURES

- **Typical propagation delay: 3.0ns**
- **Typical supply current ($-I_{EE}$): 110mA**

DESCRIPTION

The 10192 contains four line drivers with complementary outputs. Each driver has a Data (D_n) input and shares an Enable ($\overline{E}_n$) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K ECL input signals and provides a nominal signal of 800mV across a 50Ω load at each output collector. Outputs can drive higher values of load resistance, provided that the combination of IR drop and load return voltage V_{LR} does not cause an output collector to go more negative than –2.4V with respect to V_{CC}. To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5V with respect to V_{CC}. When the $\overline{E}_n$ input is High, both output transistors of a driver are nonconducting. When not used, the $\overline{E}_n$ inputs, as well as the D_n inputs, may be left open. Outputs must be loaded during input leakage tests.

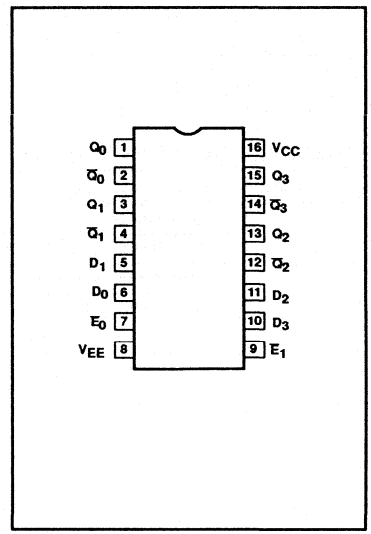
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10192N
16–Pin Ceramic DIP	10192F

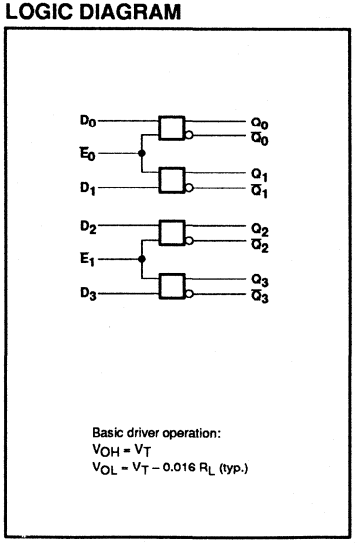
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
$\overline{E}_0$, $\overline{E}_1$	Enable Inputs
$Q_0 - Q_3$, $\overline{Q}_0 - \overline{Q}_3$	Data Outputs

PIN CONFIGURATION

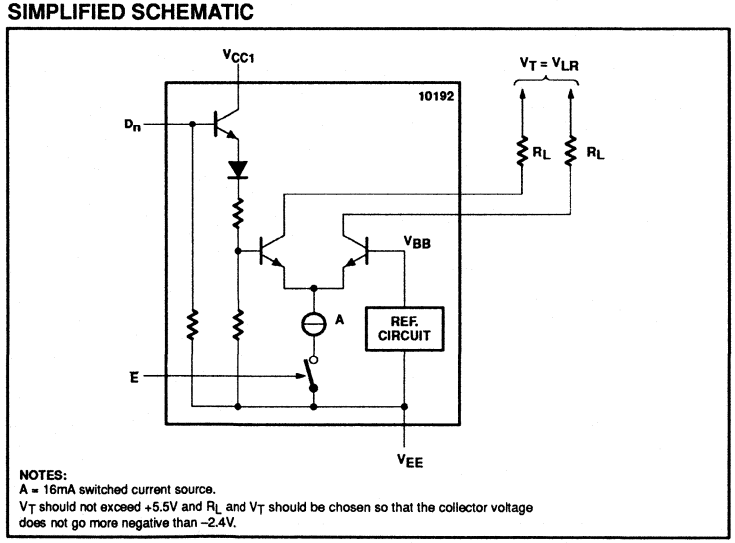


LOGIC DIAGRAM



Basic driver operation:
$V_{OH} = V_T$
$V_{OL} = V_T - 0.016\ R_L$ (typ.)

SIMPLIFIED SCHEMATIC



NOTES:
A = 16mA switched current source.
V_T should not exceed +5.5V and R_L and V_T should be chosen so that the collector voltage does not go more negative than –2.4V.

Bus Driver | 10192

FUNCITON TABLE

INPUTS		OUTPUTS	
$\overline{E}$	D	$\overline{Q}$	Q
L	L	H	L
L	H	L	H
H	X	H	H

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
V_T	Load termination voltage		5.5	V
V_O	Output voltage (at collector)	Max	+5.5	V
		Min	–2.4	V
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ground, V_{EE} = –5.2V ± 0.010V, T_A = –30°C to +85°C output loading 50Ω to –2.0V ± 0.010V unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
I_{OH}	Output current High–State	T_A = –30°C	For $\overline{Q}$ outputs, apply V_{ILMIN} to all inputs. For			2.0	mA
		T_A = +25°C	Q outputs, apply V_{ILMIN} to $\overline{E}_n$ inputs with			2.0	mA
		T_A = +85°C	V_{IHMAX} applied to D_n inputs.			2.0	mA
I_{OHT}	Output threshold current High–State	T_A = –30°C	For Q outputs, apply V_{IHT} to each D_n input, one				mA
		T_A = +25°C	at a time, with V_{ILMIN} applied to all other inputs. For $\overline{Q}$ outputs, apply V_{ILT} to each D_n input, one			2.0	mA
		T_A = +85°C	at a time, with V_{ILMIN} applied to all other inputs.				mA
I_{OLT}	Output threshold current Low–State	T_A = –30°C	For Q outputs, apply V_{ILT} to each D_n input, one	13.5			mA
		T_A = +25°C	at a time, with V_{ILMIN} applied to all other inputs. For $\overline{Q}$ outputs, apply V_{IHT} to each D_n input, one	14			mA
		T_A = +85°C	at a time, with V_{ILMIN} applied to all other inputs.	14			mA
I_{OL}	Output current Low–State	T_A = –30°C	For $\overline{Q}$ outputs, apply V_{IHMAX} to D_n inputs	13.5		18	mA
		T_A = +25°C	with V_{ILMIN} applied to E_n inputs. For	14		18	mA
		T_A = +85°C	Q outputs, apply V_{ILMIN} to all inputs.	14		19	mA
I_{OZ}	Output leakage current High impedance	T_A = –30°C	Apply V_{IHMAX} to all inputs.			300	µA
		T_A = +25°C				300	µA
		T_A = +85°C				300	µA
I_{IH}	High level input current	T_A = –30°C	Apply V_{IHMAX} to each input under test,			425	µA
		T_A = +25°C	one at a time, with V_{ILMIN} applied to			265	µA
		T_A = +85°C	all other inputs. Outputs must be loaded.			265	µA
I_{IL}	Low level input current	T_A = –30°C	Apply V_{ILMIN} to each input under test,	0.5			µA
		T_A = +25°C	one at a time, with V_{IHMAX} applied to	0.5			µA
		T_A = +85°C	all other inputs. Outputs must be loaded.	0.3			µA
$-I_{EE}$	V_{EE} supply current	T_A = –30°C				154	mA
		T_A = +25°C			110	140	mA
		T_A = +85°C				154	mA

NOTES:

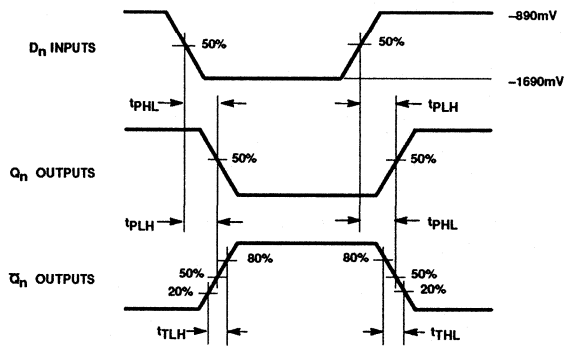
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS V_{CC} = ground, V_{EE} = –5.2V ± 0.010V

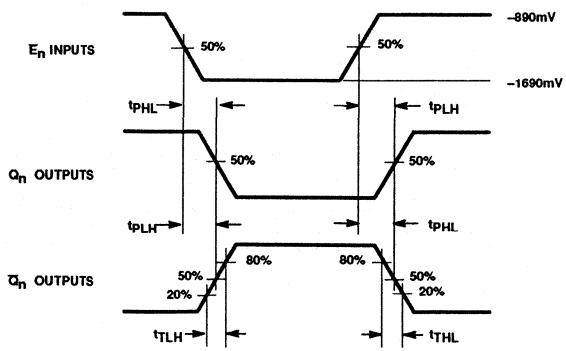
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			T_A = –30°C		T_A = +25°C			T_A = +85°C		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	2.00 2.00	4.47 4.47	2.00 2.00	3.00 3.00	4.50 4.50	2.00 2.00	4.80 4.80	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to Q_n, $\overline{Q}_n$	Waveform 2	2.50 2.50	6.30 6.30	2.50 2.50	3.50 3.50	6.00 6.00	2.50 2.50	6.60 6.60	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1, 2	1.30 1.30	3.50 3.50	1.30 1.30	2.30 2.30	3.30 3.30	1.30 1.30	3.50 3.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



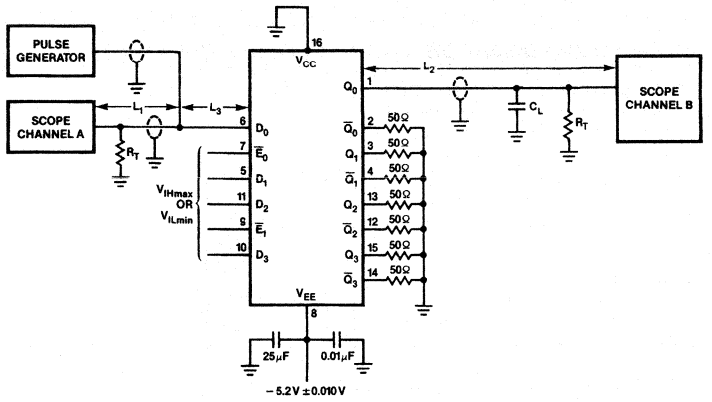
Waveform 1. Propagation Delay and Transition Times for Data to Outputs



Waveform 2. Propagation Delay and Transition Times for Enable to Outputs

Bus Driver 10192

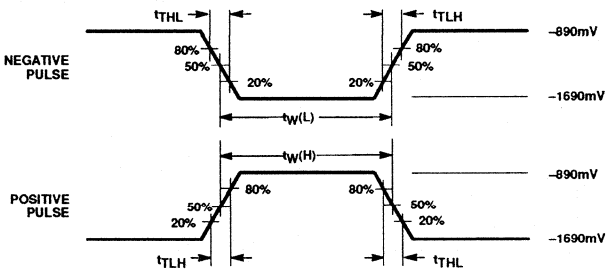
TEST CIRCUIT AND WAVEFORMS



NOTES:

1. $V_{CC1} = V_{CC2} = GND$ (0V), $V_{EE} = -5.2V \pm 0.010V$.
2. Decoupling 0.01μF and 25μF from GND to V_{EE} (0.01μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3 the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. R_T = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

TC05251S



INPUT PULSE REQUIREMENT V_{CC1} = GND ()V), V_{EE} = −5.2V ± 0.010V, V_T = GND (0V)					
Family	**Amplitude**	**Rep Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
10K ECL	800mV$_{P-P}$	1MHz	500ns	2.0 ± 0.2ns	2.0 ± 0.2ns

Philips Components

Document No.	853–0687
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10210
Line Driver

High-Speed Dual 3-Input/3-Output OR Line Driver

FEATURES

- **Typical propagation delay: 1.5ns**
- **Typical supply current ($-I_{EE}$): 31mA**

DESCRIPTION

The 10210 is a high-speed dual 3-input/3-output OR line driver intended to drive up to six transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications. The 10210 is a higher speed version of the 10110. It is a pin-for-pin replacement for the device. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

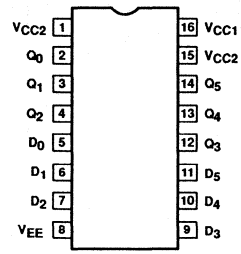
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10210N
16–Pin Ceramic DIP	10210F

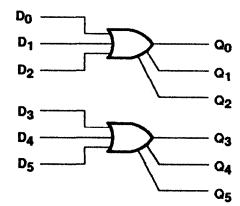
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
$Q_0 - Q_5$	Data Outputs (OR)

PIN CONFIGURATION

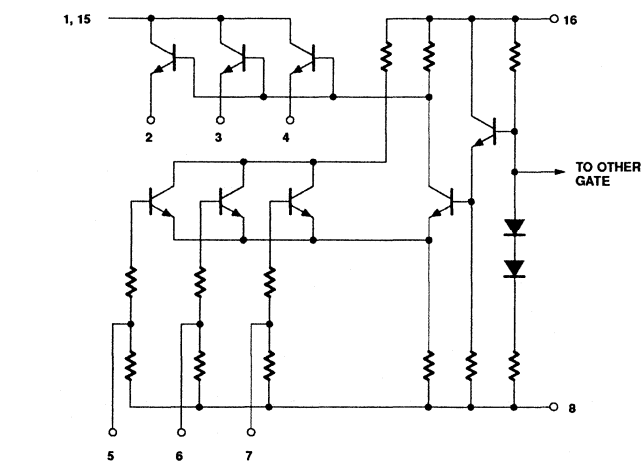


LOGIC DIAGRAM



$Q_0 = Q_1 = Q_2 = D_0 + D_1 + D_2$
$Q_3 = Q_4 = Q_5 = D_3 + D_4 + D_5$

SIMPLIFIED SCHEMATIC



Line Driver 10210

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to all inputs.	−1060		−890	mV
		$T_A = +25°C$		−960		−810	mV
		$T_A = +85°C$		−890		−700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{IHT} to each D_n input, one at a time, with V_{ILMIN} applied to all other inputs.	−1080			mV
		$T_A = +25°C$		−980			mV
		$T_A = +85°C$		−910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Apply V_{ILT} to each D_n input, one at a time, with V_{ILMIN} applied to all other inputs.			−1655	mV
		$T_A = +25°C$				−1630	mV
		$T_A = +85°C$				−1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	Apply V_{ILMIN} to all inputs.	−1890		−1675	mV
		$T_A = +25°C$		−1850		−1650	mV
		$T_A = +85°C$		−1825		−1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			650	µA
		$T_A = +25°C$				410	µA
		$T_A = +85°C$				410	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under test, one at a time, with V_{IHMAX} applied to all other inputs.	0.5			µA
		$T_A = +25°C$		0.5			µA
		$T_A = +85°C$		0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				42	mA
		$T_A = +25°C$			31	38	mA
		$T_A = +85°C$				42	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

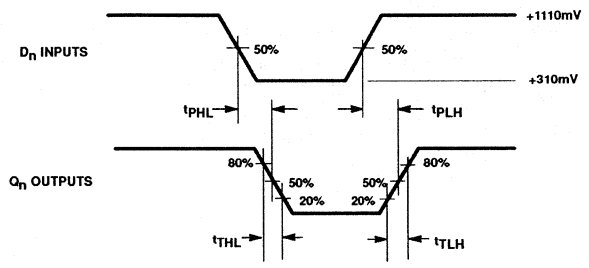
Line Driver 10210

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	2.60 2.60	1.00 1.00	1.50 1.50	2.50 2.50	1.00 1.00	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.00 1.00	2.60 2.60	1.00 1.00	1.50 1.50	2.50 2.50	1.00 1.00	2.80 2.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Data to Output

Document No.	853–0688
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10211
Line Driver

High-Speed Dual 3-Input/3-Output NOR Line Driver

FEATURES

- **Typical propagation delay: 1.5ns**
- **Typical supply current ($-I_{EE}$): 30mA**

DESCRIPTION

The 10211 is a high-speed dual 3-input/3-output NOR line driver intended to drive up to three transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications. The 10211 is a higher speed version of the 10111. It is a pin-for-pin replacement for this type. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

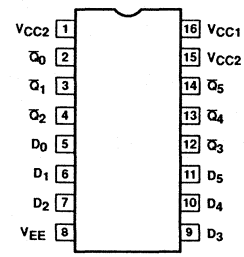
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10211N
16–Pin Ceramic DIP	10211F

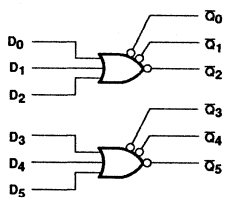
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
$Q_0 - Q_5$	Data Outputs

PIN CONFIGURATION

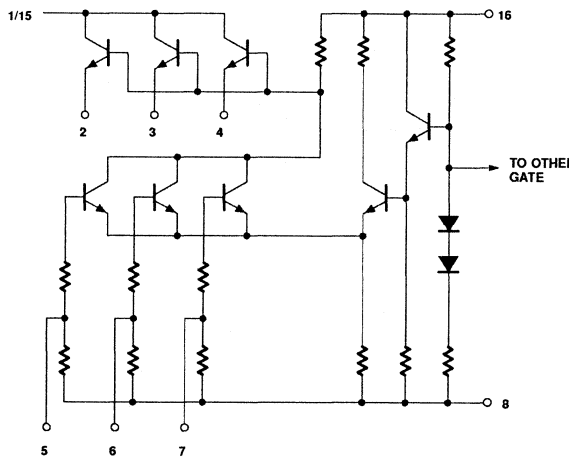


LOGIC DIAGRAM



$$Q_0 = Q_1 = Q_2 = \overline{D_0 + D_1 + D_2}$$
$$Q_3 = Q_4 = Q_5 = \overline{D_3 + D_4 + D_5}$$

SIMPLIFIED SCHEMATIC



Line Driver 10211

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	Apply V_{ILMIN} to all inputs.	−1060		−890	mV
		$T_A = +25°C$		−960		−810	mV
		$T_A = +85°C$		−890		−700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	Apply V_{ILT} to each input, one at a time, with V_{ILMIN} applied to all other inputs.	−1080			mV
		$T_A = +25°C$		−980			mV
		$T_A = +85°C$		−910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	Apply V_{IHT} to each input, one at a time, with V_{ILMIN} applied to all other inputs.			−1655	mV
		$T_A = +25°C$				−1630	mV
		$T_A = +85°C$				−1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	Apply V_{IHMAX} to all inputs.	−1890		−1675	mV
		$T_A = +25°C$		−1850		−1650	mV
		$T_A = +85°C$		−1825		−1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			650	µA
		$T_A = +25°C$				410	µA
		$T_A = +85°C$				410	µA
I_{IL}	Low level input current	$T_A = -30°C$	Apply V_{ILMIN} to each input under test, one at a time, with V_{IHMAX} applied to all other inputs.	0.5			µA
		$T_A = +25°C$		0.5			µA
		$T_A = +85°C$		0.3			µA
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$				42	mA
		$T_A = +25°C$			30	38	mA
		$T_A = +85°C$				42	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

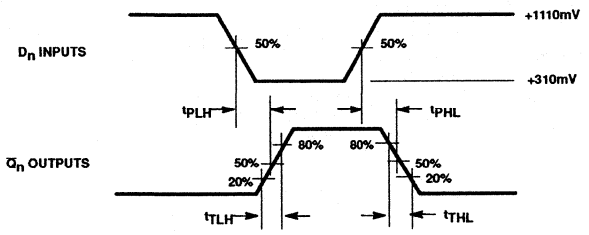
Line Driver | 10211

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 1	1.00 1.00	2.60 2.60	1.00 1.00	1.50 1.50	2.50 2.50	1.00 1.00	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		1.00 1.00	2.60 2.60	1.00 1.00	1.50 1.50	2.50 2.50	1.00 1.00	2.80 2.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Data to Output

Philips Components

Document No.	853–0689
ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10216
Line Receiver

Triple Differential OR/NOR Line Receiver (High-Speed)

FEATURES

- **Typical propagation delay: 1.5ns**
- **Typical supply current ($-I_{EE}$): 20mA**

DESCRIPTION

The 10216 is a high-speed triple differential amplifier for use in sensing differential signals over long lines. The Reference Bias Voltage (V_{BB}) is made available at Pin 11 to make the device useful as a Schmitt Trigger or in other applications where a stable reference voltage is necessary. If any amplifier in a package is not used the input of that amplifier must be tied V_{BB} (Pin 11) to prevent upsetting the current source bias network.

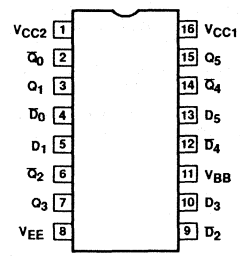
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic DIP	10216N
16-Pin Ceramic DIP	10216F

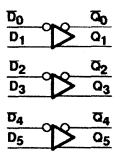
PIN DESCRIPTION

PINS	DESCRIPTION
$\overline{D}_0$, $\overline{D}_2$, $\overline{D}_4$; D_1, D_3, D_5	Data Inputs
$\overline{Q}_0$, $\overline{Q}_2$, $\overline{Q}_4$	Data Outputs (NOR)
Q_1, Q_3, Q_5	Data Outputs (OR)
V_{BB}	Reference Bias Voltage Output

PIN CONFIGURATION

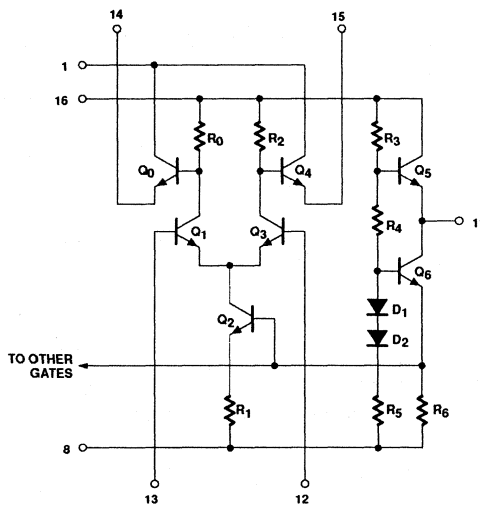


LOGIC DIAGRAM



$Q_0 = D_0$; $Q_1 = \overline{D}_0$
$Q_2 = D_2$; $Q_3 = \overline{D}_2$
$Q_4 = D_5$; $Q_5 = \overline{D}_4$

SIMPLIFIED SCHEMATIC



Line Receiver 10216

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILMIN} to each inverting input, one at a time, with V_{BB} applied to all non–inverting inputs and w/ V_{IHMAX} applied to all other inverting inputs. For $\overline{Q}_n$ outputs, apply V_{IHMAX} to each inverting input, one at a time, with V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]	–1060		–890	mV
		$T_A = +25°C$		–960		–810	mV
		$T_A = +85°C$		–890		–700	mV
V_{OHT}	High level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{ILT} to each inverting input, one at a time, w/ V_{BB} applied to all non–inverting inputs and with V_{IHMAX} applied to all other inverting inputs. For $\overline{Q}_n$ outputs, apply V_{IHT} to each inverting input, one at a time, with V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs.[4]	–1080			mV
		$T_A = +25°C$		–980			mV
		$T_A = +85°C$		–910			mV
V_{OLT}	Low level output threshold voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHT} to each inverting input, one at a time, w/ V_{BB} applied to all non–inverting inputs and V_{ILMIN} applied to all other inverting inputs. For $\overline{Q}_n$ outputs, apply V_{ILT} to each inverting input, one at a time, with V_{BB} applied to all non–inverting inputs and V_{IHMAX} applied to all other inverting inputs.[4]			–1655	mV
		$T_A = +25°C$				–1630	mV
		$T_A = +85°C$				–1595	mV
V_{OL}	Low level output voltage	$T_A = -30°C$	For Q_n outputs, apply V_{IHMAX} to each inverting input, one at a time, w/ V_{BB} applied to all non–inverting inputs and V_{ILMIN} applied to all other inverting inputs. For $\overline{Q}_n$ outputs, apply V_{ILMIN} to each inverting input, one at a time, with V_{BB} applied to all non–inverting inputs and V_{IHMAX} applied to all other inverting inputs.[4]	–1890		–1675	mV
		$T_A = +25°C$		–1850		–1650	mV
		$T_A = +85°C$		–1825		–1615	mV
I_{IH}	High level input current	$T_A = -30°C$	Apply V_{IHMAX} to each inverting input under test, one at a time, w/ V_{ILMIN} applied to all other inverting inputs and V_{BB} applied to all non–inverting inputs. Apply V_{IHMAX} to each non–inverting input under test, one at a time, with V_{ILMIN} applied to all other non–inverting inputs and V_{BB} applied to all inverting inputs.[4]			180	µA
		$T_A = +25°C$				115	µA
		$T_A = +85°C$		–1825		115	mV
$-I_{EE}$	V_{EE} supply current	$T_A = -30°C$	Apply V_{ILMIN} to all inverting inputs. Apply V_{BB} to all non–inverting inputs.			27	mA
		$T_A = +25°C$			20	25	mA
		$T_A = +85°C$				27	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{BB}	Reference voltage	T_A = –30°C	All inverting or all non–inverting	–1420		–1280	mV
		T_A = +25°C	input pins are tied to the V_{BB} pin	–1350	–1290	–1230	mV
		T_A = +85°C	during measurement.	–1295		–1150	mV
$-I_{CBO}$	Input leakage current	T_A = –30°C	Apply V_{EE} to each inverting input under test, one at			1.5	µA
		T_A = +25°C	a time, w/ V_{ILMIN} applied to all other inverting inputs			1.0	µA
		T_A = +85°C	and V_{BB} applied to all non–inverting inputs.[4]			1.0	µA

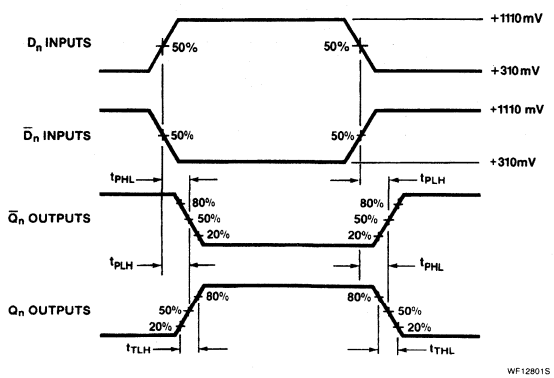
NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. Refer to DC Test Circuit.

AC ELECTRICAL CHARACTERISTICS V_{CC1} = V_{CC2} = ground, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = –30°C MIN.	LIMITS T_A = –30°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C TYP.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH}	Propagation delay	Waveform 1	1.00	2.60	1.00	1.50	2.50	1.00	2.80	ns
t_{PHL}	D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$		1.00	2.60	1.00	1.50	2.50	1.00	2.80	ns
t_{TLH}	Transition time		1.00	2.60	1.00	1.50	2.50	1.00	2.80	ns
t_{THL}	20% to 80%, 80% to 20%		1.00	2.60	1.00	1.50	2.50	1.00	2.80	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

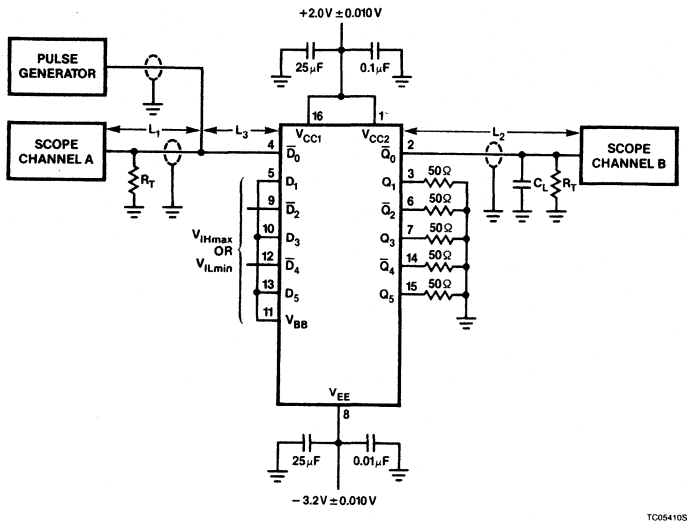
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times for Data to Output

Line Receiver 10216

AC TEST CIRCUIT



NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to V_{CC}. 0.01μF and 25μF from GND to V_{EE}. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

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ECN No.	99799
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

10231
Flip-Flop

Dual D-Type Master-Slave Flip-Flop (High-Speed)

FEATURES

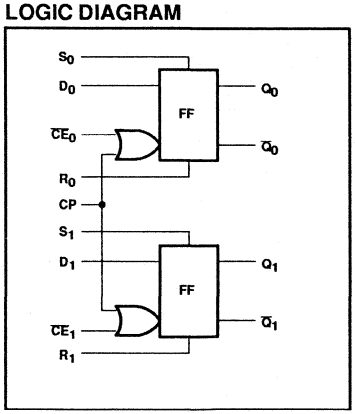
- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 52mA**

DESCRIPTION

The 10231 is a High-Speed Dual D-type Master-Slave Flip-Flop. It contains Asynchronous Set (S) and Reset (R) which override Clock (CP) and Clock Enable ($\overline{CE}_n$) inputs. Each flip-flop may be clocked separately by using the enable inputs for the clocking function and holding the Clock in the Low-State. For the two flip-flops to be clocked, the Clock must be used with the clock Enable inputs held in the Low-State.

The outputs of the 10231 change state with the positive transition of the Clock. Due to the master-slave structure of the device, a change in the information present at the data (D) input will not modify the output information at any other time. All unused inputs must be tied to V_{IL} or V_{EE}.

LOGIC DIAGRAM



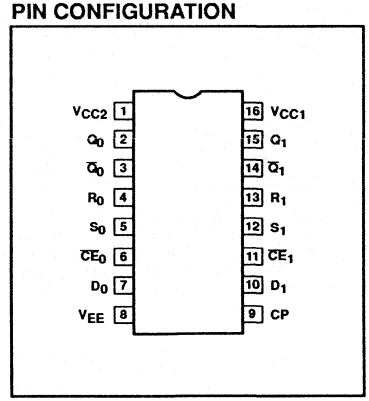
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic DIP	10231N
16-Pin Ceramic DIP	10231F

PIN DESCRIPTION

PINS	DESCRIPTION
D_0, D_1	Data Inputs
CP	Clock Input
$\overline{CE}_0$, $\overline{CE}_1$	Clock Enable Inputs
S_0, S_1	Set Inputs
R_0, R_1	Reset Inputs
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data Outputs

PIN CONFIGURATION



Flip-Flop 10231

FUNCTION TABLES

SYNCHRONOUS OPERATION

INPUTS			OUTPUT
D_n	C_P	$\overline{C_E}$*	Q_{n+1}**
L	L	L	Q_n
L	L	H	Q_n
L	H	L	L
L	H	H	Q_n
H	L	L	Q_n
H	L	H	Q_n
H	H	L	H
H	H	H	Q_n

* Conditions for CP and $\overline{CE}$ may be interchanged. In this table $\overline{CE}$ is static, while for CP and H represent a transition from Low to High between t_n and T_{n+1}.

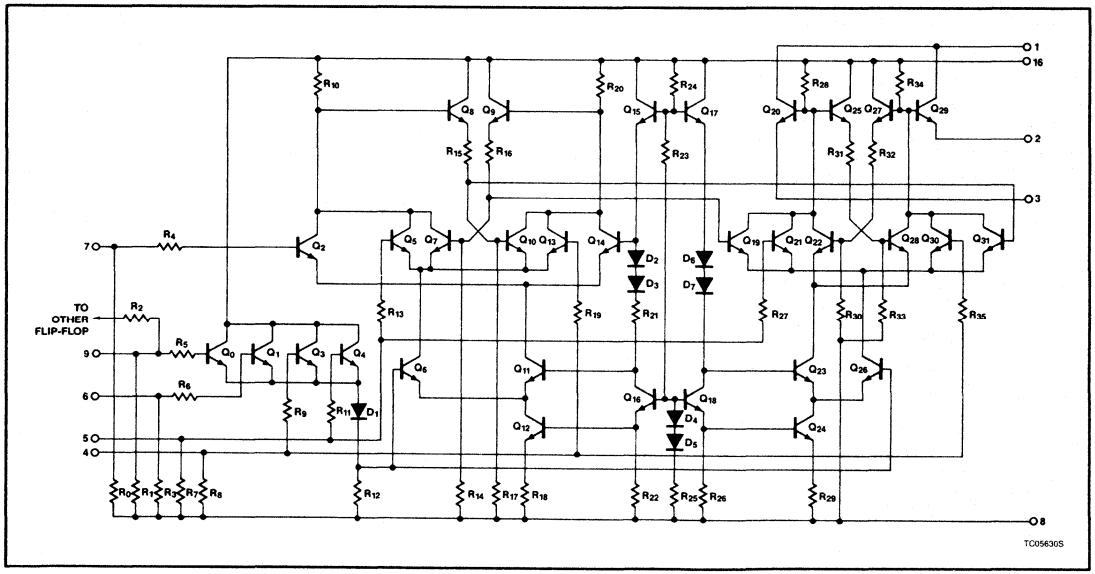
** R and S = Low

ASYNCHRONOUS OPERATION

INPUTS		OUTPUT
R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N

H = High Voltage Level
L = Low Voltage Level
N = Not allowed

SIMPLIFIED SCHEMATIC



Flip-Flop 10231

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q outputs, apply V_{IHMAX} to S_n inputs with	−1060		−890	mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}$ outputs, apply V_{IHMAX} to R_n inputs with	−960		−810	mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.	−890		−700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q outputs, apply V_{IHT} to S_n inputs, with	−1080			mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}$ outputs, apply V_{IHT} to R_n inputs, with	−980			mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.	−910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q outputs, apply V_{IHT} to R_n inputs, with			−1655	mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}$ outputs, apply V_{IHT} to S_n inputs, with			−1630	mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			−1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q outputs, apply V_{IHMAX} to R_n inputs, with	−1890		−1675	mV
			$T_A = +25°C$	V_{ILMIN} applied to all other inputs. For $\overline{Q}$ outputs, apply V_{IHMAX} to S_n inputs, with	−1850		−1650	mV
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.	−1825		−1615	mV
I_{IH}	High level input current	D_n, $\overline{CE}_n$ inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under test, one at a time, with V_{ILMIN} applied to all other inputs.			350	µA
			$T_A = +25°C$				220	µA
			$T_A = +85°C$				220	µA
		R_n, S_n inputs	$T_A = -30°C$				650	µA
			$T_A = +25°C$				410	µA
			$T_A = +85°C$				410	µA
		CP input	$T_A = -30°C$	Apply V_{IHMAX} to CP input with V_{ILMIN} applied to all other inputs.			460	µA
			$T_A = +25°C$				290	µA
			$T_A = +85°C$				290	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under test, one at a time, with V_{IHMAX} applied to all other inputs.	0.5			µA
			$T_A = +25°C$		0.5			µA
			$T_A = +85°C$		0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				72	mA
			$T_A = +25°C$			52	65	mA
			$T_A = +85°C$				72	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$T_A = +25°C$			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation					0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation					0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

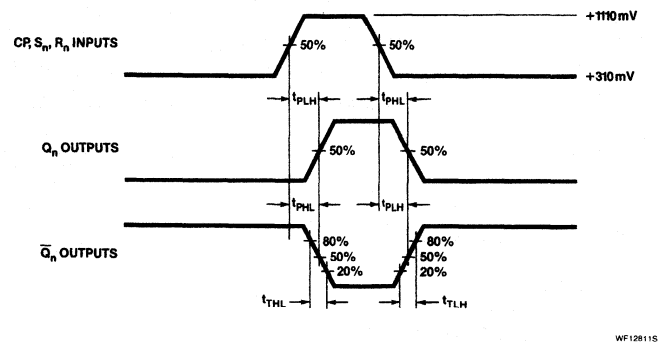
Flip-Flop 10231

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 0.010V$

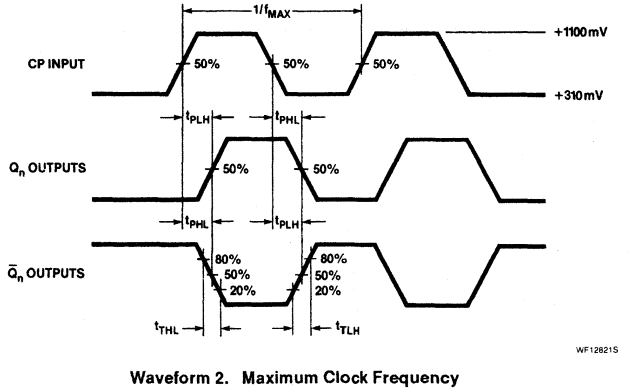
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS							UNIT
			$T_A = -30°C$		$T_A = +25°C$			$T_A = +85°C$		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency	Waveform 2	200		200	225		200		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	1.50 1.50	3.40 3.40	1.50 1.50	2.00 2.00	3.30 3.30	1.60 1.60	3.70 3.70	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n, R_n to Q_n, $\overline{Q}_n$		1.10 1.10	3.40 3.40	1.10 1.10	2.00 2.00	3.30 3.30	1.20 1.20	3.70 3.70	ns ns
t_s	Setup time D_n to CP	Waveform 3	1.50		1.00			1.50		ns
t_h	Hold time CP to D_n	Waveform 3	0.90		0.75			0.90		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	0.90 0.90	3.30 3.30	1.00 1.00	1.30 1.30	3.10 3.10	1.00 1.00	3.60 3.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS

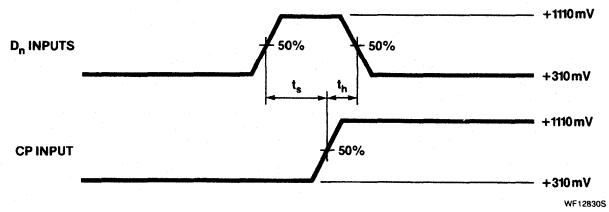


Waveform 1. Propagation Delay and Transition Times, CP, S_n, R_n Inputs to Outputs



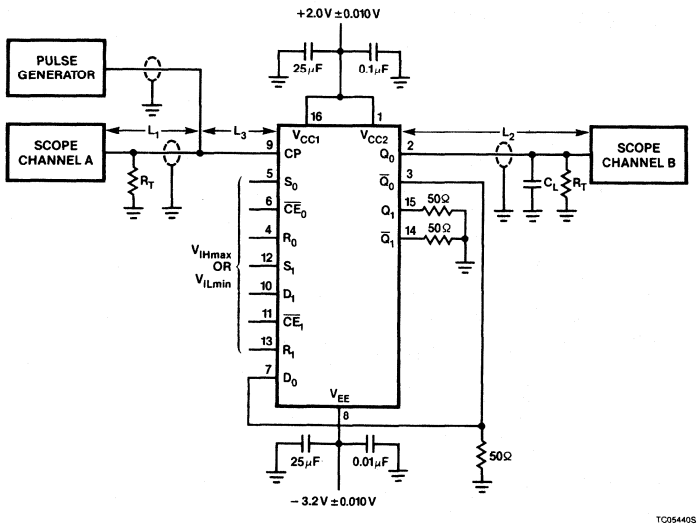
Waveform 2. Maximum Clock Frequency

AC WAVEFORMS (Continued)



Waveform 3. Setup and Hold Times for Data to Clock

TOGGLE FREQUENCY TEST CIRCUIT



NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to V_{CC}. 0.01μF and 25μF from GND to V_{EE}. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. R_T = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. C_L = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Section 7
100K Series Data Sheets

ECL Products

INDEX

100101	Triple 5–Input OR/NOR Gate	357
100102	Quint 2–Input OR/NOR Gate With Enable	362
100107	Quint Exclusive OR/Exclusive NOR Gate With Compare Output	367
100112	Quad Driver	373
100113	Quad Driver (High speed)	378
100114	Quint Differential Line Receiver	383
100117	Triple 1–2–2 Input OR–AND/OR–AND–INVERT Gate	389
100118	Quint 2–4–4–4–5 Input OR–AND Gate	394
100122	9–Bit Buffer	399
100123	Bus Driver	403
100124	Hex TTL–to–ECL Translator	409
100124A	Hex TTL–to–ECL Translator (low power)	409
100125	Hex ECL–to–TTL Translator	416
100126	9–Bit Backplane Driver	423
100131	Triple D–Type Master–Slave Flip–Flop	427
100136	Counter/Shift Register	436
100141	8–Bit Shift Register	447
100150	Hex D–Type Latch	455
100151	Hex D–Type Master–Slave Flip–Flop	462
100155	Quad 2–Way Multiplexer/Latch	469
100158	8–Bit Shift Matrix	476
100160	Dual 9–Bit Parity Checker/Generator/8–Bit Comparator	481
100163	Dual 8–Input Multiplexer	486
100164	16–Input Multiplexer	492
100165	Universal Priority Encoder	498
100166	9–Bit Comparator	505
100170	Universal Demultiplexer/Decoder	510
100171	Triple 4–Input Multiplexer	516
100175	100K–to–10K Translator	522
100179	Carry Look–Ahead Generator	529
100180	High speed 6–Bit Adder	536
100181	4–Bit Binary/BCD ALU	542
100231	Triple D–Type Master–Slave Flip–Flop (High speed version of 100131)	552
100255	Quint Bidirectional 100K–to–10K Translator	561
100790	9–Bit Transceiver	572
100982	Hex ECL–TTL Translating Transceiver with Registers	579
100984	Quad ECL–TTL Translating Transceiver with Registers	593
100990	9–Bit Transceiver	606

Document No.	853–0604
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100101

Triple 5–Input OR/NOR Gate

FEATURES

- **Typical propagation delay: 0.75ns**
- **Typical supply current ($-I_{EE}$): 27mA**

DESCRIPTION

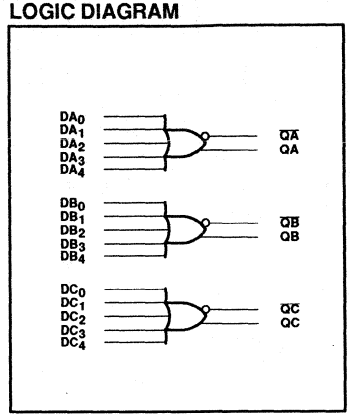
The 100101 is a triple 5–input OR/NOR gate.

All unused inputs can be left open due to integrated pull–down resistors.

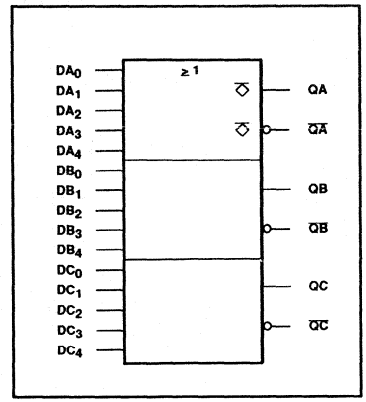
PIN DESCRIPTION

PINS	DESCRIPTION
$DA_0 - DA_4$, $DB_0 - DB_4$, $DC_0 - DC_4$	Data Inputs
QA, QB, QC	True Data Outputs (OR)
$\overline{QA}$, $\overline{QB}$, $\overline{QC}$	Complementary Data Outputs (NOR)

LOGIC DIAGRAM



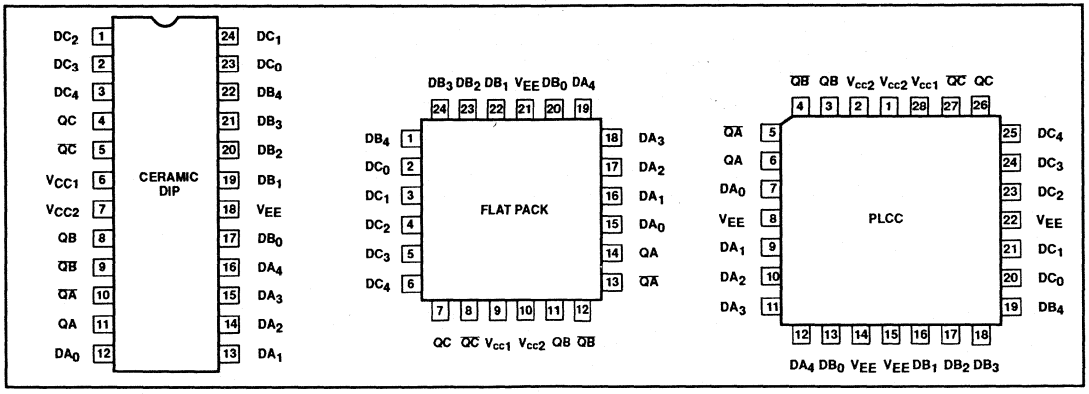
IEC/IEEE SYMBOL



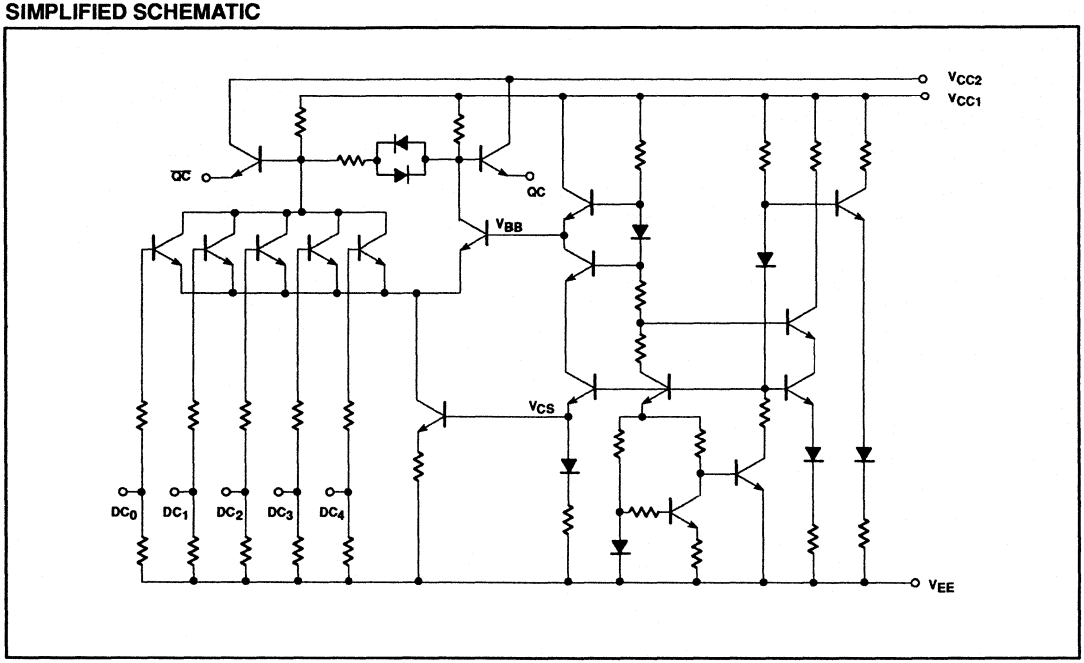
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100101F
24–Pin Ceramic Flat Pack	100101Y
28–Pin PLCC	100101A

PIN CONFIGURATIONS



SIMPLIFIED SCHEMATIC



FUNCTION TABLE

INPUTS					OUTPUTS	
DA_0	DA_1	DA_2	DA_3	DA_4	$\overline{QA}$	QA
L	L	L	L	L	H	L
H	X	X	X	X	L	H
X	H	X	X	X	L	H
X	X	H	X	X	L	H
X	X	X	H	X	L	H
X	X	X	X	H	L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family.		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs Loaded with 50Ω to –2.0V ± 0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					350	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}.			18	27	38	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n to QA and $\overline{QA}$, DB_n to QB and $\overline{QB}$, DC_n to QC and $\overline{QC}$	Waveform 1	0.50 0.50	1.15 1.15	0.50 0.50	1.15 1.15	0.55 0.55	1.30 1.30	ns ns
t_{TLH} t_{THL}	Transition time for all outputs		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.10 1.10	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n to QA and $\overline{QA}$, DB_n to QB and $\overline{QB}$, DC_n to QC and $\overline{QC}$	Waveform 1	0.50 0.50	1.15 1.15	0.50 0.50	1.15 1.15	0.55 0.55	1.30 1.30	ns ns
t_{TLH} t_{THL}	Transition time for all outputs		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.10 1.10	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n to QA and $\overline{QA}$, DB_n to QB and $\overline{QB}$, DC_n to QC and $\overline{QC}$	Waveform 1	0.50 0.50	0.95 0.95	0.50 0.50	0.95 0.95	0.55 0.55	1.10 1.10	ns ns
t_{TLH} t_{THL}	Transition time for all outputs		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.10 1.10	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

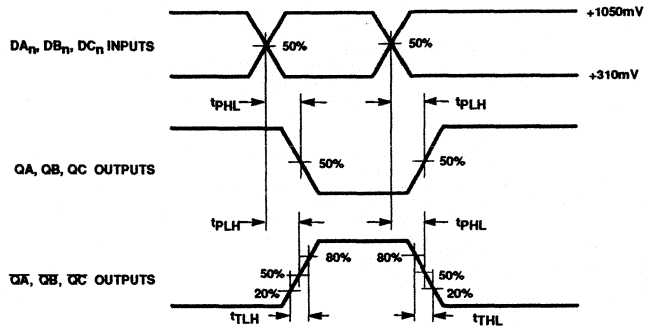
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n to QA and $\overline{QA}$, DB_n to QB and $\overline{QB}$, DC_n to QC and $\overline{QC}$	Waveform 1	0.50 0.50	0.95 0.95	0.50 0.50	0.95 0.95	0.55 0.55	1.10 1.10	ns ns
t_{TLH} t_{THL}	Transition time for all outputs		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.10 1.10	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Philips Components

Document No.	853–0605
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100102

Quint 2–Input OR–NOR Gate With Common Enable

FEATURES

- **Typical propagation delay: 0.75ns**
- **Typical supply current ($-I_{EE}$): 55mA**

DESCRIPTION

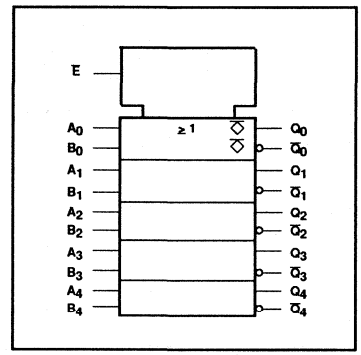
The 100102 has five 2–input OR–NOR gates with a common enable.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_4$, $B_0 - B_4$	Data Inputs
$\overline{E}$	Enable Input
$Q_0 - Q_4$	True Data Outputs (OR)
$\overline{Q}_0 - \overline{Q}_4$	Complementary Data Outputs (NOR)

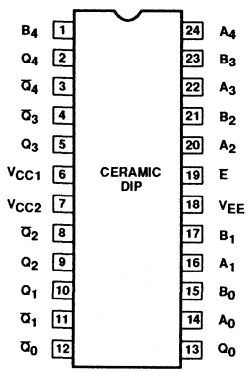
IEC/IEEE SYMBOL

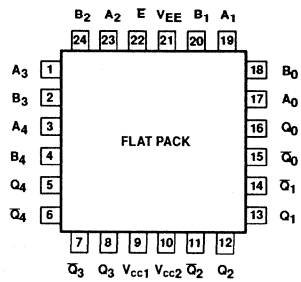


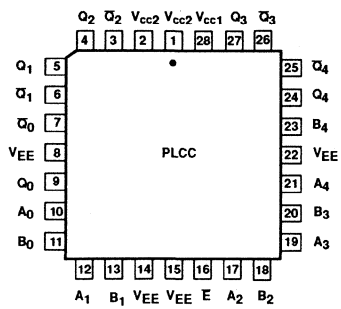
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100102F
24–Pin Ceramic Flat Pack	100102Y
28–Pin PLCC	100102A

PIN CONFIGURATIONS



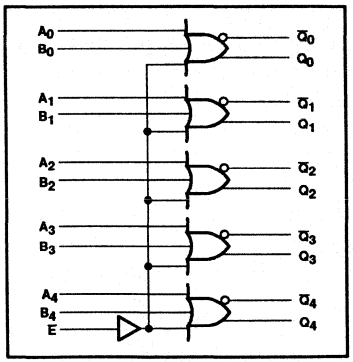




Gate

100102

LOGIC DIAGRAM

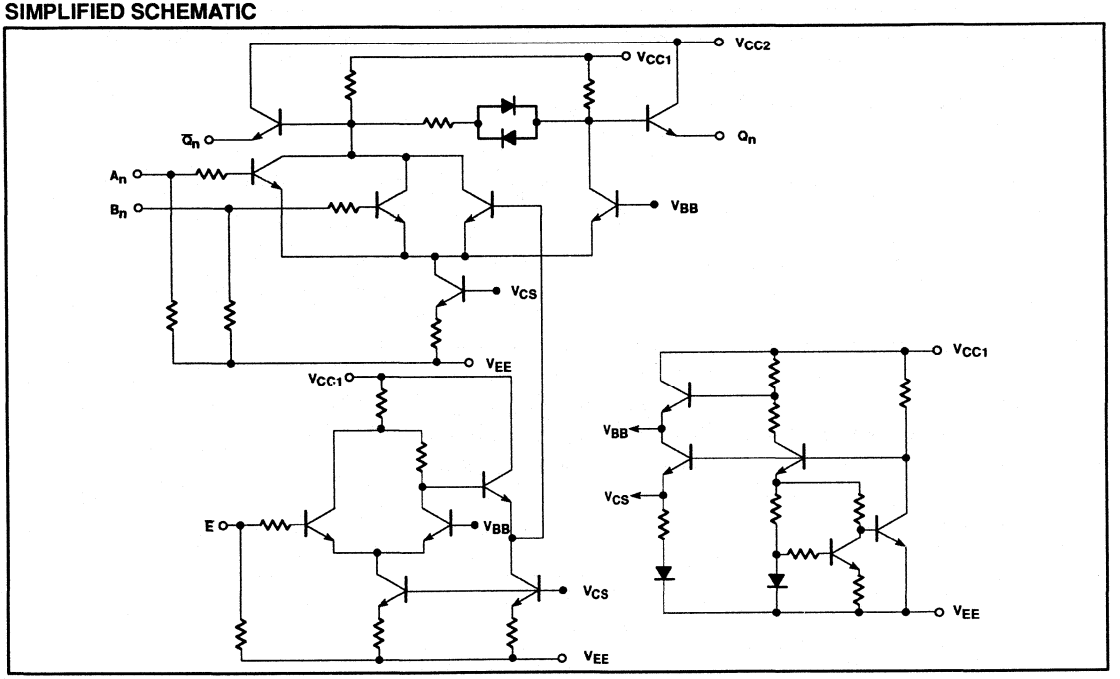


FUNCTION TABLE

INPUTS			OUTPUTS	
D_0	D_1	$\overline{E}$	Q_0	$\overline{Q}_0$
X	X	H	H	L
X	H	X	H	L
H	X	X	H	L
L	L	L	L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE: Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs Loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	D_n inputs	One input under test at V_{IHMAX}.					350	µA
		$\overline{E}$ input	Other inputs at V_{ILMIN}.					300	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}.			38	55	80	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.35 1.35	0.45 0.45	1.15 1.15	0.45 0.45	1.40 1.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n or $\overline{Q}_n$		0.90 0.90	2.15 2.15	0.95 0.95	2.15 2.15	0.95 0.95	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.10 1.10	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.35 1.35	0.45 0.45	1.15 1.15	0.45 0.45	1.40 1.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n or $\overline{Q}_n$		0.90 0.90	2.15 2.15	0.95 0.95	2.15 2.15	0.95 0.95	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.10 1.10	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.15 1.15	0.45 0.45	0.95 0.95	0.45 0.45	1.20 1.20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n or $\overline{Q}_n$		0.90 0.90	1.95 1.95	0.95 0.95	1.95 1.95	0.95 0.95	2.00 2.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.10 1.10	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

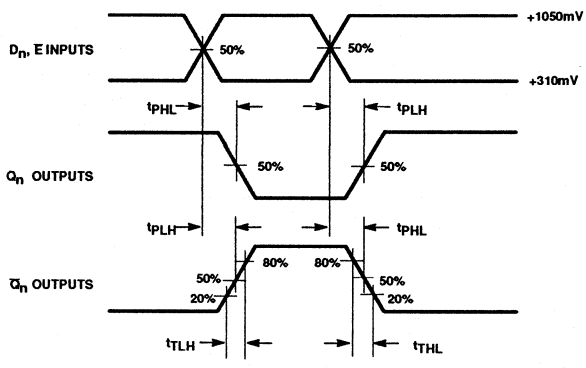
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.15 1.15	0.45 0.45	0.95 0.95	0.45 0.45	1.20 1.20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n or $\overline{Q}_n$		0.90 0.90	1.95 1.95	0.95 0.95	1.95 1.95	0.95 0.95	2.00 2.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.10 1.10	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Philips Components

Document No.	853–0606
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100107

Quint Exclusive–OR/Exclusive–NOR Gate With Compare Output

FEATURES

- **Typical propagation delay: 0.95ns**
- **Typical supply current ($-I_{EE}$): 68mA**

DESCRIPTION

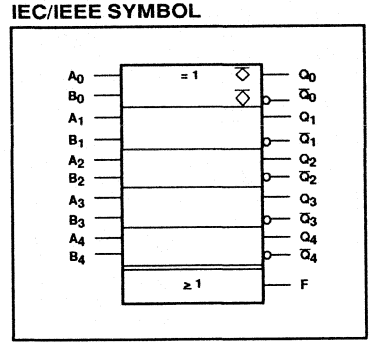
The 100107 has five 2–input, 2–output Exclusive–OR/Exclusive–NOR gates with a Compare Output.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_4$, $B_0 - B_4$	Data Inputs
$Q_0 - Q_4$	Exclusive–OR Outputs
$\overline{Q}_0 - \overline{Q}_4$	Exclusive–NOR Outputs
F	Compare Output

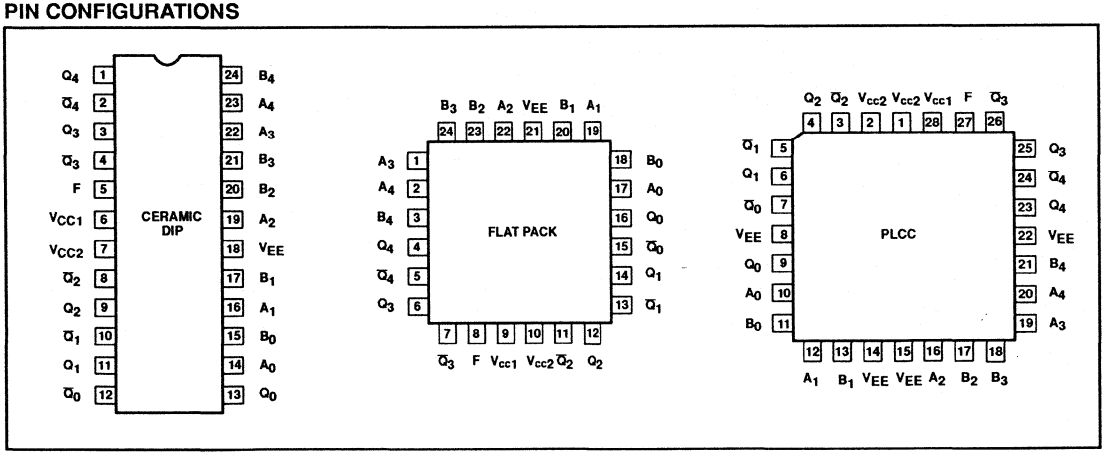
IEC/IEEE SYMBOL



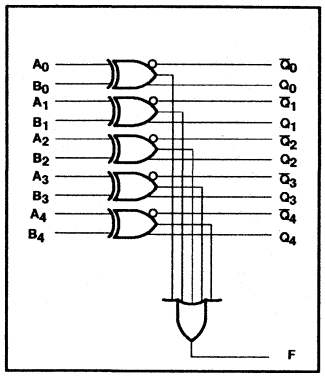
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100107F
24–Pin Ceramic Flat Pack	100107Y
28–Pin PLCC	100107A

PIN CONFIGURATIONS



LOGIC DIAGRAM



FUNCTION TABLE (For Q_n and $\overline{Q}_n$)

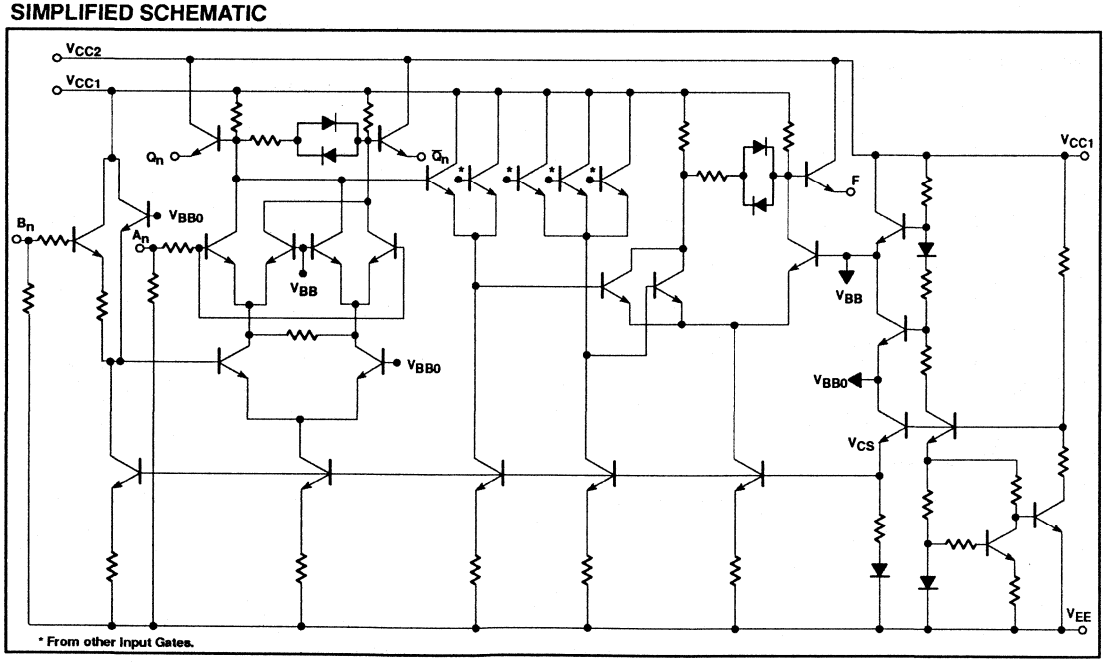
INPUTS		OUTPUTS	
A_n	B_n	$Q_n = A_n \oplus B_n$	$\overline{Q}_n = \overline{A_n \oplus B_n}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

FUNCTION TABLE (For the Compare Output)

INPUTS					OUTPUT
$A_0 \oplus B_0$	$A_1 \oplus B_1$	$A_2 \oplus B_2$	$A_3 \oplus B_3$	$A_4 \oplus B_4$	F
L	L	L	L	L	L
H	X	X	X	X	H
X	H	X	X	X	H
X	X	H	X	X	H
X	X	X	H	X	H
X	X	X	X	H	H

NOTES:
⊕ = Exclusive–OR operation
H = High voltage level
L = Low voltage level
X = Don't care

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltag when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs Loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	B_n	One input under test at V_{IHMAX}.					250	µA
		A_n	Other inputs at V_{ILMIN}.					350	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}.			46	68	96	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C MIN.	LIMITS T_A = 0°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH}	Propagation delay B_n to Q_n or $\overline{Q}_n$	Waveform 1	0.55	1.90	0.55	1.80	0.55	1.90	ns
t_{PHL}			0.55	1.90	0.55	1.80	0.55	1.90	ns
t_{PLH}	Propagation delay A_n to Q_n or $\overline{Q}_n$		0.55	1.70	0.55	1.60	0.55	1.70	ns
t_{PHL}			0.55	1.70	0.55	1.60	0.55	1.70	ns
t_{PLH}	Propagation delay A_n, B_n to F		1.15	2.75	1.15	2.75	1.15	3.00	ns
t_{PHL}			1.15	2.75	1.15	2.75	1.15	3.00	ns
t_{TLH}	Transition time Q_n, $\overline{Q}_n$ or F		0.45	1.70	0.45	1.55	0.45	1.70	ns
t_{THL}			0.45	1.70	0.45	1.55	0.45	1.70	ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay B_n to Q_n or $\overline{Q}_n$	Waveform 1	0.55 0.55	1.90 1.90	0.55 0.55	1.80 1.80	0.55 0.55	1.90 1.90	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n or $\overline{Q}_n$		0.55 0.55	1.70 1.70	0.55 0.55	1.60 1.60	0.55 0.55	1.70 1.70	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F		1.15 1.15	2.75 2.75	1.15 1.15	2.75 2.75	1.15 1.15	3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$ or F		0.45 0.45	1.70 1.70	0.45 0.45	1.55 1.55	0.45 0.45	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay B_n to Q_n or $\overline{Q}_n$	Waveform 1	0.55 0.55	1.70 1.70	0.55 0.55	1.60 1.60	0.55 0.55	1.70 1.70	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n or $\overline{Q}_n$		0.55 0.55	1.50 1.50	0.55 0.55	1.40 1.40	0.55 0.55	1.50 1.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F		1.15 1.15	2.55 2.55	1.15 1.15	2.55 2.55	1.15 1.15	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$ or F		0.45 0.45	1.70 1.70	0.45 0.45	1.55 1.55	0.45 0.45	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

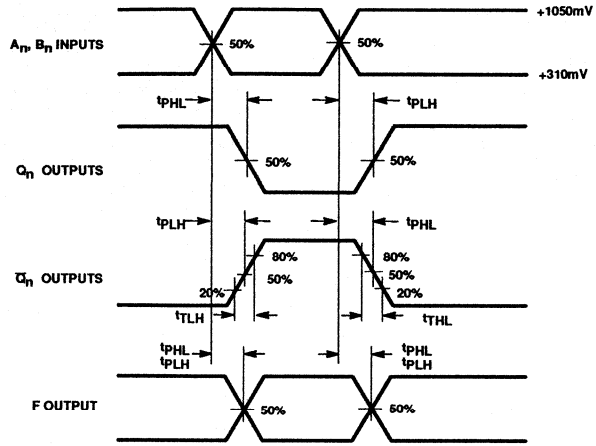
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay B_n to Q_n or $\overline{Q}_n$	Waveform 1	0.55 0.55	1.70 1.70	0.55 0.55	1.60 1.60	0.55 0.55	1.70 1.70	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n or $\overline{Q}_n$		0.55 0.55	1.50 1.50	0.55 0.55	1.40 1.40	0.55 0.55	1.50 1.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F		1.15 1.15	2.55 2.55	1.15 1.15	2.55 2.55	1.15 1.15	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$ or F		0.45 0.45	1.70 1.70	0.45 0.45	1.55 1.55	0.45 0.45	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–0607
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100112

Quad Driver

FEATURES

- **Typical propagation delay: 0.85ns for data inputs, 1.4ns for Enable Input**
- **Typical supply current ($-I_{EE}$): 73mA**

DESCRIPTION

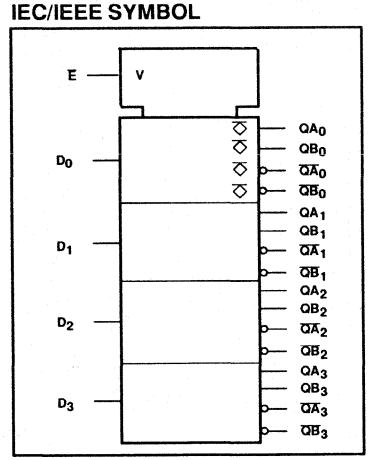
The 100112 has four, 2–input OR–NOR gates. One input from each gate is tied together to form a common enable. Each gate has two OR outputs and two NOR outputs. For a faster version of this part, see the 100113.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
$\overline{E}$	Enable Input
$QA_0 - QA_3$, $QB_0 - QB_3$	True Data Outputs (OR)
$\overline{QA}_0 - \overline{QA}_3$, $\overline{QB}_0 - \overline{QB}_3$	Complementary Data Outputs (NOR)

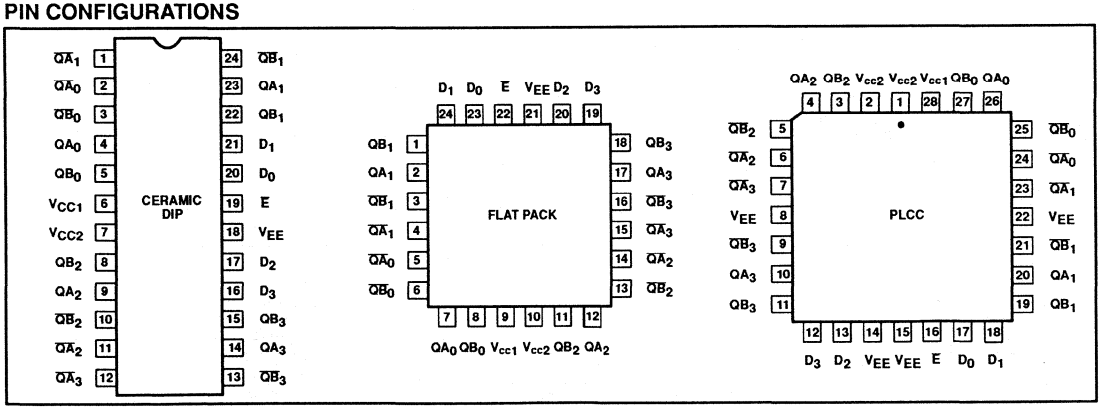
IEC/IEEE SYMBOL



ORDERING INFORMATION

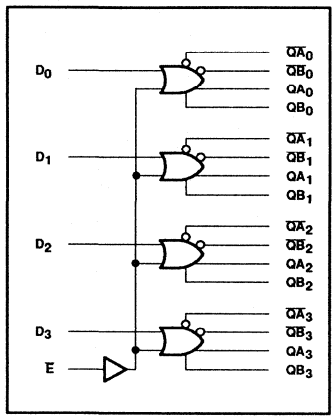
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100112F
24–Pin Ceramic Flat Pack	100112Y
28–Pin PLCC	100112A

PIN CONFIGURATIONS



Driver | 100112

LOGIC DIAGRAM

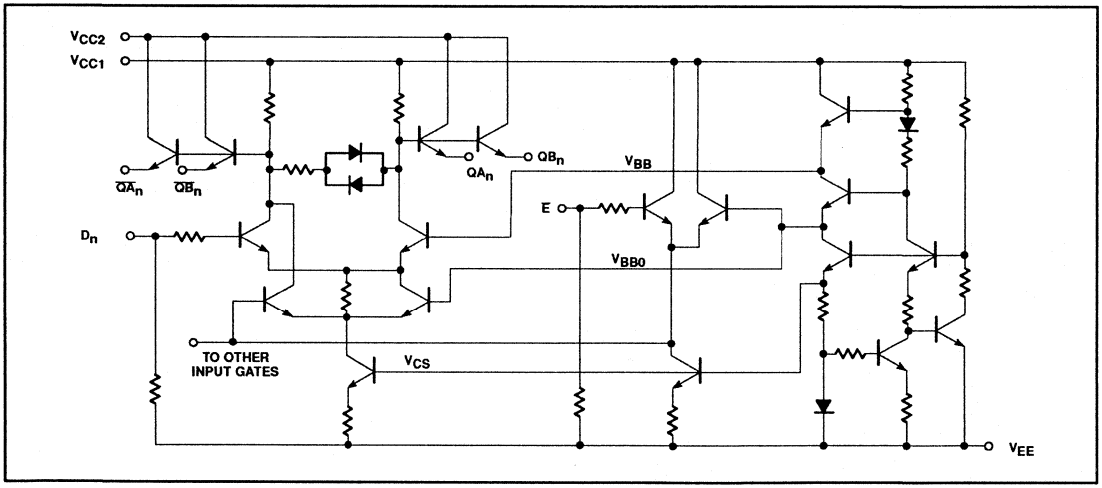


FUNCTION TABLE (One Gate)

INPUTS		OUTPUTS			
D_n	$\overline{E}$	$\overline{QA}_n$	$\overline{QB}_n$	QA_n	QB_n
H	X	L	L	H	H
X	H	L	L	H	H
L	L	H	H	L	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs Loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	D_n inputs	One input under test at V_{IHMAX}.					550	µA
		$\overline{E}$ input	Other inputs at V_{ILMIN}.					450	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}.			51	73	106	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$	Waveform 1	0.55 0.55	1.40 1.40	0.55 0.55	1.35 1.35	0.45 0.45	1.40 1.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$		0.65 0.65	1.90 1.90	0.65 0.65	1.90 1.90	0.65 0.65	1.90 1.90	ns ns
t_{TLH} t_{THL}	Transition time all outputs		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$	Waveform 1	0.55 0.55	1.40 1.40	0.55 0.55	1.35 1.35	0.45 0.45	1.40 1.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$		0.65 0.65	1.90 1.90	0.65 0.65	1.90 1.90	0.65 0.65	1.90 1.90	ns ns
t_{TLH} t_{THL}	Transition time all outputs		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$	Waveform 1	0.55 0.55	1.20 1.20	0.55 0.55	1.15 1.15	0.45 0.45	1.20 1.20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$		0.65 0.65	1.70 1.70	0.65 0.65	1.70 1.70	0.65 0.65	1.70 1.70	ns ns
t_{TLH} t_{THL}	Transition time all outputs		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

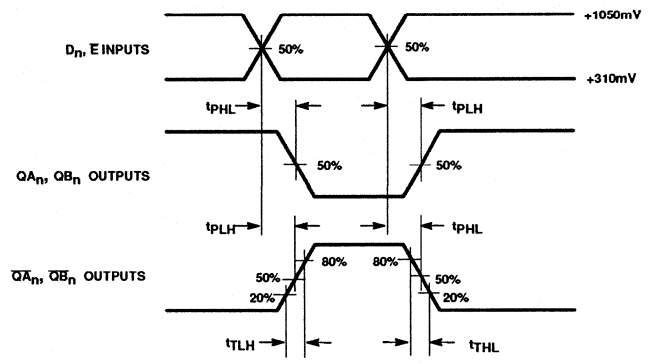
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$	Waveform 1	0.55 0.55	1.20 1.20	0.55 0.55	1.15 1.15	0.45 0.45	1.20 1.20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$		0.65 0.65	1.70 1.70	0.65 0.65	1.70 1.70	0.65 0.65	1.70 1.70	ns ns
t_{TLH} t_{THL}	Transition time all outputs		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

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ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100113

Quad Driver (High Speed)

FEATURES

- **Typical propagation delay: 0.80ns for data inputs, 1.4ns for Enable Input**
- **Typical supply current ($-I_{EE}$): 75mA**

DESCRIPTION

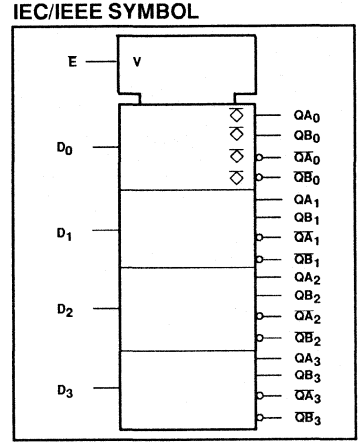
The 100113 has four, 2–input OR–NOR gates. One input from each gate is tied together to form a common enable. Each gate has two OR outputs and two NOR outputs. The 100113 is a high–speed version of the 100112.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
$\overline{E}$	Enable Input
$QA_0 - QA_3$, $QB_0 - QB_3$	True Data Outputs (OR)
$\overline{QA}_0 - \overline{QA}_3$, $\overline{QB}_0 - \overline{QB}_3$	Complementary Data Outputs (NOR)

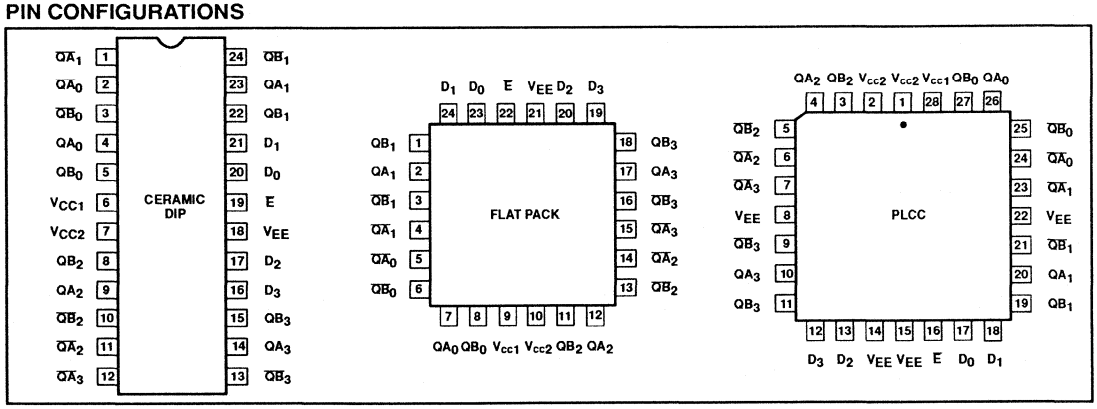
IEC/IEEE SYMBOL



ORDERING INFORMATION

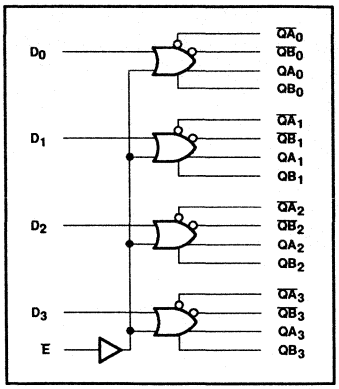
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100113F
24–Pin Ceramic Flat Pack	100113Y
28–Pin PLCC	100113A

PIN CONFIGURATIONS



Driver | 100113

LOGIC DIAGRAM

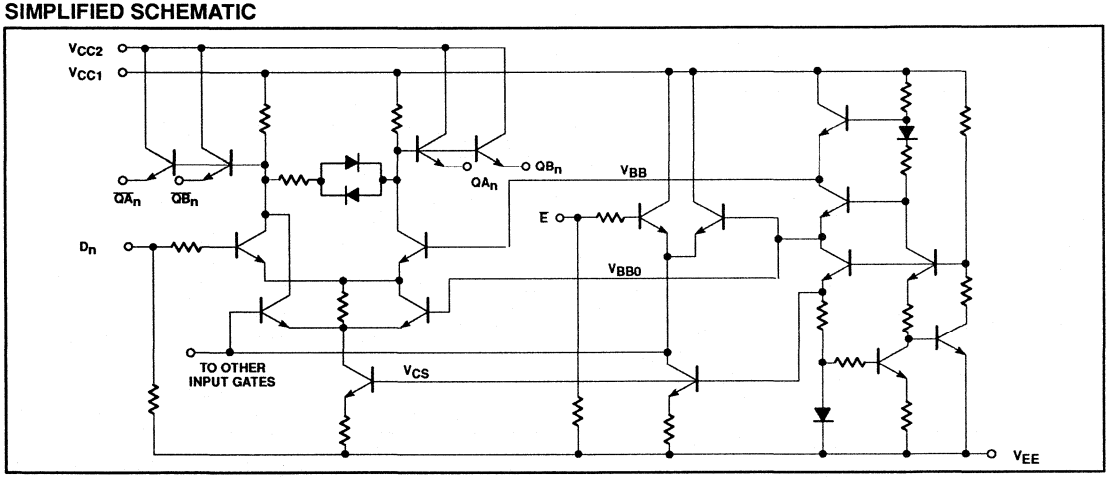


FUNCTION TABLE (One Gate)

INPUTS		OUTPUTS			
D_n	$\overline{E}$	$\overline{QA}_n$	$\overline{QB}_n$	QA_n	QB_n
H	X	L	L	H	H
X	H	L	L	H	H
L	L	H	H	L	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V) the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs Loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	D_n inputs	One input under test at V_{IHMAX}.					550	µA
		E input	Other inputs at V_{ILMIN}.					450	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}.			54	75	116	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.35 1.35	0.45 0.45	1.40 1.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$		0.55 0.55	1.90 1.90	0.55 0.55	1.90 1.90	0.55 0.55	1.90 1.90	ns ns
t_{TLH} t_{THL}	Transition time all outputs		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.35 1.35	0.45 0.45	1.40 1.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$		0.55 0.55	1.90 1.90	0.55 0.55	1.90 1.90	0.55 0.55	1.90 1.90	ns ns
t_{TLH} t_{THL}	Transition time all outputs		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$	Waveform 1	0.45 0.45	1.20 1.20	0.45 0.45	1.15 1.15	0.45 0.45	1.20 1.20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$		0.55 0.55	1.70 1.70	0.55 0.55	1.70 1.70	0.55 0.55	1.70 1.70	ns ns
t_{TLH} t_{THL}	Transition time all outputs		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

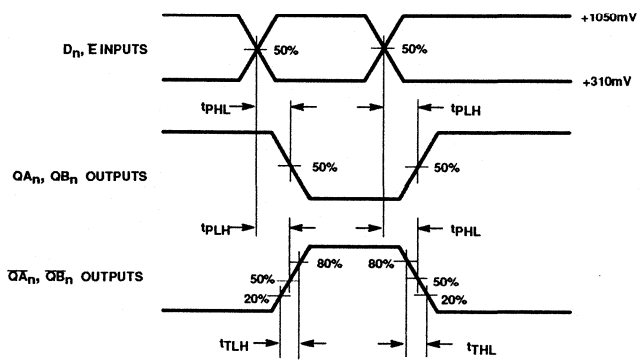
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$	Waveform 1	0.45 0.45	1.20 1.20	0.45 0.45	1.15 1.15	0.45 0.45	1.20 1.20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to QA_n, QB_n, $\overline{QA}_n$, $\overline{QB}_n$		0.55 0.55	1.70 1.70	0.55 0.55	1.70 1.70	0.55 0.55	1.70 1.70	ns ns
t_{TLH} t_{THL}	Transition time all outputs		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–0609
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100114

Quint Differential Line Driver

FEATURES

•Typical supply current ($-I_{EE}$): 73mA

DESCRIPTION

The 100114 contains five receivers with differential inputs (D_n, $\overline{D}_n$) and complementary outputs (Q_n, $\overline{Q}_n$). The inputs allow each receiver to be used in an inverting, non–inverting, or differential fashion. An internal reference voltage generator provides V_{BB} for single–ended operation. An external supply can also be used as the reference voltage. When used in the differential mode, common mode rejection makes this device tolerant of ground offsets and transients between signal source and the receiver.

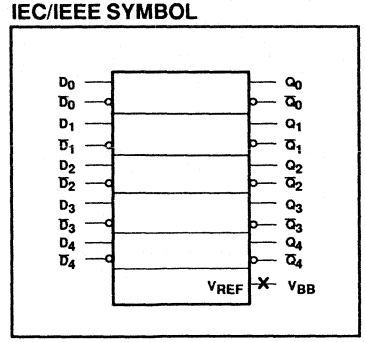
If both receiver inputs are left open or tied to the same voltage, the true output Q_n will be at a low logic level, and the complementary output $\overline{Q}_n$ will be high.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_4$,	True data Inputs
$\overline{D}_0 - \overline{D}_4$,	Complementary data inputs
$Q_0 - Q_4$	True data outputs
$\overline{Q}_0 - \overline{Q}_4$	Complementary data outputs
V_{BB}	Reference voltage output

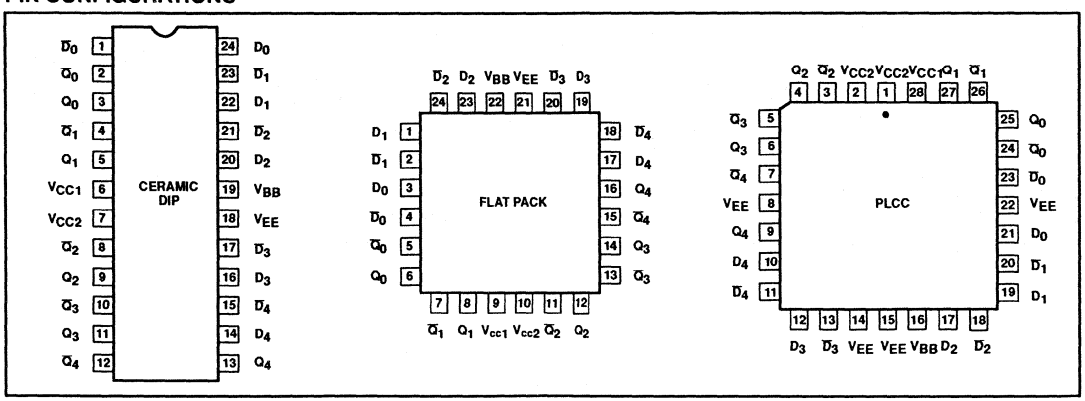
IEC/IEEE SYMBOL



ORDERING INFORMATION

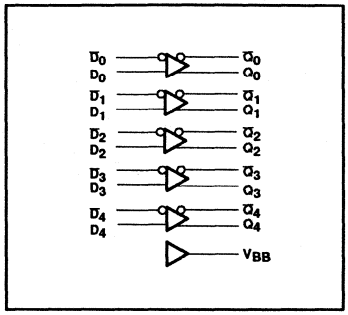
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100114F
24–Pin Ceramic Flat Pack	100114Y
28–Pin PLCC	100114A

PIN CONFIGURATIONS



Line Receiver 100114

LOGIC DIAGRAM

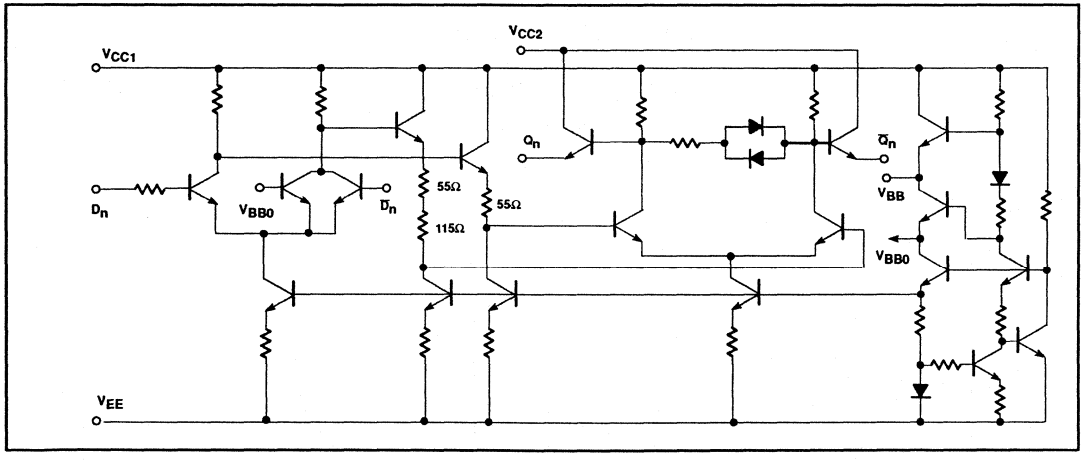


FUNCTION TABLE (One Gate)

INPUTS		OUTPUTS	
D_n	$\overline{D}_n$	Q_n	$\overline{Q}_n$
H	V_{BB}	H	L
L	V_{BB}	L	H
V_{BB}	H	L	H
V_{BB}	L	H	L
$V_{ID} \geq 0V$		L	H
$V_{ID} \leq -V_{DIFFMIN}$		H	L
$-V_{DIFFMIN} < V_{ID} < 0V$		*	*
open	open	L	H
V_{CC}	V_{CC}	L	H
V_{EE}	V_{EE}	L	H

NOTES:
H = High voltage level
L = Low voltage level
* = Indeterminate state
V_{BB} = Threshold level provided by reference voltage output of 100114.
V_{ID} = The voltage at $\overline{D}_n$ minus the voltage at D_n

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or 10KH ECL family		–5.7			V
V_{IH}[2]	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}[2]	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
V_{CM}[3]	Common mode voltage	V_{EE} = –4.2V				
		V_{EE} = –4.5V	0		1.0	V
		V_{EE} = –4.8V				
V_{DIFF}[4]	Differential input voltage	V_{EE} = –4.2V				
		V_{EE} = –4.5V	150			V
		V_{EE} = –4.8V				
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTES:
1. When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.
2. For input voltages outside the specified V_{IH} and V_{IL} ranges, the output voltage specifications will hold true. However, the AC performance will be according to specification only if two conditions are met: First, either D_n or $\overline{D}_n$ must be above –2300mV at all times. Second, both D_n and $\overline{D}_n$ must be below –230mV.
3. V_{CM} is added or subtracted with respect to V_{BB}. For common–mode applications, the total voltage applied to D_n or $\overline{D}_n$ should be no less than V_{BB}–V_{CM} (max) and no greater than V_{BB} + V_{CM} (max).
4. V_{DIFF} (min) is the minimum voltage difference by which D_n must exceed $\overline{D}_n$ such that output Q_n will assume a high logic level. See Function Table.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
V_{BB}	Reference output voltage	All D_n open, all $\overline{D}_n$ connected to V_{BB} pin.		V_{EE} = –4.5V	–1380	–1320	–1260	mV
				V_{EE} = –4.8V to –4.2V	–1396	–1320	–1244	mV
I_{IH}	High level input current	One D_n input under test at V_{IHMAX}. All other D_n inputs at V_{ILMIN}. All $\overline{D}_n$ inputs at V_{BB}.					65	µA
$-I_{CBO}$	Input leakage current	One D_n input under test at V_{EE}. All other D_n inputs at V_{ILMIN}. All $\overline{D}_n$ inputs at V_{BB}.					10	µA
$-I_{EE}$	V_{EE} supply current	Inputs open			51	73	106	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	0.55 0.55	2.20 2.20	0.60 0.60	2.20 2.20	0.70 0.70	2.40 2.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.30 1.30	0.45 0.45	1.20 1.20	0.45 0.45	1.30 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	0.55 0.55	2.20 2.20	0.60 0.60	2.20 2.20	0.70 0.70	2.40 2.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.30 1.30	0.45 0.45	1.20 1.20	0.45 0.45	1.30 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	0.55 0.55	2.00 2.00	0.60 0.60	2.00 2.00	0.70 0.70	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.30 1.30	0.45 0.45	1.20 1.20	0.45 0.45	1.30 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

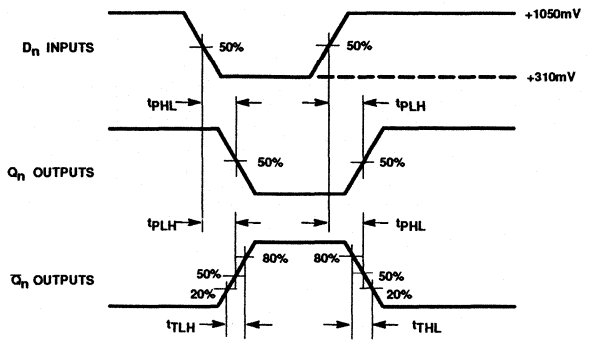
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n, $\overline{D}_n$ to Q_n, $\overline{Q}_n$	Waveform 1	0.55 0.55	2.00 2.00	0.60 0.60	2.00 2.00	0.70 0.70	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.30 1.30	0.45 0.45	1.20 1.20	0.45 0.45	1.30 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

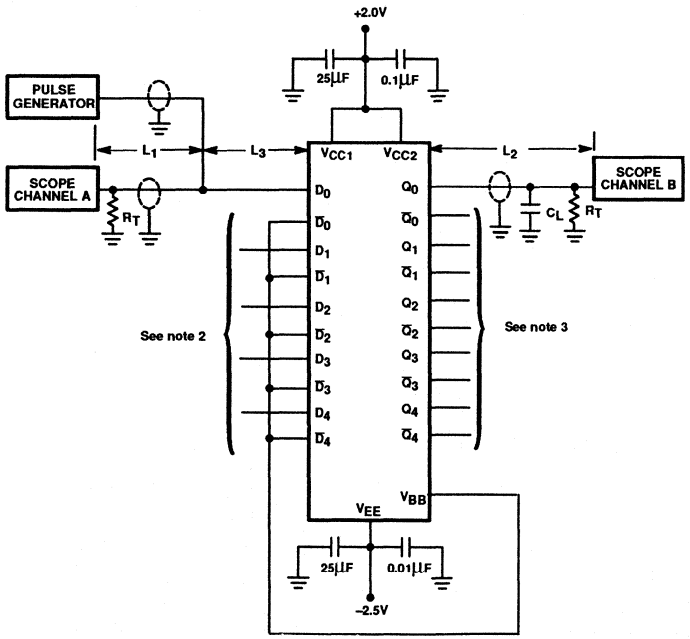
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
1. All power and signal voltages shifted up 2.0V for AC bench test purposes.
2. AC measurements are for single-ended operation of the device ($\overline{D}_n = V_{BB}$)

AC TEST CIRCUIT



NOTES:
1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a 2 High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

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ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100117

Triple 1–2–2 Input OR–AND/ OR–AND–INVERT Gate

FEATURES

- **Typical propagation delay: 1.4ns for the data inputs, 0.75ns for the Enable Inputs**
- **Typical supply current ($-I_{EE}$): 57mA**

DESCRIPTION

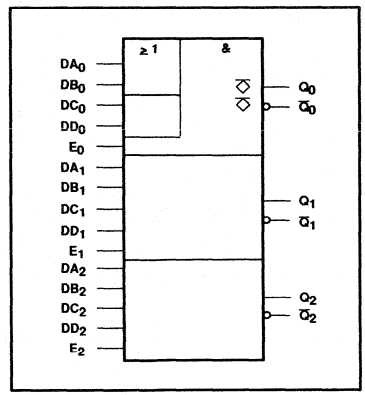
The 100117 has three OR/AND gates with True and Complementary outputs.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$DA_0 - DA_2$, $DB_0 - DB_2$, $DC_0 - DC_2$, $DD_0 - DD_2$	Data Inputs
$E_0 - E_2$	Enable Inputs
$Q_0 - Q_2$	True Data Outputs
$\overline{Q}_0 - \overline{Q}_2$	Complementary Data Outputs

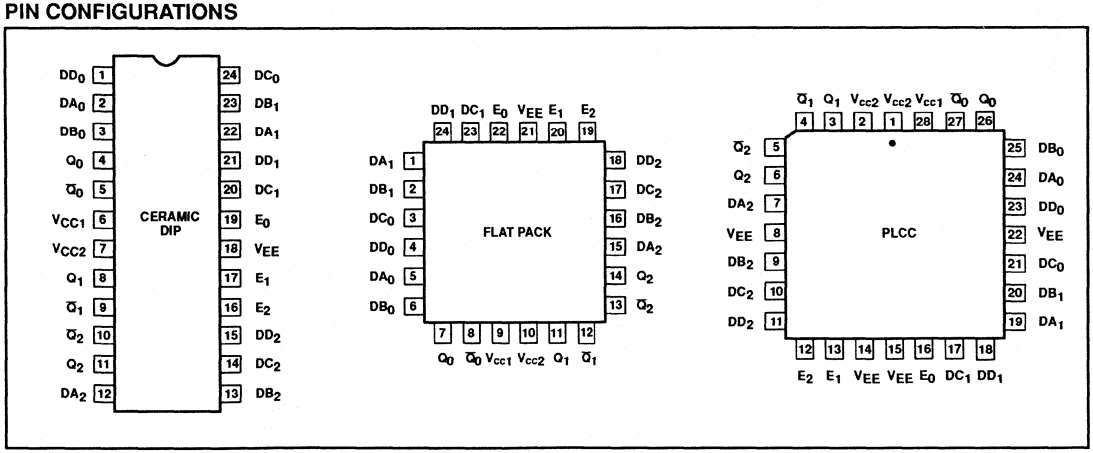
IEC/IEEE SYMBOL



ORDERING INFORMATION

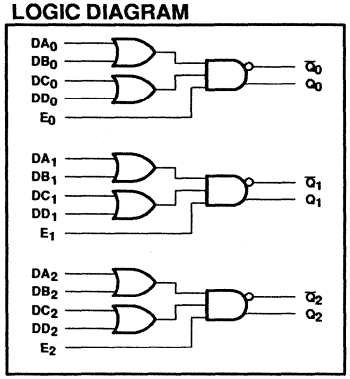
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100117F
24–Pin Ceramic Flat Pack	100117Y
28–Pin PLCC	100117A

PIN CONFIGURATIONS



Gate | 100117

LOGIC DIAGRAM

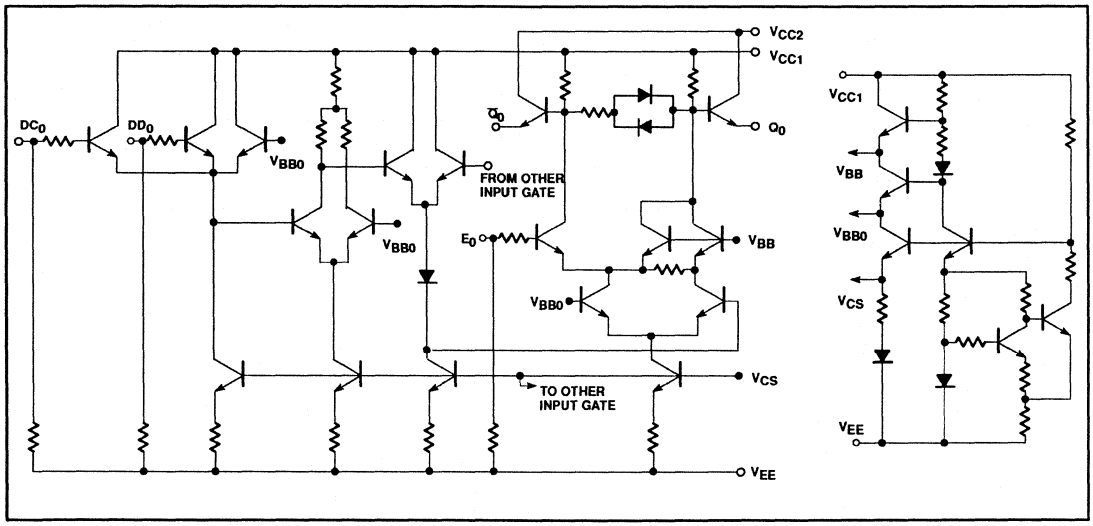


FUNCTION TABLE

INPUTS					OUTPUTS	
E_n	DA_n	DB_n	DC_n	DD_n	Q_n	$\overline{Q}_n$
L	X	X	X	X	L	H
X	X	X	L	L	L	H
X	L	L	X	X	L	H
H	H	X	H	X	H	L
H	X	H	X	H	H	L
H	X	H	H	X	H	L
H	H	X	X	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					260	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}.			37	57	79	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n, DC_n, DD_n, to Q_n, $\overline{Q}_n$	Waveform 1	0.90 0.90	2.60 2.60	0.90 0.90	2.50 2.50	0.90 0.90	2.60 2.60	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to Q_n, $\overline{Q}_n$		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n, DC_n, DD_n, to Q_n, $\overline{Q}_n$	Waveform 1	0.90 0.90	2.60 2.60	0.90 0.90	2.50 2.50	0.90 0.90	2.60 2.60	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to Q_n, $\overline{Q}_n$		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n, DC_n, DD_n, to Q_n, $\overline{Q}_n$	Waveform 1	0.90 0.90	2.40 2.40	0.90 0.90	2.30 2.30	0.90 0.90	2.40 2.40	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

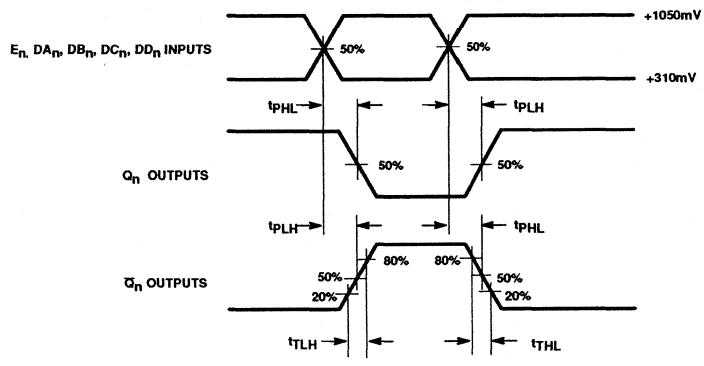
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n, DC_n, DD_n, to Q_n, $\overline{Q}_n$	Waveform 1	0.90 0.90	2.40 2.40	0.90 0.90	2.30 2.30	0.90 0.90	2.40 2.40	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$		0.45 0.45	1.20 1.20	0.45 0.45	1.10 1.10	0.45 0.45	1.20 1.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–0611
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100118

Quint 2–4–4–4–5 Input OR–AND Gate

FEATURES

- **Typical propagation delay: 1.15ns**
- **Typical supply current ($-I_{EE}$): 43mA**

DESCRIPTION

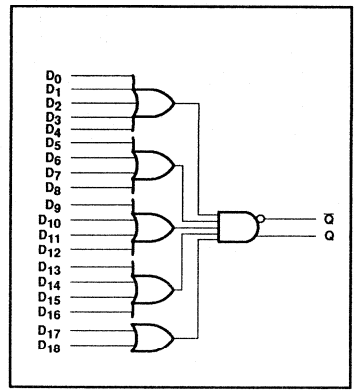
The 100118 is a 2–4–4–4–5 input OR–AND gate with a True and a Complementary Output.

All unused inputs can be left open due to integrated pull–down resistors.

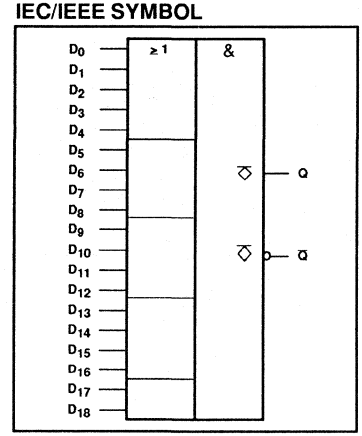
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_{18}$	Data Inputs
Q	True Data Output
$\overline{Q}$	Complementary Data Output

LOGIC DIAGRAM



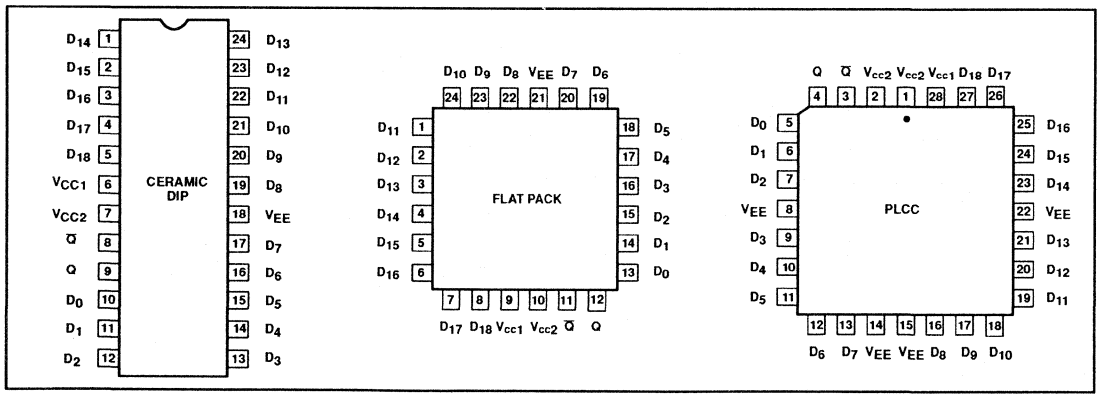
IEC/IEEE SYMBOL



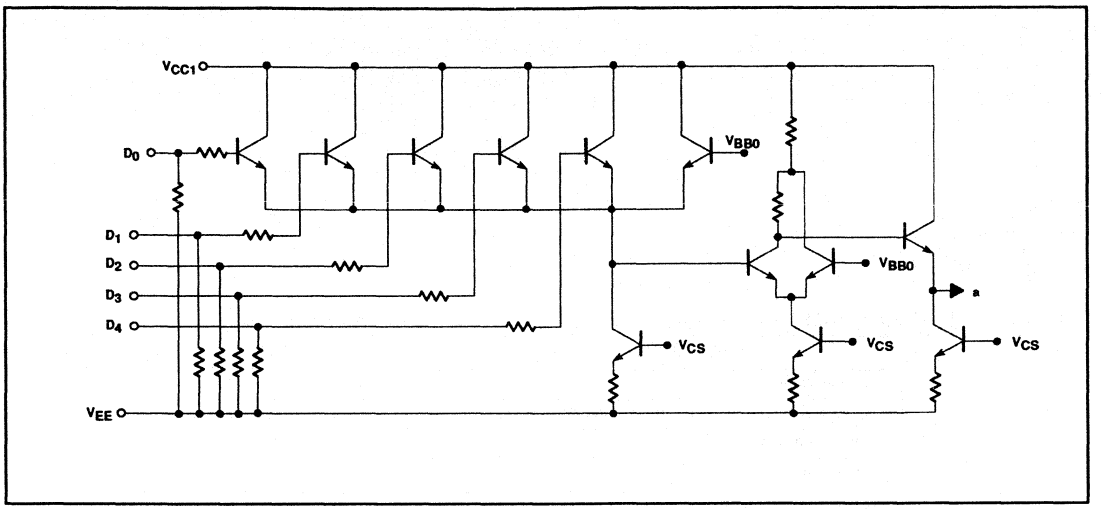
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100118F
24–Pin Ceramic Flat Pack	100118Y
28–Pin PLCC	100118A

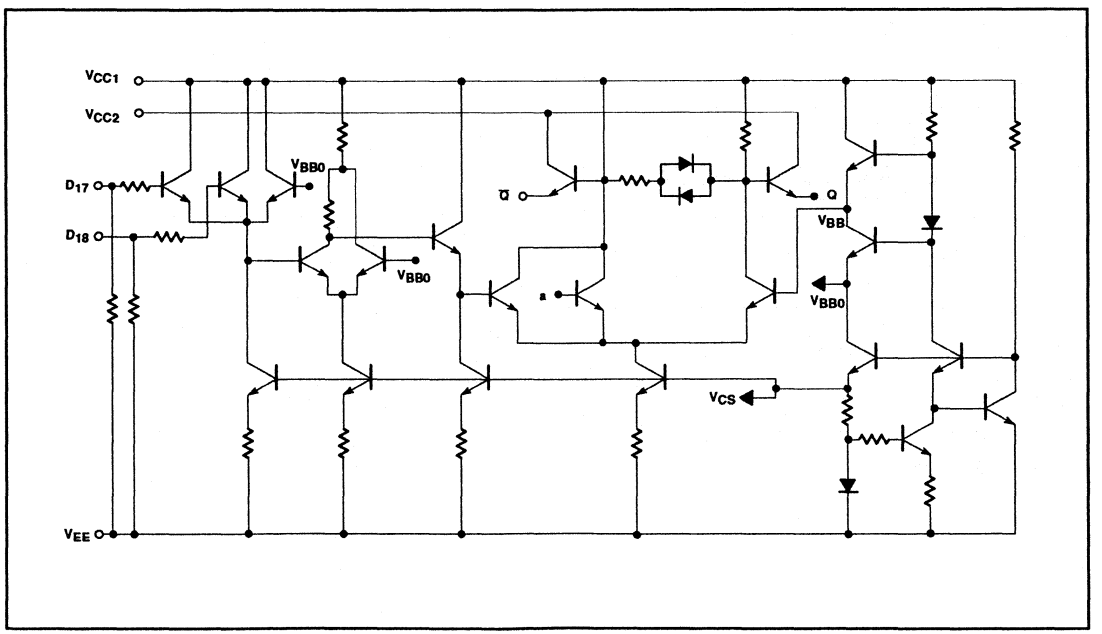
PIN CONFIGURATIONS



SIMPLIFIED SCHEMATIC FOR OR GATE



SIMPLIFIED SCHEMATIC FOR AND GATE



FUNCTION TABLE

INPUTS																		OUTPUTS	
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	D_{16}	D_{17}	D_{18}	$\overline{Q}$	Q
L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L
X	X	X	X	X	L	L	L	L	X	X	X	X	X	X	X	X	X	X	H	L
X	X	X	X	X	X	X	X	X	L	L	L	L	X	X	X	X	X	X	H	L
X	X	X	X	X	X	X	X	X	X	X	X	X	L	L	L	L	X	X	H	L
X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	L	L	H	L
all other combinations																			L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, $T_A = 0°C$ to $+85°C$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	$V_{EE} = -4.2V$	–1150		–880	mV
		$V_{EE} = -4.5V$	–1165			
		$V_{EE} = -4.8V$	–1165			
V_{IL}	Low level input voltage	$V_{EE} = -4.2V$	–1810		–1475	mV
		$V_{EE} = -4.5V$			–1475	mV
		$V_{EE} = -4.8V$			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}, other inputs at V_{ILMIN}.					350	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}, other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}.			32	43	92	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C MIN.	LIMITS T_A = 0°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to Q, $\overline{Q}$	Waveform 1	0.85 0.85	3.20 3.20	0.85 0.85	3.20 3.20	0.85 0.85	3.40 3.40	ns ns
t_{TLH} t_{THL}	Transition time Q, $\overline{Q}$		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q, $\overline{Q}$	Waveform 1	0.85 0.85	3.20 3.20	0.85 0.85	3.20 3.20	0.85 0.85	3.40 3.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -4.8V \text{ to } -4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q, $\overline{Q}$	Waveform 1	0.85 0.85	3.00 3.00	0.85 0.85	3.00 3.00	0.85 0.85	3.20 3.20	ns ns
t_{TLH} t_{THL}	Transition time Q, $\overline{Q}$		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

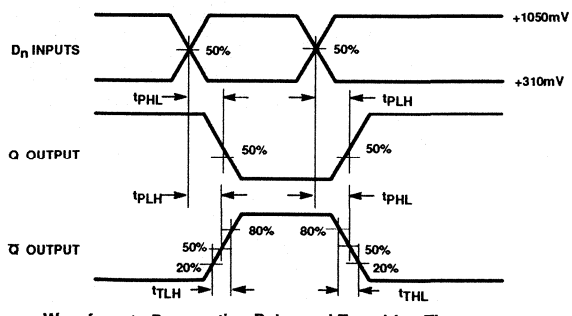
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q, $\overline{Q}$	Waveform 1	0.85 0.85	3.00 3.00	0.85 0.85	3.00 3.00	0.85 0.85	3.20 3.20	ns ns
t_{TLH} t_{THL}	Transition time Q, $\overline{Q}$		0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–0612
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100122

9–Bit Buffer

FEATURES

- **Typical propagation delay: 0.75ns**
- **Typical supply current ($-I_{EE}$): 78mA**

DESCRIPTION

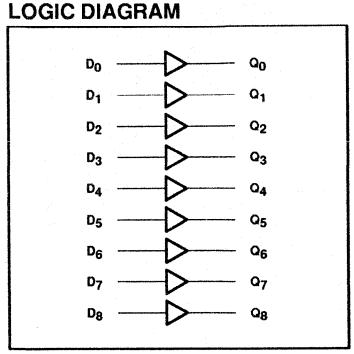
The 100122 contains 9 Buffer Gates, each with a single input and a single output.

All unused inputs can be left open due to integrated pull–down resistors.

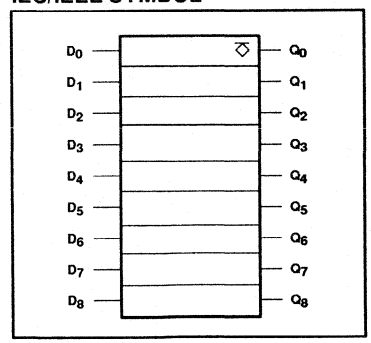
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_8$	Data Inputs
$Q_0 - Q_8$	Data Outputs

LOGIC DIAGRAM



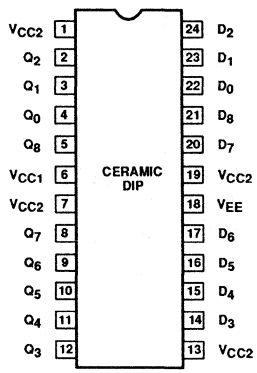
IEC/IEEE SYMBOL

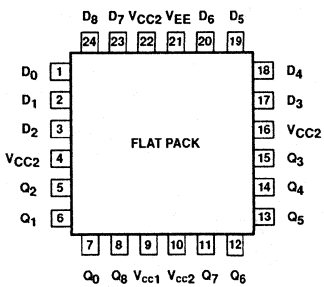


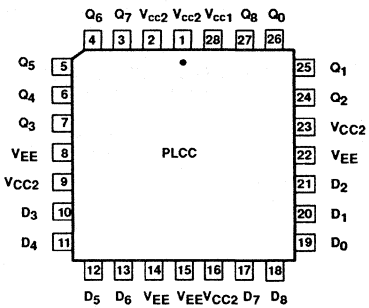
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100122F
24–Pin Ceramic Flat Pack	100122Y
28–Pin PLCC	100122A

PIN CONFIGURATIONS

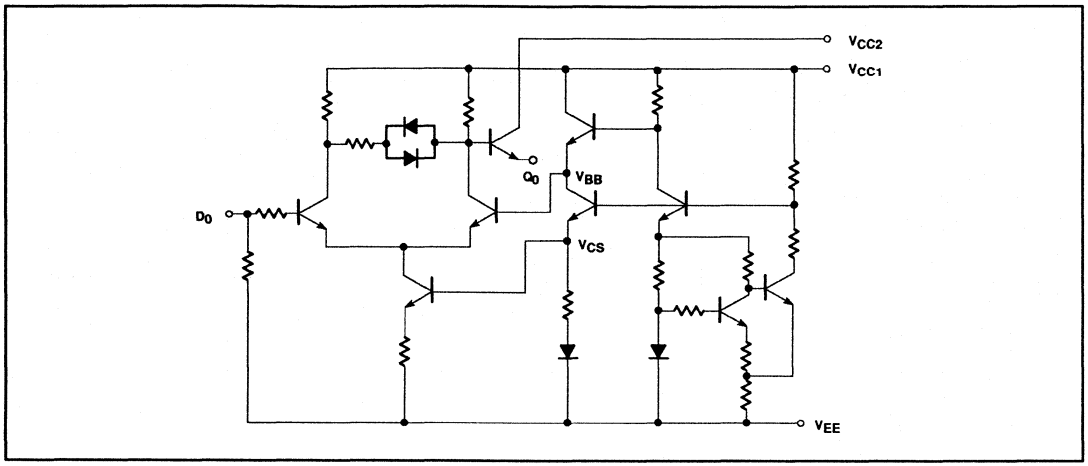






Buffer 100122

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}, other inputs at V_{ILMIN}.					350	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}, other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}.			46	78	96	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C MIN.	LIMITS T_A = 0°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH}	Propagation delay	Waveform 1	0.45	1.60	0.45	1.45	0.45	1.60	ns
t_{PHL}	D_n to Q_n		0.45	1.60	0.45	1.45	0.45	1.60	ns
t_{TLH}	Transition time Q_n		0.45	1.40	0.45	1.30	0.45	1.30	ns
t_{THL}			0.45	1.40	0.45	1.30	0.45	1.30	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	0.45 0.45	1.60 1.60	0.45 0.45	1.45 1.45	0.45 0.45	1.60 1.60	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.30 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.25 1.25	0.45 0.45	1.40 1.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.30 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

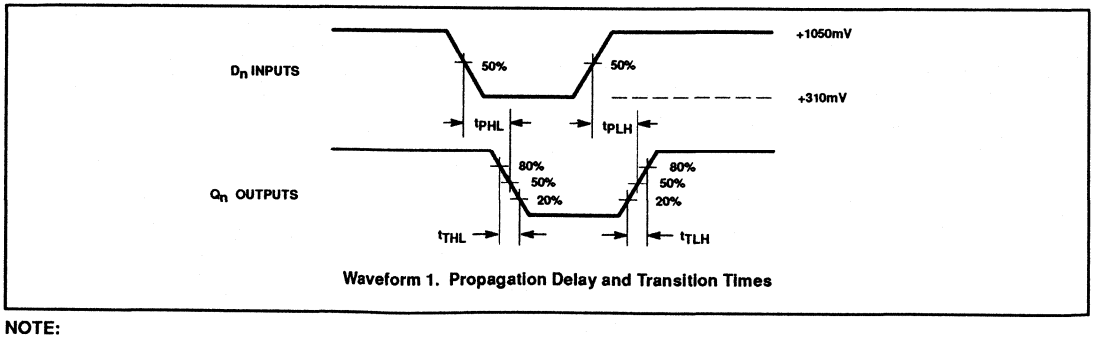
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.25 1.25	0.45 0.45	1.40 1.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.30 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–0613
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100123

Bus Driver

FEATURES

- **Typical propagation delay: 2.5 ns**
- **Typical supply current ($-I_{EE}$): 176mA**
- **Low logic level of output doubles as a high impedance state.**
- **Output drives 25Ω loads**

DESCRIPTION

The 100123 contains six bus drivers capable of driving a load as Low as 25Ω. Each output has its respective ground connection; this reduces crosstalk. The driver has an AND–OR configuration. The Low level output voltage is more negative than for usual ECL outputs.

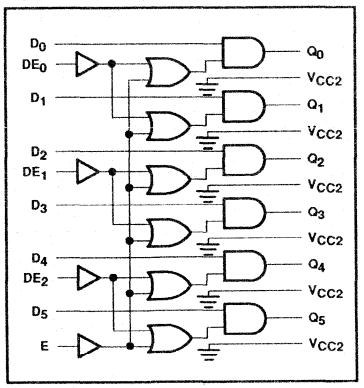
When the output goes Low, its emitter–follower turns Off. As a result, the Low logic level approaches the termination voltage (–2.0V) and represents a high impedance state.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
E	Common Enable Input
$DE_0 - DE_2$	Dual Enable Inputs
$Q_0 - Q_5$	Data Outputs

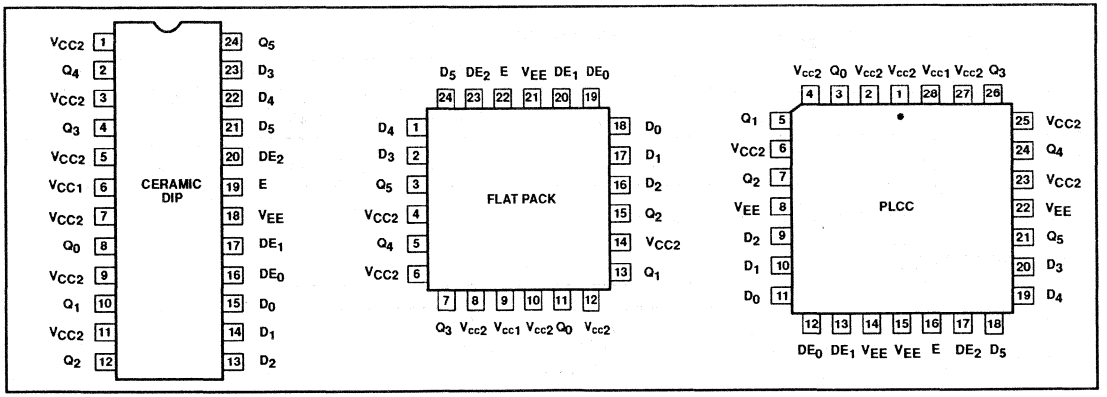
LOGIC DIAGRAM



ORDERING INFORMATION

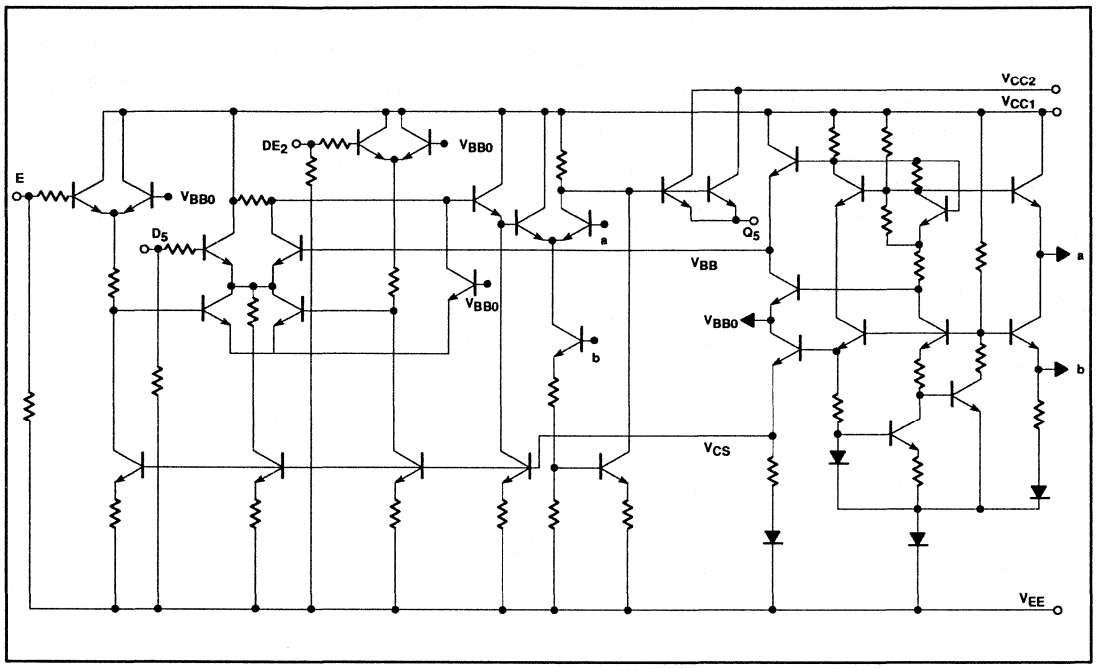
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100123F
24–Pin Ceramic Flat Pack	100123Y
28–Pin PLCC	100123A

PIN CONFIGURATIONS



Bus Driver 100123

SIMPLIFIED SCHEMATIC



FUNCTION TABLE (One Gate)

INPUTS			OUTPUT
E	DE_0	D_0	Q_0
X	X	L	L
L	L	X	L
H	X	H	H
X	H	H	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–100	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

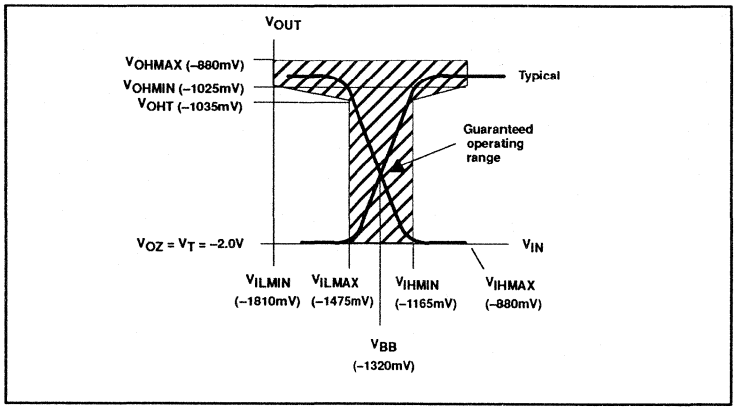
DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs Loaded with 25Ω to V_T = –2.0V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OZ}[5]	Low level output voltage		Outputs loaded with 25Ω to V_T = –2.3V	Inputs at V_{IHMIN} or V_{ILMAX}.	V_{EE} = –4.2V	V_T		–2200	mV
					V_{EE} = –4.5V	V_T		–2200	mV
					V_{EE} = –4.8V	V_T		–2200	mV
I_{IH}	High level input current	E	One input under test at V_{IHMAX}.					330	µA
		D_n, DE_n	Other inputs at V_{ILMIN}.					260	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}.			113	176	235	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.
5. The level of V_{OZ} is determined by the termination power supply (V_T = –2.3V) in combination with any leakage of the output circuit.

TRANSFER CHARACTERISTICS



AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.70 1.00	4.35 2.40	1.75 1.00	4.35 2.40	1.75 1.10	4.65 2.60	ns ns
t_{PLH} t_{PHL}	Propagation delay DE_n to Q_n		2.00 1.20	4.70 3.00	2.00 1.20	4.70 3.00	2.00 1.20	5.10 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		2.10 1.20	5.40 3.30	2.10 1.20	5.30 3.30	2.10 1.20	5.80 3.70	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.70 0.45	2.00 1.30	0.70 0.45	1.90 1.20	0.70 0.45	2.10 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.70 1.00	4.35 2.40	1.75 1.00	4.35 2.40	1.75 1.10	4.65 2.60	ns ns
t_{PLH} t_{PHL}	Propagation delay DE_n to Q_n		2.00 1.20	4.70 3.00	2.00 1.20	4.70 3.00	2.00 1.20	5.10 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		2.10 1.20	5.40 3.30	2.10 1.20	5.30 3.30	2.10 1.20	5.80 3.70	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.70 0.45	2.00 1.30	0.70 0.45	1.90 1.20	0.70 0.45	2.10 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.70 1.00	4.15 2.20	1.75 1.00	4.15 2.20	1.75 1.10	4.45 2.40	ns ns
t_{PLH} t_{PHL}	Propagation delay DE_n to Q_n		2.00 1.20	4.50 2.80	2.00 1.20	4.50 2.80	2.00 1.20	4.90 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		2.10 1.20	5.20 3.10	2.10 1.20	5.10 3.10	2.10 1.20	5.60 3.50	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.70 0.45	2.00 1.30	0.70 0.45	1.90 1.20	0.70 0.45	2.10 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

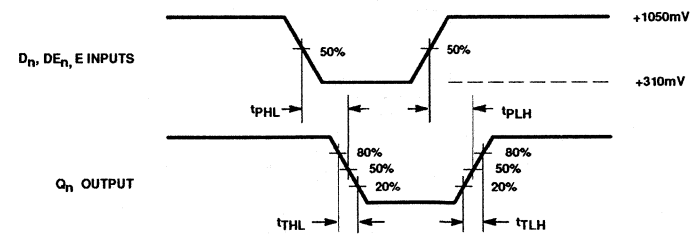
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.70 1.00	4.15 2.20	1.75 1.00	4.15 2.20	1.75 1.10	4.45 2.40	ns ns
t_{PLH} t_{PHL}	Propagation delay DE_n to Q_n		2.00 1.20	4.50 2.80	2.00 1.20	4.50 2.80	2.00 1.20	4.90 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		2.10 1.20	5.20 3.10	2.10 1.20	5.10 3.10	2.10 1.20	5.60 3.50	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.70 0.45	2.00 1.30	0.70 0.45	1.90 1.20	0.70 0.45	2.10 1.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

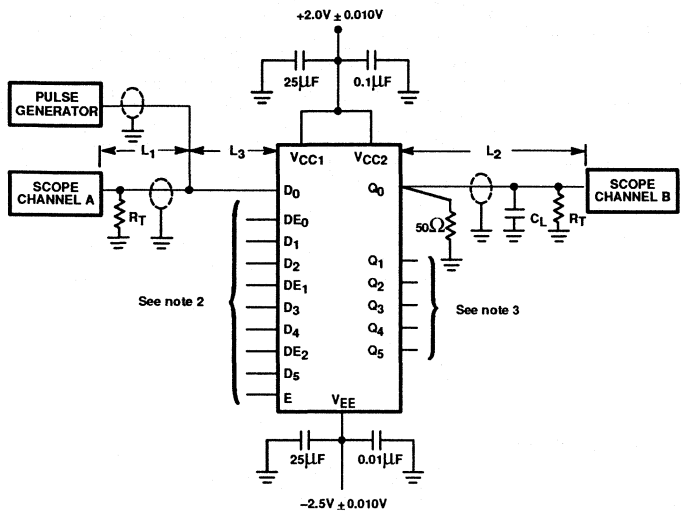
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

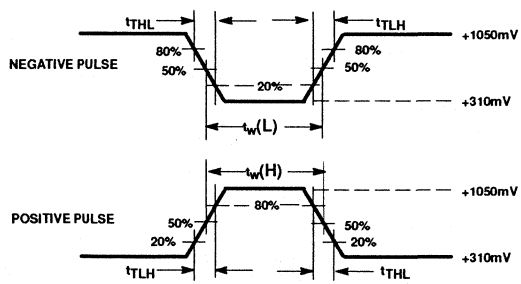
AC TEST CIRCUIT



NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.8V$ to $-2.2V$, $V_T = 0V$ (system ground)				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
100K ECL	740mV$_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–1440
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100124/100124A

Hex TTL–to–ECL Translator

FEATURES

- **Typical propagation delay: 1.70ns**
- **Typical ECL supply current ($-I_{EE}$): 96mA for the 100124 and 71mA for the 100124A**
- **Typical TTL supply current (I_{TTL}): 44mA for the 100124 and 10mA for the 100124A**

DESCRIPTION

The 100124 is a hex translator that converts TTL logic levels to 100K ECL logic levels. When the common Enable (E) is Low, all true outputs are Low, and all inverting outputs are High. The differential outputs allow each circuit to be used as an inverting, noninverting, or differential line driver.

In differential operation, common mode rejection helps overcome ground offsets and transients between the 100124 and its receiver. V_{EE} and V_{TTL} may be applied in any order.

The 100124A is a low power version of the 100124. The only difference between the two parts are the limits of the ECL and TTL supply currents.

All unused inputs can be left open due to integrated pull–down resistors.

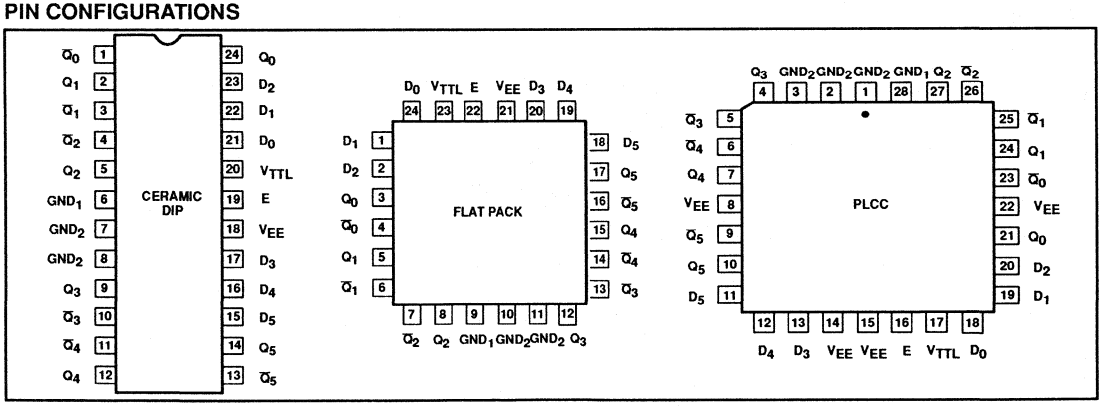
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs (TTL compatible)
E	Enable input (TTL compatible)
$Q_0 - Q_5$	True data outputs (100K ECL compatible)
$\overline{Q}_0 - \overline{Q}_5$	Complementary data outputs (100K ECL compatible)

ORDERING INFORMATION

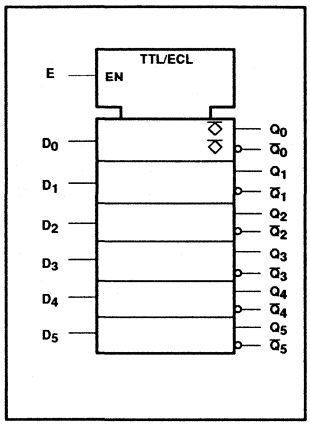
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100124F/100124AF
24–Pin Ceramic Flat Pack	100124Y/100124AY
28–Pin PLCC	100124A/100124AA

PIN CONFIGURATIONS

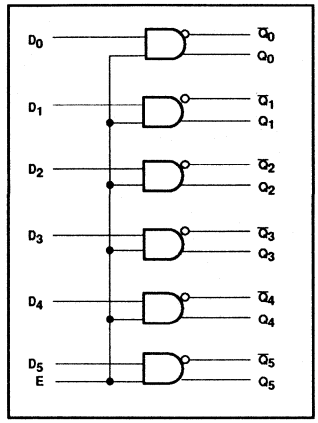


Translator 100124/100124A

IEC/IEEE SYMBOL



LOGIC DIAGRAM

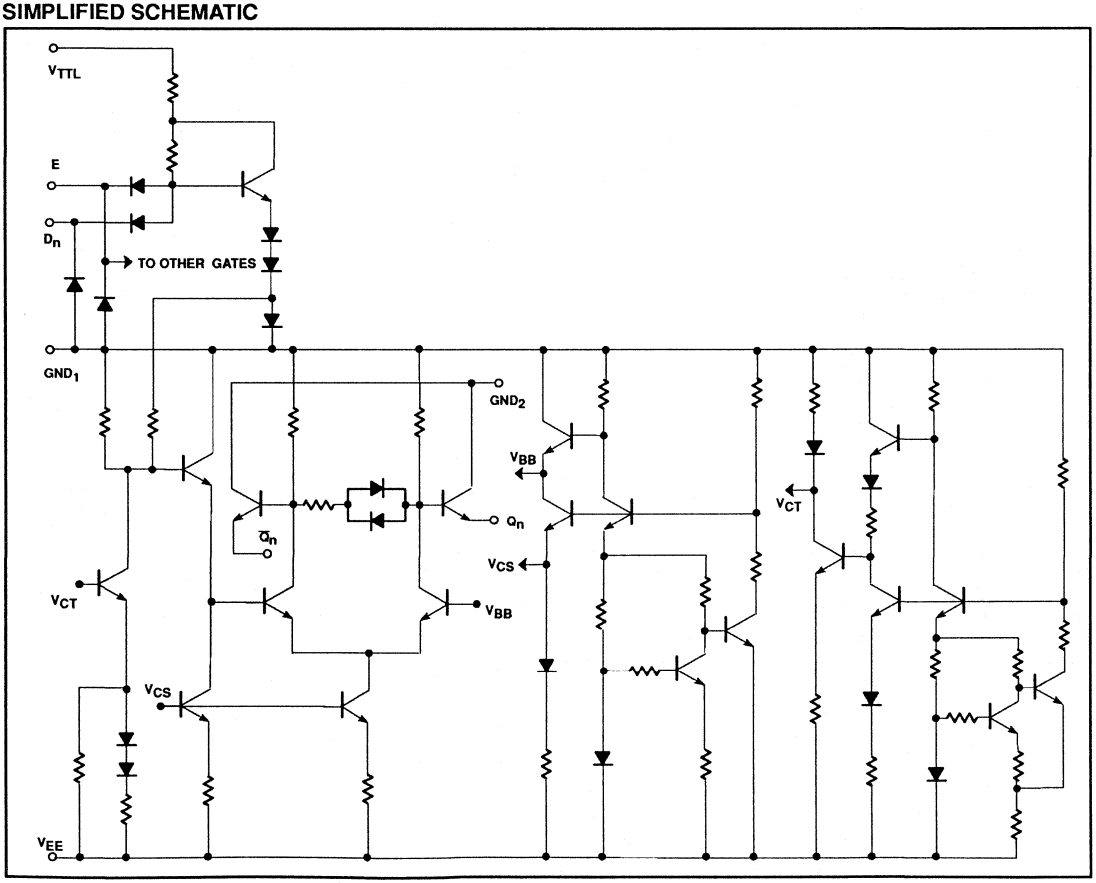


FUNCTION TABLE (One Gate)

INPUTS		OUTPUTS	
E	D_n	Q_n	$\overline{Q}_n$
H	H	H	L
H	L	L	H
L	X	L	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

GND_1 = GND_2 = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{TTL}	TTL Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to V_{TTL}	V
I_{IN}	Input current	–30 to +5.0	mA
V_{EE}	ECL Supply voltage	–7.0 to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	NOM.	MAX.	
GND_1, GND_2	Circuit ground	0	0	0	V
V_{TTL}	TTL Supply voltage	+4.5	+5.0	+5.5	V
V_{EE}	ECL Supply voltage	–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family	–5.7			V
V_{IH}	High level input voltage	+2.0			V
V_{IL}	Low level input voltage			+0.8	V
T_A	Operating ambient temperature range	0	+25	+85	°C

NOTE:
When operating at other than the V_{EE} specified voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

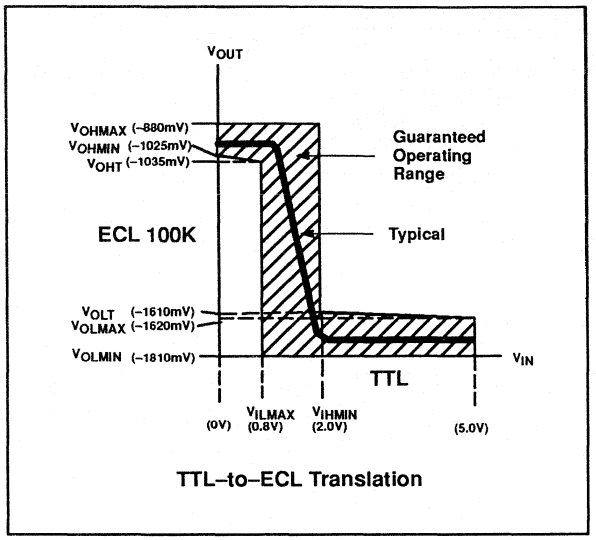
$GND_1 = GND_2$ = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs Loaded with 50Ω to –2.0V ±0.010V	E, D_n = 2.4V, test Q_n	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			E, D_n = 2.0V, test Q_n	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			E, D_n = 0.8V, test Q_n	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			E, D_n = 0.4V, test Q_n	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
$-I_{EE}$	V_{EE} supply current	100124	All inputs ≥ V_{IHMIN}				96	140	mA
		100124A					71	90	mA
V_{IK}	Input clamp voltage	D_n inputs	Apply –18mA to one D_n, other inputs open.			–1.5			V
		E input	Apply –18mA to one E, other inputs open.			–1.5			V
I_I	Input current at maximum input voltage	D_n inputs	D_n input under test =+5.5V, other inputs = ground.					1.0	mA
		E input	E = +5.5V, other inputs = ground.					1.0	mA
I_{IH}	High level input current	D_n inputs	D_n input under test =+2.4V, other inputs = ground.					20	uA
		E input	E = +2.4V, other inputs = ground.					120	µA
$-I_{IL}$	Low level input current	D_n inputs	D_n input under test =+0.4V, other inputs = +2.4V.					1.6	mA
		E input	E = +0.4V, other inputs = +2.4V.					9.6	mA
I_{TTL}	TTL supply current	100124	All inputs at ground.				44	75	mA
		100124A					10	15	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

TRANSFER CHARACTERISTICS



TTL–to–ECL Translation

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $GND_1 = GND_2$ = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{E}$ to Q_n or $\overline{Q}_n$	Waveform 1	0.50 0.50	3.00 3.00	0.50 0.50	2.90 2.90	0.50 0.50	3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $GND_1 = GND_2$ = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{E}$ to Q_n or $\overline{Q}_n$	Waveform 1	0.50 0.50	3.00 3.00	0.50 0.50	2.90 2.90	0.50 0.50	3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $GND_1 = GND_2$ = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{E}$ to Q_n or $\overline{Q}_n$	Waveform 1	0.50 0.50	2.80 2.80	0.50 0.50	2.70 2.70	0.50 0.50	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

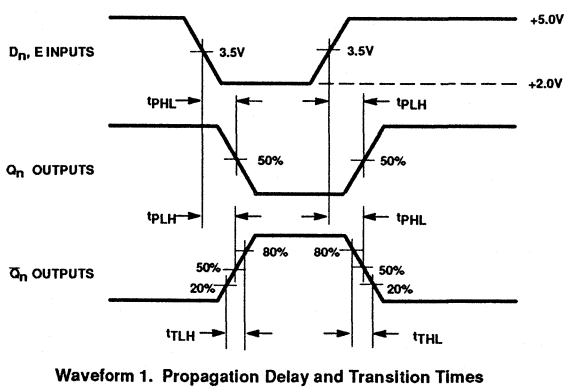
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $GND_1 = GND_2$ = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{E}$ to Q_n or $\overline{Q}_n$	Waveform 1	0.50 0.50	2.80 2.80	0.50 0.50	2.70 2.70	0.50 0.50	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$		0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS

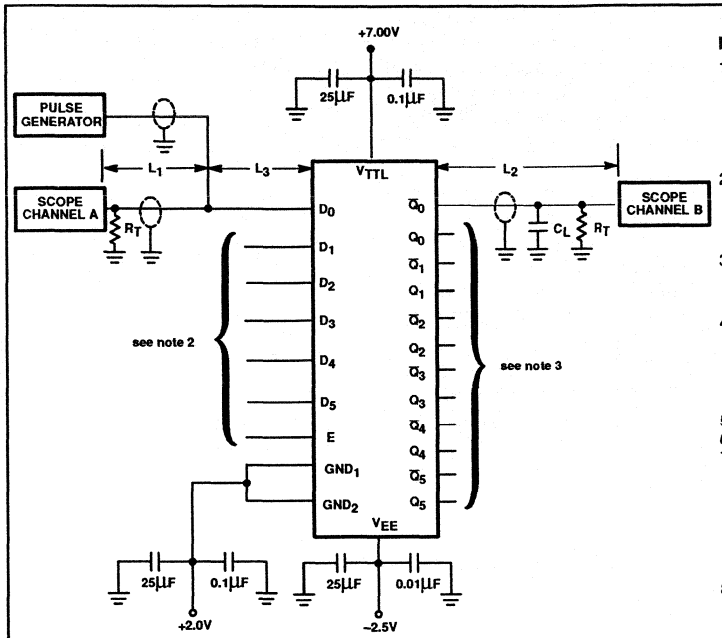


Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Translator | 100124/100124A

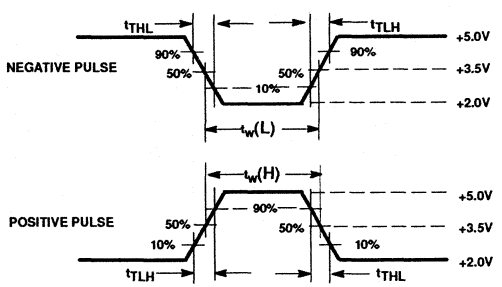
AC TEST CIRCUIT



NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead length should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded with 50Ω to ground. The tolerance of all resistors should be ± 1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance = $C_L \leq$ 3pF.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS GND1 = GND2 = +2.0V ± 0.010V, V_{EE} = −2.8V to −2.2V, V_{TTL} = +6.5V to +7.5V, V_T = 0V (system ground)				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
TTL	$3.0V_{p-p}$	1MHz	500ns	2.5 ± 0.2ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–1441
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100125

Hex ECL–to–TTL Translator

FEATURES

- **Typical propagation delay: 2.2ns**
- **Typical ECL supply current ($-I_{EE}$): 65mA**
- **Typical TTL supply current (I_{TTL}): 75mA**

DESCRIPTION

The 100125 is a hex translator that converts ECL logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non–inverting, or differential receiver. An internal reference voltage generator provides V_{BB} for single–ended operation or for use in Schmitt trigger applications.

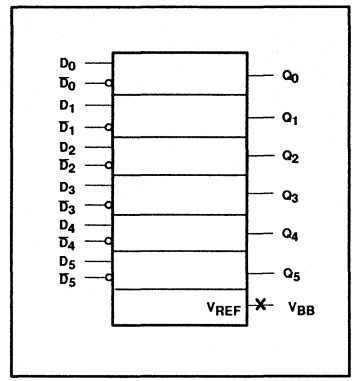
When used in the differential mode, common mode rejection makes this device tolerant of ground offsets and transients between the signal source and the translator. The 100125 outputs are designed to go to a low logic level whenever both inputs are left open or tied to V_{EE}. The V_{EE} and V_{TTL} power may be applied in any order.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	True data Inputs (100K ECL compatible)
$\overline{D}_0 - \overline{D}_5$	Complementary data inputs (100K ECL compatible)
V_{BB}	Reference voltage output (100K ECL compatible)
$Q_0 - Q_5$	Data outputs (TTL compatible)

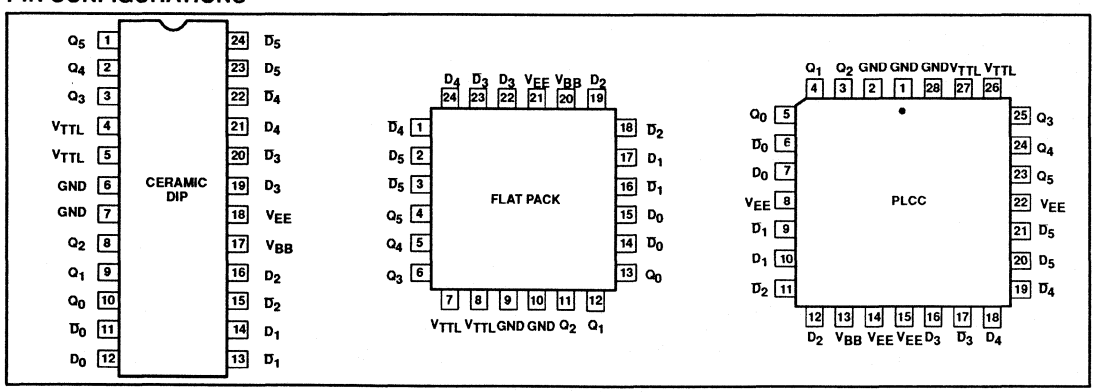
IEC/IEEE



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100125F
24–Pin Ceramic Flat Pack	100125Y
28–Pin PLCC	100125A

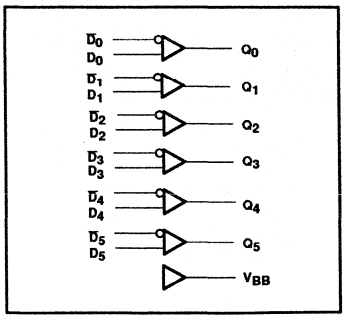
PIN CONFIGURATIONS



Translator

100125

LOGIC DIAGRAM

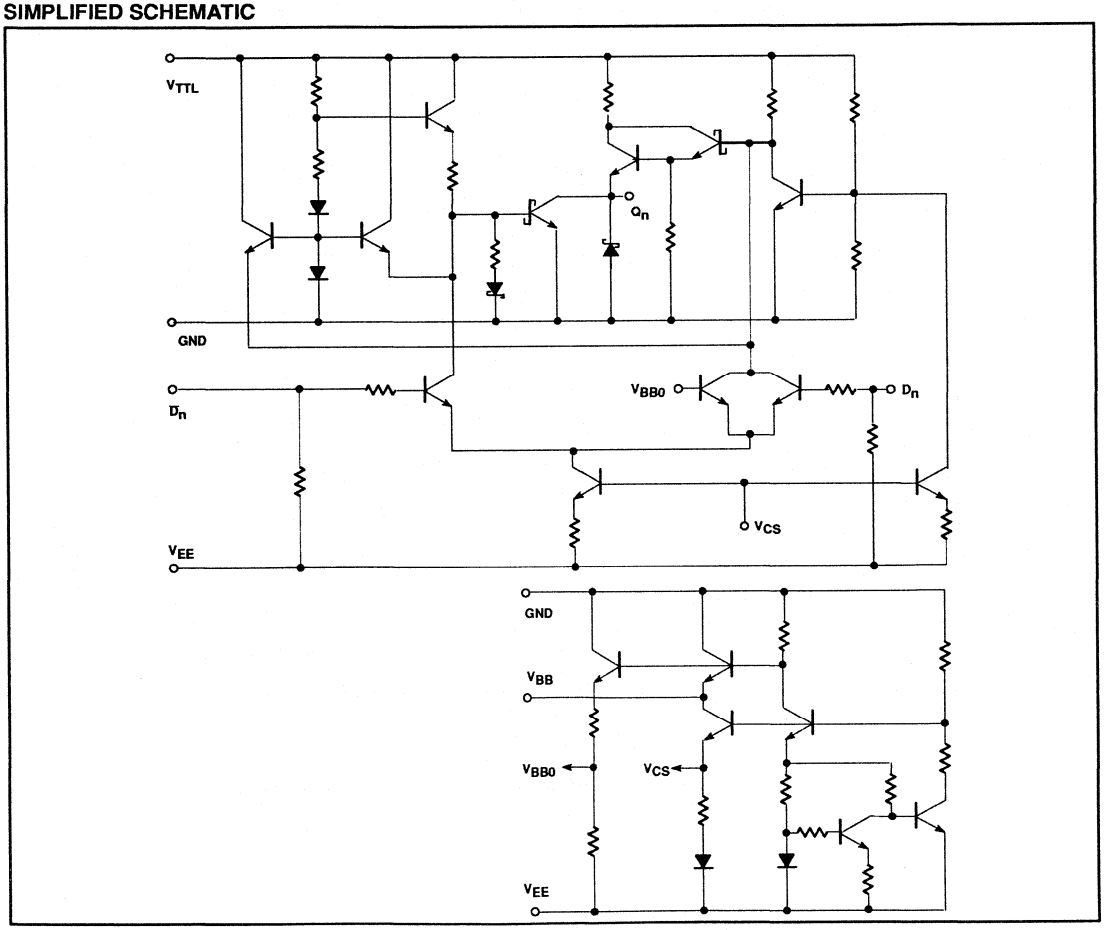


FUNCTION TABLE

INPUTS		OUTPUTS
D_n	$\overline{D}_n$	Q_0
L	H	L
H	L	H
L	L	U
H	H	U
open	open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

NOTES:
H = High voltage level
L = Low voltage level
U = Undefined level

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS GND = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	ECL Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
V_{TTL}	Output source current (continuous)	–0.5V to +7.0	V
V_{OUT}	Voltage applied to output in high state	–0.5V to V_{TTL}	V
I_O	Output source (continuous)	–40	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
GND	Circuit ground		0	0	0	V
V_{TTL}	TTL supply voltage		+4.5	+5.0	+5.5	V
V_{EE}	ECL supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	ECL supply voltage when operating with the 10K or the 10KH ECL family.		–5.7			V
V_{IH}[2]	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}[2]	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
V_{CM}[3]	Common mode voltage	V_{EE} = –4.2V			1.0	V
		V_{EE} = –4.5V	0			
		V_{EE} = –4.8V				
V_{DIFF}[4]	Differential input voltage	V_{EE} = –4.2V				V
		V_{EE} = –4.5V	150			
		V_{EE} = –4.8V				
$-I_{OH}$	High level output current				2.0	mA
I_{OL}	Low level output current				20	mA
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTES:
1. When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.
2. For input voltages outside the specified V_{IH} and V_{IL} ranges, the output voltage specifications will hold true. However, the AC performance will be according to specification only if two conditions are met: First, D_n or $\overline{D}_n$ must be above –2300mV at all times. Second, both D_n and $\overline{D}_n$ must be below –230mV.
3. V_{CM} is added or subtracted with respect to V_{BB}. For common–mode applications, the total voltage applied to D_n or $\overline{D}_n$ should be no less than V_{BB}–V_{CM}(max) and no greater than V_{BB} + V_{CM}(max).
4. V_{DIFF}(min) is the minimum voltage difference by which D_n must exceed $\overline{D}_n$ such that the output Q_n will assume a defined logic level(Low or High).

DC ELECTRICAL CHARACTERISTICS

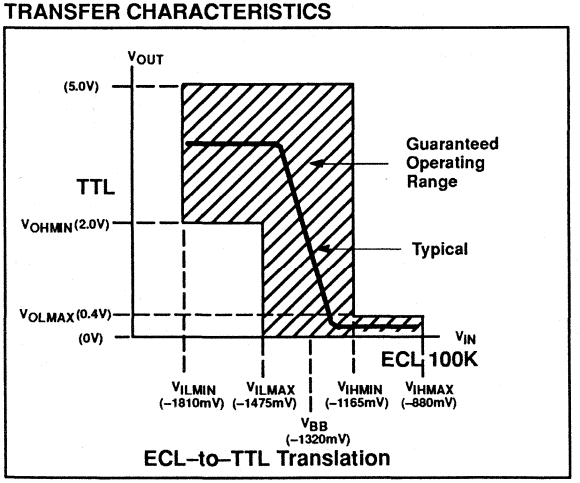
GND = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	All D_n = V_{IHMIN}, all $\overline{D}_n$ connected to V_{BB} pin. I_{OH} = –2.0 mA		2.5	3.4		V
V_{OL}	Low level output voltage	All D_n = V_{ILMAX}, all $\overline{D}_n$ connected to V_{BB} pin. I_{OL} = +20 mA			0.35	0.5	V
V_{OS1}	Indeterminate input protection test	All D_n = all $\overline{D}_n$ = V_{EE}. I_{OL} = +20 mA				0.5	V
V_{OS2}	Indeterminate input protection test	All D_n and all $\overline{D}_n$ open. I_{OL} = +20 mA				0.5	V
V_{BB}	Reference output voltage	V_{EE} = –4.5V	All D_n open, all $\overline{D}_n$ connected to V_{BB} pin.	–1380	–1320	–1260	mV
		V_{EE} = –4.8V to –4.2V		–1396	–1320	–1244	mV
I_{IH}	High level input current	One D_n input under test at V_{IHMAX}, all other D_n inputs at V_{ILMIN}. All $\overline{D}_n$ inputs connected to V_{BB} pin.				350	µA
I_{IL}	Low level Input current	One D_n input under test at V_{ILMIN}, all other D_n inputs at V_{IHMAX}. All $\overline{D}_n$ inputs connected to V_{BB} pin.		0.5			µA
$-I_{EE}$	V_{EE} supply current	All D_n at V_{IHMAX}. All $\overline{D}_n$ at V_{BB}.		40	65	85	mA
$-I_{OS}$	Short circuit current[4]	All D_n connected to V_{BB} pin. All $\overline{D}_n$ inputs at V_{ILMIN}. One Q_n under test at ground, V_{TTL} = 5.5V.		–40		100	mA
I_{TTLH}	V_{TTL} supply current outputs High	All D_n connected to V_{BB} pin. All $\overline{D}_n$ inputs at V_{ILMIN}. V_{TTL} = 5.5V.			70	100	mA
I_{TTLL}	V_{TTL} supply current outputs Low	All D_n connected to V_{BB} pin. All $\overline{D}_n$ inputs at V_{IHMAX}. V_{TTL} = 5.5V.			80	115	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. Not more than one output should be shorted at a time. The other outputs should not be loaded. For testing I_{OS}, the use of a high–speed test apparatus and/or sample–and–hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

TRANSFER CHARACTERISTICS



ECL–to–TTL Translation

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP GND = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{D}_n$ to Q_n	Waveform 1	0.80 0.80	3.50 3.50	0.90 0.90	3.70 3.70	1.00 1.00	4.00 4.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n 1.0V to 2.0V, 2.0V to 1.0V		0.50 0.50	2.60 2.60	0.50 0.50	2.60 2.60	0.50 0.50	2.60 2.60	ns ns

NOTES:
1. For AC test setup information, see AC Testing, Chapter 2, Section 3.
2. This AC data is for a Schottky load. When testing the 100125 with a FAST load, propagation delays may increase as much as 1.5ns.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP GND = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{D}_n$ to Q_n	Waveform 1	0.72 0.72	3.85 3.85	0.81 0.81	4.07 4.07	0.90 0.90	4.40 4.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n 1.0V to 2.0V, 2.0V to 1.0V		0.45 0.45	2.86 2.86	0.45 0.45	2.86 2.86	0.45 0.45	2.86 2.86	ns ns

NOTES:
1. For AC test setup information, see AC Testing, Chapter 2, Section 3.
2. This AC data is for a Schottky load. When testing the 100125 with a FAST load, propagation delays may increase as much as 1.5ns.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC GND = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{D}_n$ to Q_n	Waveform 1	0.80 0.80	3.30 3.30	0.90 0.90	3.50 3.50	1.00 1.00	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n 1.0V to 2.0V, 2.0V to 1.0V		0.50 0.50	2.50 2.50	0.50 0.50	2.50 2.50	0.50 0.50	2.50 2.50	ns ns

NOTES:
1. For AC test setup information, see AC Testing, Chapter 2, Section 3.
2. This AC data is for a Schottky load. When testing the 100125 with a FAST load, propagation delays may increase as much as 1.5ns.

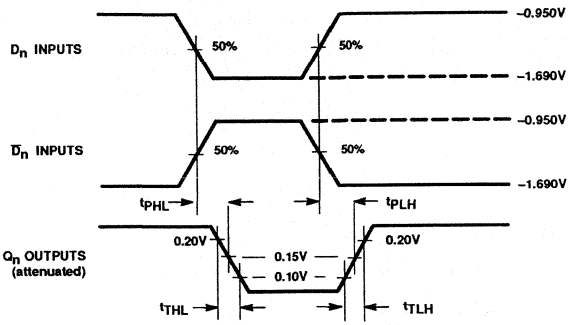
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC GND = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{D}_n$ to Q_n	Waveform 1	0.72 0.72	3.63 3.63	0.81 0.81	3.85 3.85	0.90 0.90	4.18 4.18	ns ns
t_{TLH} t_{THL}	Transition time Q_n 1.0V to 2.0V, 2.0V to 1.0V		0.45 0.45	2.75 2.75	0.45 0.45	2.75 2.75	0.45 0.45	2.75 2.75	ns ns

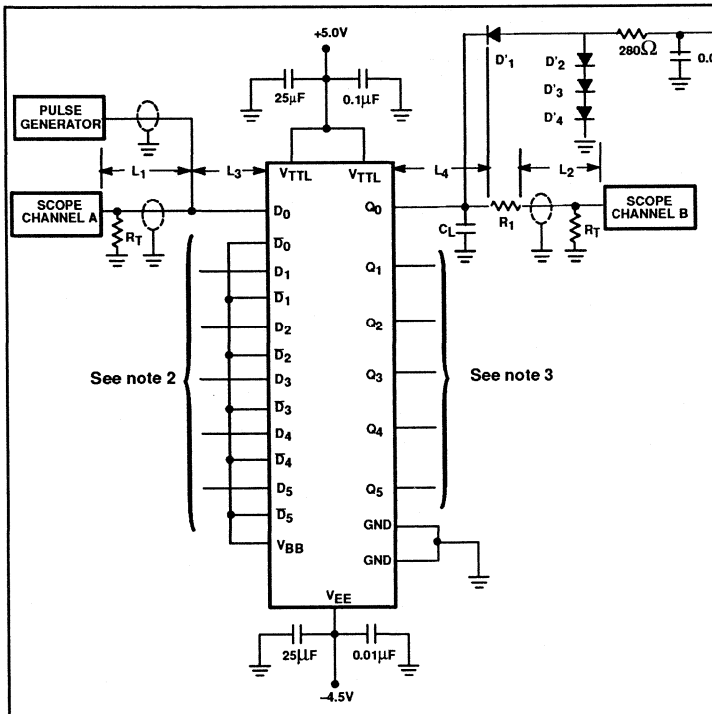
NOTES:
1. For AC test setup information, see AC Testing, Chapter 2, Section 3.
2. This AC data is for a Schottky load. When testing the 100125 with a FAST load, propagation delays may increase as much as 1.5ns.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

AC TEST CIRCUIT

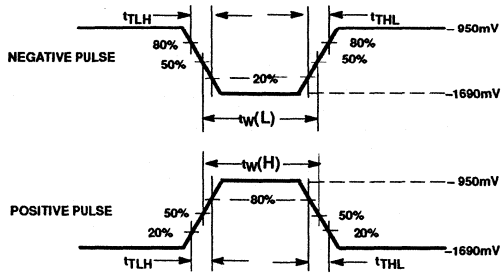


NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ± 1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm). L_4, the lead length from the DUT output pin to R_1 and D_1, should not exceed 1/4 inch.
5. R_T = 50Ω termination internal to scope. R_1 = 450Ω.
6. Fixture and stray capacitance (not including scope cable capacitance) = C_L = 25pF.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).

Translator 100125

ECL INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS
GND = 0V (system ground),
V_{EE} = –4.8V to –4.2V, V_{TTL} = +4.5V to +5.5V

Family	Amplitude	Rep Rate	$t_{W(H)}$, $t_{W(L)}$	t_{TLH}, t_{THL}
100K ECL	740mV_{p-p}	1MHz	500ns	0.7 ± 0.1ns

Document No.	853–0616
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100126

Backplane Driver

FEATURES

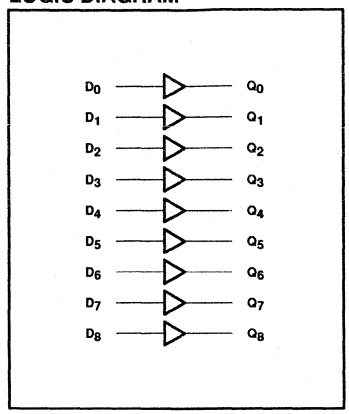
- **Typical propagation delay: 2.0ns**
- **Typical supply current ($-I_{EE}$): 78mA**

DESCRIPTION

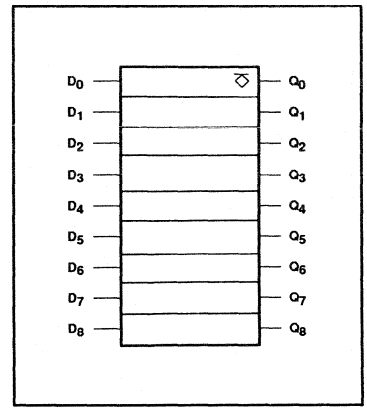
The 100126 contains nine independent, high–speed buffer gates each with a single input and a single output. The gates are non–inverting. These buffers are useful in bus–oriented systems where buffering is desired. The output transition times are slower to minimize noise when used in a backplane environment.

All unused inputs can be left open due to integrated pull–down resistors.

LOGIC DIAGRAM



IEC/IEEE SYMBOL



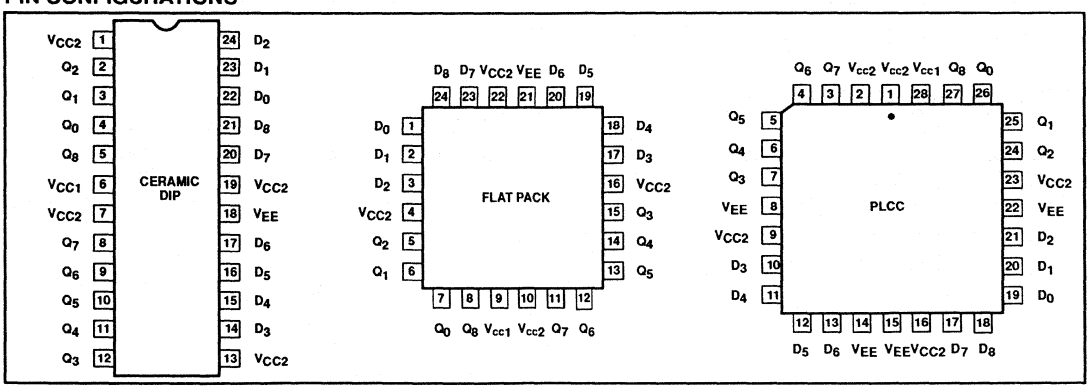
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_8$	Data Inputs
$Q_0 - Q_8$	Data Outputs

ORDERING INFORMATION

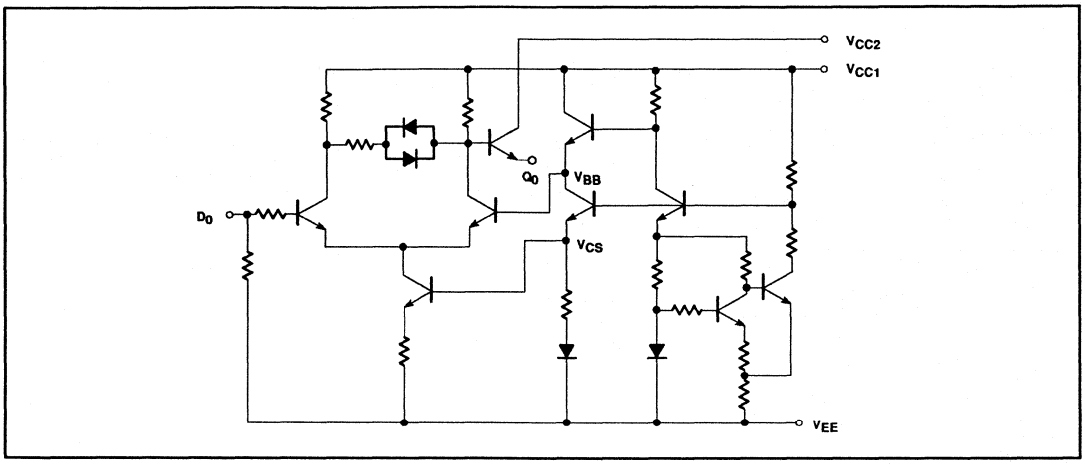
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP their (400 mils wide)	100126F
24–Pin Ceramic Flat Pack	100126Y
28–Pin PLCC	100126A

PIN CONFIGURATIONS



Backplane Driver | 100126

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified·

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

Backplane Driver | 100126

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs Loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					350	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}.			46	78	96	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C MIN.	LIMITS T_A = 0°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH}	Propagation delay D_n to Q_n	Waveform 1	1.05	2.75	1.05	2.75	1.05	2.75	ns
t_{PHL}			1.05	2.75	1.05	2.75	1.05	2.75	ns
t_{TLH}	Transition time Q_n		1.15	3.30	1.15	3.30	1.05	3.30	ns
t_{THL}			1.15	3.30	1.15	3.30	1.05	3.30	ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.05 1.05	2.75 2.75	1.05 1.05	2.75 2.75	1.05 1.05	2.75 2.75	ns ns
t_{TLH} t_{THL}	Transition time Q_n		1.15 1.15	3.30 3.30	1.15 1.15	3.30 3.30	1.05 1.05	3.30 3.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.05 1.05	2.55 2.55	1.05 1.05	2.55 2.55	1.05 1.05	2.55 2.55	ns ns
t_{TLH} t_{THL}	Transition time Q_n		1.15 1.15	3.30 3.30	1.15 1.15	3.30 3.30	1.05 1.05	3.30 3.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

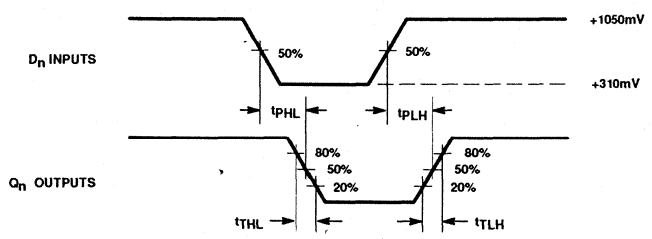
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.05 1.05	2.55 2.55	1.05 1.05	2.55 2.55	1.05 1.05	2.55 2.55	ns ns
t_{TLH} t_{THL}	Transition time Q_n		1.15 1.15	3.30 3.30	1.15 1.15	3.30 3.30	1.05 1.05	3.30 3.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–0617
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100131

Triple D–Type Master–Slave Flip–Flop

FEATURES

- **Typical propagation delay: 1.3ns**
- **Typical supply current ($-I_{EE}$): 110mA**

DESCRIPTION

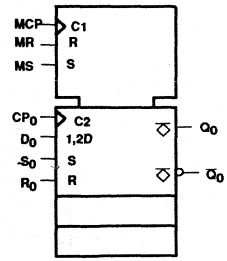
100131 has three D–type master–slave flip–flops with true and complementary outputs. In addition to common clock, set and reset lines, each flip–flop also has individual clock, set and reset lines.

Unused input must be tied to a low voltage, either V_{IL} or V_{EE}.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_2$	Data Inputs
MCP	Master Clock Input
$CP_0 - CP_2$	Individual Clock Inputs
MS	Master Set Input
$S_0 - S_2$	Individual Set Inputs
MR	Master Reset Input
$R_0 - R_2$	Individual Reset Input
$Q_0 - Q_2$	True Data Outputs
$\overline{Q}_0 - \overline{Q}_2$	Complementary Data Outputs

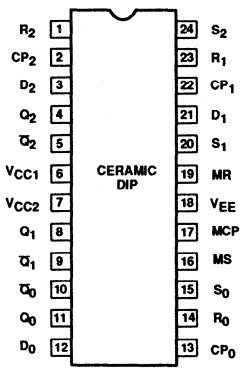
IEC/IEEE SYMBOL

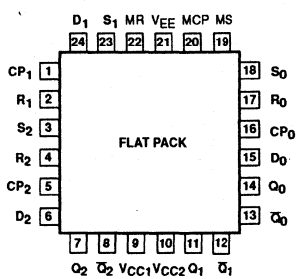


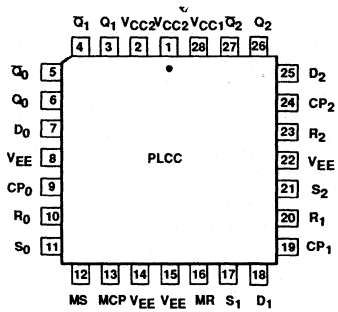
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100131F
24–Pin Ceramic Flat Pack	100131Y
28–Pin PLCC	100131A

PIN CONFIGURATIONS

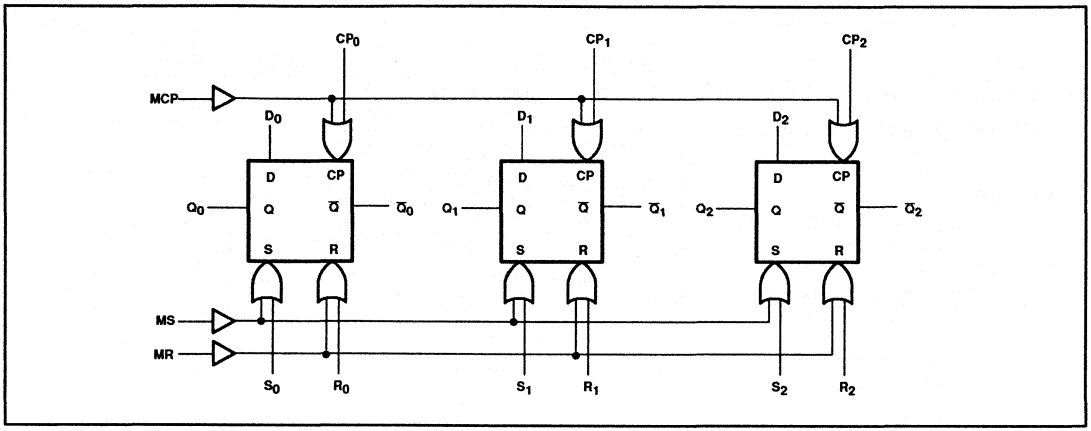






Flip–Flop 100131

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS	
D_n	MCP	CP_n	MS	S_n	MR	R_n	Q_n	$\overline{Q}_n$
X	X	X	L	L	H	X	L	H
X	X	X	L	L	X	H	L	H
X	X	X	H	X	L	L	H	L
X	X	X	X	H	L	L	H	L
X	X	X	H	X	H	X	undefined	
X	X	X	H	X	X	H	undefined	
X	X	X	X	H	H	X	undefined	
X	X	X	X	H	X	H	undefined	
H	↑	L	L	L	L	L	H	L
L	↑	L	L	L	L	L	L	H
H	L	↑	L	L	L	L	H	L
L	L	↑	L	L	L	L	L	H
X	↕	↕	L	L	L	L	NC	NC

NOTES:
H = High voltage level
L = Low voltage level
X = Don't Care
↑ = Low–to–High transition
↕ = No Low–to–High transition
NC = No change

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, $T_A = 0°C$ to $+85°C$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the I0KH ECL family.		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	D_n, CP_n	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					240	µA
		MCP, MS, MR						450	µA
		R_n, S_n						530	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			74	110	149	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.

NOTES (CONTINUED):

3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP V_{CC1} = V_{CC2} = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS						UNIT
				T_A = 0°C		T_A = +25°C		T_A = +85°C		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1		350		350		350		MHz
t_{PLH} t_{PHL}	Propagation delay MCP to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.75 0.75	2.40 2.40	0.75 0.75	2.15 2.15	0.70 0.70	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.70 0.70	2.20 2.20	0.70 0.70	2.00 2.00	0.70 0.70	2.20 2.20	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveforms 2,3	$CP_n = V_{ILMIN}$	1.10 1.10	2.70 2.70	1.05 1.05	2.60 2.60	1.05 1.05	2.70 2.70	ns ns
t_{PLH} t_{PHL}	MS, MR to Q_n, $\overline{Q}_n$		$CP_n = V_{IHMAX}$	1.10 1.10	3.05 3.05	1.10 1.10	2.95 2.95	1.10 1.10	3.05 3.05	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveforms 2,3	$CP_n = V_{ILMIN}$	0.65 0.65	1.90 1.90	0.70 0.70	1.70 1.70	0.70 0.70	1.90 1.90	ns ns
t_{PLH} t_{PHL}	R_n, S_n to Q_n, $\overline{Q}_n$		$CP_n = V_{IHMAX}$	0.70 0.70	2.10 2.10	0.70 0.70	2.00 2.00	0.70 0.70	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1		0.45 0.45	2.00 2.00	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time D_n to CP_n, MCP	Waveforms 2,3		0.90		0.70		0.90		ns
t_h	Hold time CP_n, MCP to D_n			0.60		0.60		0.80		ns
t_R	Release time R_n, S_n to CP_n, MCP	Waveforms 2,3		1.50		1.30		1.50		ns
t_R	Release time MR, MS to CP_n, MCP			2.50		2.30		2.50		ns
$t_w(H)$	Pulse width High MR, MS, R_n, S_n, CP_n, MCP	Waveforms 1,2,3		2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

Flip–Flop 100131

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS						UNIT
				$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1		350		350		350		MHz
t_{PLH} t_{PHL}	Propagation delay MCP to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.75 0.75	2.40 2.40	0.75 0.75	2.15 2.15	0.70 0.70	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.70 0.70	2.20 2.20	0.70 0.70	2.00 2.00	0.70 0.70	2.20 2.20	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveforms 2,3	$CP_n = V_{ILMIN}$	1.10 1.10	2.70 2.70	1.05 1.05	2.60 2.60	1.05 1.05	2.70 2.70	ns ns
t_{PLH} t_{PHL}	MS, MR to Q_n, $\overline{Q}_n$		$CP_n = V_{IHMAX}$	1.10 1.10	3.05 3.05	1.10 1.10	2.95 2.95	1.10 1.10	3.05 3.05	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveforms 2,3	$CP_n = V_{ILMIN}$	0.65 0.65	1.90 1.90	0.70 0.70	1.70 1.70	0.70 0.70	1.90 1.90	ns ns
t_{PLH} t_{PHL}	R_n, S_n to Q_n, $\overline{Q}_n$		$CP_n = V_{IHMAX}$	0.70 0.70	2.10 2.10	0.70 0.70	2.00 2.00	0.70 0.70	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1		0.45 0.45	2.00 2.00	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time D_n to CP_n, MCP	Waveforms 2,3		0.90		0.70		0.90		ns
t_h	Hold time CP_n, MCP to D_n			0.60		0.60		0.80		ns
t_R	Release time R_n, S_n to CP_n, MCP	Waveforms 2,3		1.50		1.30		1.50		ns
t_R	Release time MR, MS to CP_n, MCP			2.50		2.30		2.50		ns
$t_w(H)$	Pulse width High MR, MS, R_n, S_n, CP_n, MCP	Waveforms 1,2,3		2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} =$ ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS						UNIT
				$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1		350		350		350		MHz
t_{PLH} t_{PHL}	Propagation delay MCP to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.75 0.75	2.20 2.20	0.75 0.75	1.95 1.95	0.70 0.70	2.10 2.10	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.70 0.70	2.00 2.00	0.70 0.70	1.80 1.80	0.70 0.70	2.00 2.00	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveforms 2,3	$CP_n = V_{ILMIN}$	1.10 1.10	2.50 2.50	1.05 1.05	2.40 2.40	1.05 1.05	2.50 2.50	ns ns
t_{PLH} t_{PHL}	MS, MR to Q_n, $\overline{Q}_n$		$CP_n = V_{IHMAX}$	1.15 1.15	2.85 2.85	1.05 1.05	2.75 2.75	1.05 1.05	2.85 2.85	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveforms 2,3	$CP_n = V_{ILMIN}$	0.65 0.65	1.70 1.70	0.70 0.70	1.50 1.50	0.70 0.70	1.70 1.70	ns ns
t_{PLH} t_{PHL}	R_n, S_n to Q_n, $\overline{Q}_n$		$CP_n = V_{IHMAX}$	0.70 0.70	1.90 1.90	0.70 0.70	1.80 1.80	0.70 0.70	2.00 2.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1		0.45 0.45	2.00 2.00	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time D_n to CP_n, MCP	Waveforms 2,3		0.80		0.60		0.80		ns
t_h	Hold time CP_n, MCP to D_n			0.50		0.50		0.70		ns
t_R	Release time R_n, S_n to CP_n, MCP	Waveforms 2,3		1.40		1.20		1.40		ns
t_R	Release time MR, MS to CP_n, MCP			2.40		2.20		2.40		ns
$t_w(H)$	Pulse width High MR, MS, R_n, S_n, CP_n, MCP	Waveforms 1,2,3		2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

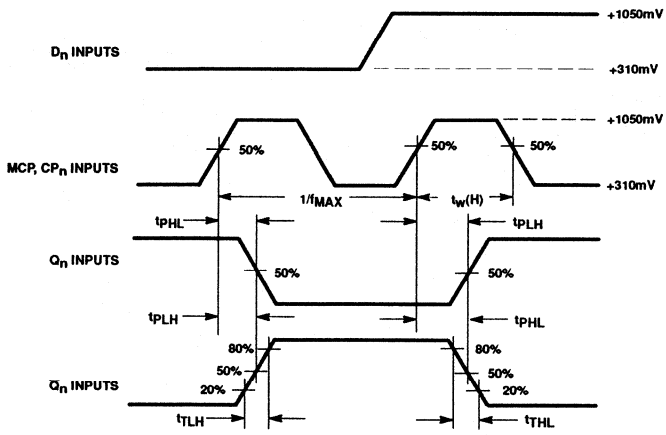
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

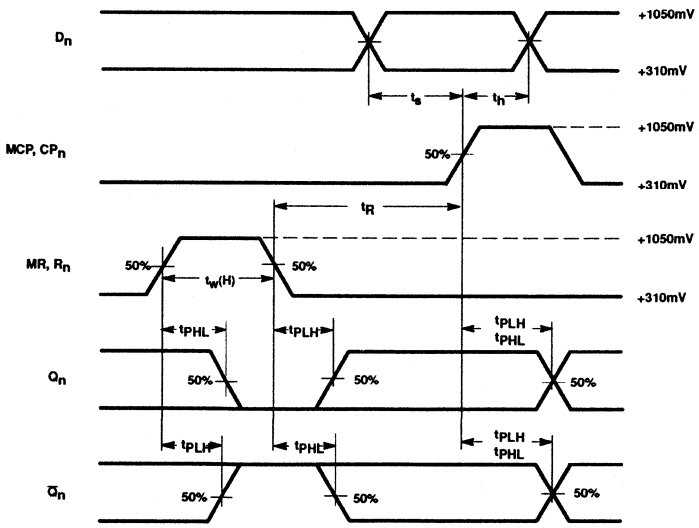
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS						UNIT
				$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1		350		350		350		MHz
t_{PLH} t_{PHL}	Propagation delay MCP to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.75 0.75	2.20 2.20	0.75 0.75	1.95 1.95	0.70 0.70	2.10 2.10	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.70 0.70	2.00 2.00	0.70 0.70	1.80 1.80	0.70 0.70	2.00 2.00	ns ns
t_{PLH} t_{PHL}	Propagation delay MS, MR to Q_n, $\overline{Q}_n$	Waveforms 2,3	$CP_n = V_{ILMIN}$	1.10 1.10	2.50 2.50	1.05 1.05	2.40 2.40	1.05 1.05	2.50 2.50	ns ns
t_{PLH} t_{PHL}			$CP_n = V_{IHMAX}$	1.15 1.15	2.85 2.85	1.05 1.05	2.75 2.75	1.05 1.05	2.85 2.85	ns ns
t_{PLH} t_{PHL}	Propagation delay R_n, S_n to Q_n, $\overline{Q}_n$	Waveforms 2,3	$CP_n = V_{ILMIN}$	0.65 0.65	1.70 1.70	0.70 0.70	1.50 1.50	0.70 0.70	1.70 1.70	ns ns
t_{PLH} t_{PHL}			$CP_n = V_{IHMAX}$	0.70 0.70	1.90 1.90	0.70 0.70	1.80 1.80	0.70 0.70	2.00 2.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1		0.45 0.45	2.00 2.00	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time D_n to CP_n, MCP	Waveforms 2,3		0.80		0.60		0.80		ns
t_h	Hold time CP_n, MCP to D_n			0.50		0.50		0.70		ns
t_R	Release time R_n, S_n to CP_n, MCP	Waveforms 2,3		1.40		1.20		1.40		ns
t_R	Release time MR, MS to CP_n, MCP			2.40		2.20		2.40		ns
$t_w(H)$	Pulse width High MR, MS, R_n, S_n, CP_n, MCP	Waveforms 1,2,3		2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



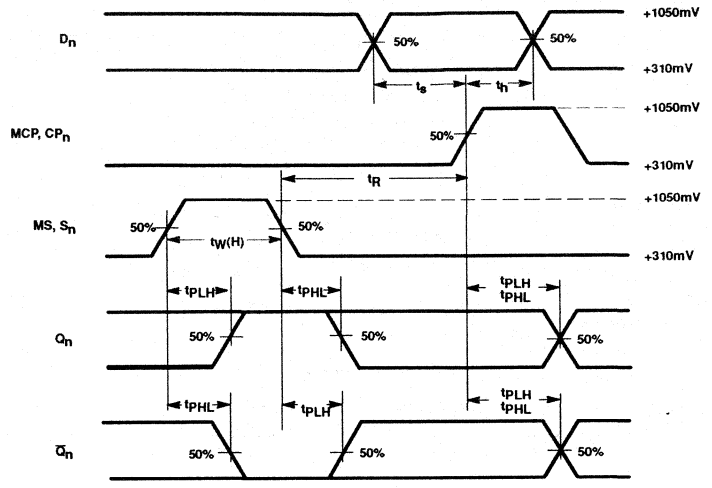
Waveform 1. Propagation Delays and Transition Times



Waveform 2. Reset, Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

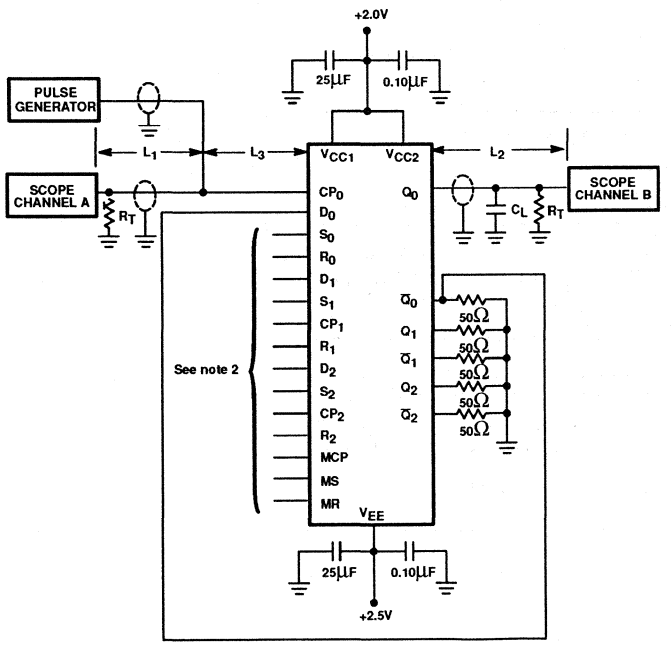
AC WAVEFORMS



Waveform 3. Set, Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

TOGGLE FREQUENCY TEST CIRCUIT



NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

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ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100136

Counter/Shift Register

FEATURES

- **Typical propagation delay: 1.8ns**
- **Typical supply current ($-I_{EE}$): 210mA**

DESCRIPTION

The 100136 functions as a four–bit counter or as a 4–bit, bidirectional shift register. These functions are determined by the three Select Inputs $S_0 - S_2$, which also allow for parallel loading, as well as complementing, clearing and holding the register contents.

In the Parallel Load mode, data can be entered into the register via the Preset inputs ($P_0 - P_3$). Outputs $Q_0 - Q_3$ reflect the state of the register, $\overline{Q}_0 - \overline{Q}_3$ give the complement of that state. A High signal on the Master Reset input will clear the value of the register contents to zero asynchronously and without regard for signals at the other inputs.

When using the 100136 in the Count Up mode, the Terminal Count output ($\overline{TC}$) goes Low when the register reaches a value of 15. In the Count Down mode, $\overline{TC}$ goes Low when the register reaches a value of zero.

When operating the 100136 in the Right Shift mode, $D_0/\overline{CET}$ serves as the serial data input. In the Left Shift mode, D_3 serves as the serial input. When shifting, the $\overline{TC}$ output has the same level as the Q_3 output.

Two count enable inputs ($\overline{CEP}$ and $D_0/\overline{CET}$) can be used in combination with the $\overline{TC}$ output to cascade more than one 100136, allowing for counting and shift capability of eight bits or more. The dual nature of the $\overline{TC}/Q_3$ outputs and the $D_0/\overline{CET}$ input allow the same control lines, interconnected between stages, to be used for either the Count or the Right Shift operation.

Unused inputs must be tied to low voltage, either V_{IL} or V_{EE}.

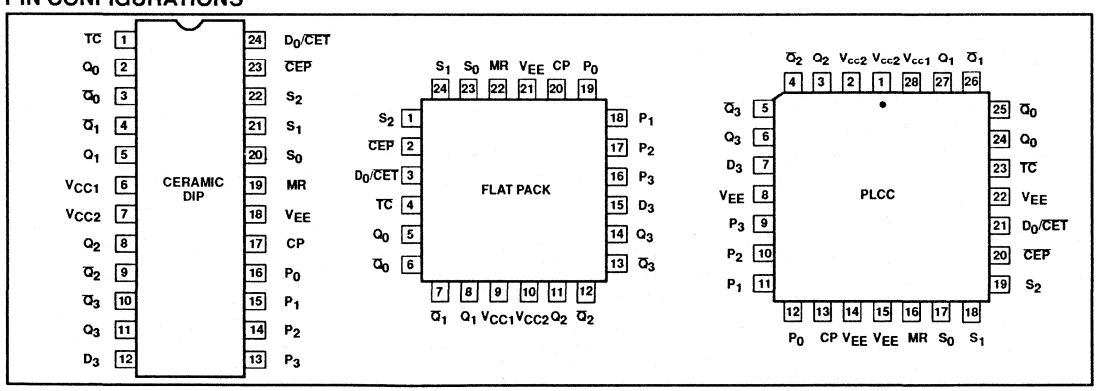
PIN DESCRIPTION

PINS	DESCRIPTION
D_3	Serial Data Inputs (Left Shift)
$P_0 - P_3$	Preset Inputs
CP	Clock Input
$D_0/\overline{CET}$	Serial Data Input (Right Shift) and Count Enable Trickle Input (Active–Low)
$\overline{CEP}$	Count Enable Parallel Input (Active–Low)
$S_0 - S_2$	Select Inputs
MR	Master Reset Input
$\overline{TC}$	Terminal Count Output
$Q_0 - Q_3$	Data Outputs

ORDERING INFORMATION

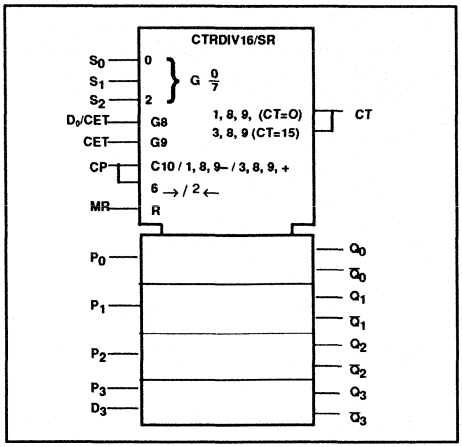
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100136F
24–Pin Ceramic Flat Pack	100136Y
28–Pin PLCC	100136A

PIN CONFIGURATIONS

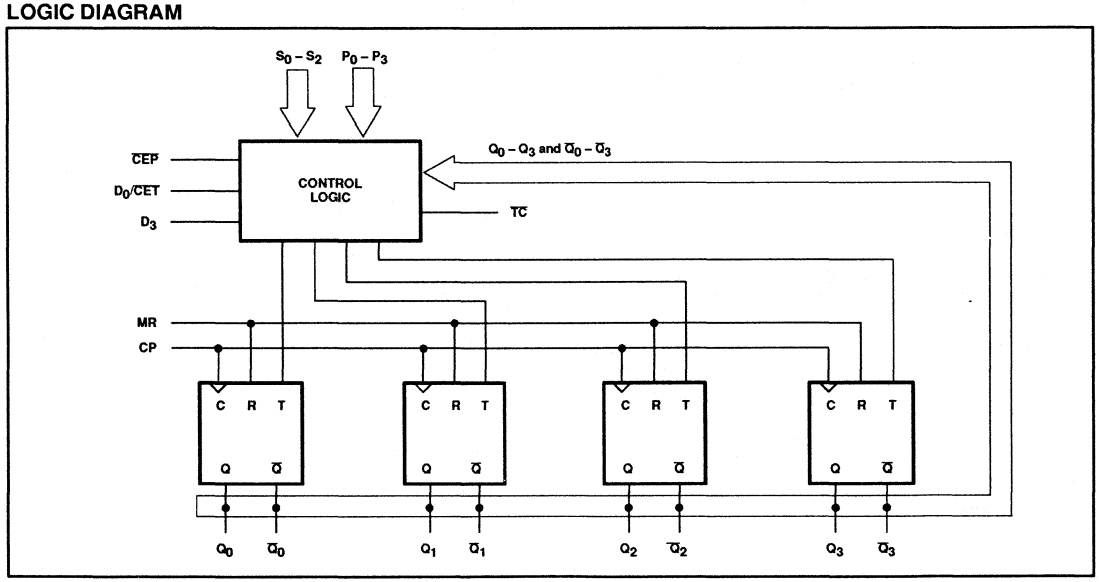


Counter/Shift Register 100136

IEC/IEEE SYMBOL



LOGIC DIAGRAM



Counter/Shift Register | 100136

FUNCTION TABLE

INPUTS								OUTPUTS					MODE
MR	S_2	S_1	S_0	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	
L	L	L	L	X	X	X	↑	P_0	P_1	P_2	P_3	L	Parallel Load
L	L	L	H	X	X	X	↑	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	L	Complement
L	L	H	L	X	X	L	↑	Q_1	Q_2	Q_3	L	L	Left Shift
L	L	H	L	X	X	H	↑	Q_1	Q_2	Q_3	H	H	(D_3 is the active serial input)
L	L	H	H	X	L	X	↑	L	Q_0	Q_1	Q_2	Q_2*	Right Shift
L	L	H	H	X	H	X	↑	H	Q_0	Q_1	Q_2	Q_2*	($D_0/\overline{CET}$ is the active serial input)
L	H	L	L	L	L	X	↑	(Q_{0-3}) minus 1				(1)	Count Down
L	H	L	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	(1)	Count Down disabled with $\overline{CEP}$ High
L	H	L	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Down disabled with $D_0/\overline{CET}$ High
L	H	L	H	X	X	X	↑	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↑	(Q_{0-3}) plus 1				(2)	Count Up
L	H	H	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	(2)	Count Up disabled with $\overline{CEP}$ High
L	H	H	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Up disabled with $D_0/\overline{CET}$ High
L	H	H	H	X	X	X	X	Q_0	Q_1	Q_2	Q_3	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

NOTES:

(1) = L if $Q_0 - Q_3$ = LLLL, H if $Q_0 - Q_3 \neq$ LLLL
(2) = L if $Q_0 - Q_3$ = HHHH, H if $Q_0 - Q_3 \neq$ HHHH
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low–to–High transition
* Before the clock, $\overline{TC}$ is Q_3; after the clock, $\overline{TC}$ is Q_2

FUNCTION SELECT TABLE

S_2	S_1	S_0	FUNCTION
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Left Shift
L	H	H	Right Shift
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

NOTES:

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:

Operation beyond the limits set forth in this table may impair the useful life of the device.

Counter/Shift Register 100136

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	P_n, S_n	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					180	µA
		$\overline{CEP}$						200	µA
		MR						240	µA
		D_3						280	µA
		CP						390	µA
		$D_0/\overline{CET}$						530	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			136	210	283	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage

NOTES (CONTINUED):

and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.

2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX	
f_{MAX}	Maximum shift frequency CP	Waveform 1	250		250		250		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.85 0.85	2.10 2.10	0.85 0.85	2.10 2.10	0.85 0.85	2.25 2.25	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		1.80 1.80	4.80 4.80	1.80 1.80	4.60 4.60	1.80 1.80	5.20 5.20	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	1.20 1.20	2.95 2.95	1.35 1.35	2.95 2.95	1.20 1.20	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to $\overline{TC}$		2.10 2.10	4.80 4.80	2.10 2.10	4.80 4.80	2.10 2.10	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay $D_0/\overline{CET}$ to $\overline{TC}$	Waveform 3	1.40 1.40	3.20 3.20	1.40 1.40	3.20 3.20	1.40 1.40	3.50 3.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{TC}$		1.40 1.40	4.60 4.60	1.60 1.60	4.60 4.60	1.60 1.60	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, $\overline{TC}$	Waveform 1	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns
t_s	Setup time D_3 to CP	Waveform 2	1.40		1.40		1.40		ns
t_h	Hold time CP to D_3		0.20		0.20		0.20		ns
t_s	Setup time P_n to CP		1.70		1.70		1.70		ns
t_h	Hold time CP to P_n		0.10		0.10		0.10		ns
t_s	Setup time $D_0/\overline{CET}$, $\overline{CEP}$ to CP		1.80		1.80		1.80		ns
t_h	Hold time CP to $D_0/\overline{CET}$, $\overline{CEP}$		0.20		0.20		0.20		ns
t_s	Setup time S_n to CP		3.80		3.80		3.80		ns
t_h	Hold time CP to S_n		–0.9		–0.9		–0.9		ns
t_R	Release time MR to CP		2.50		2.50		2.50		ns
t_w(H)	Pulse width High, MR, CP	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX	
f_{MAX}	Maximum shift frequency CP	Waveform 1	250		250		250		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.85 0.85	2.10 2.10	0.85 0.85	2.10 2.10	0.85 0.85	2.25 2.25	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		1.80 1.80	4.80 4.80	1.80 1.80	4.60 4.60	1.80 1.80	5.20 5.20	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	1.20 1.20	2.95 2.95	1.35 1.35	2.95 2.95	1.20 1.20	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to $\overline{TC}$		2.10 2.10	4.80 4.80	2.10 2.10	4.80 4.80	2.10 2.10	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay $D_0/\overline{CET}$ to $\overline{TC}$	Waveform 3	1.40 1.40	3.20 3.20	1.40 1.40	3.20 3.20	1.40 1.40	3.50 3.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{TC}$		1.40 1.40	4.60 4.60	1.60 1.60	4.60 4.60	1.60 1.60	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, $\overline{TC}$	Waveform 1	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns
t_s	Setup time D_3 to CP	Waveform 2	1.40		1.40		1.40		ns
t_h	Hold time CP to D_3		0.20		0.20		0.20		ns
t_s	Setup time P_n to CP		1.70		1.70		1.70		ns
t_h	Hold time CP to P_n		0.10		0.10		0.10		ns
t_s	Setup time $D_0/\overline{CET}$, $\overline{CEP}$ to CP		1.80		1.80		1.80		ns
t_h	Hold time CP to $D_0/\overline{CET}$, $\overline{CEP}$		0.20		0.20		0.20		ns
t_s	Setup time S_n to CP		3.80		3.80		3.80		ns
t_h	Hold time CP to S_n		–0.9		–0.9		–0.9		ns
t_R	Release time MR to CP		2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High, MR, CP	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX	
f_{MAX}	Maximum shift frequency CP	Waveform 1	250		250		250		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.85 0.85	2.15 2.15	0.85 0.85	2.15 2.15	0.85 0.85	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		1.80 1.80	4.60 4.60	1.80 1.80	4.40 4.40	1.80 1.80	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	1.20 1.20	2.75 2.75	1.35 1.35	2.75 2.75	1.20 1.20	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to $\overline{TC}$		2.10 2.10	4.60 4.60	2.10 2.10	4.60 4.60	2.10 2.10	4.80 4.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $D_0/\overline{CET}$ to $\overline{TC}$	Waveform 3	1.40 1.40	3.00 3.00	1.40 1.40	3.00 3.00	1.40 1.40	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{TC}$		1.40 1.40	4.60 4.60	1.60 1.60	4.60 4.60	1.60 1.60	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, $\overline{TC}$	Waveform 1	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns
t_s	Setup time D_3 to CP	Waveform 2	1.40		1.40		1.40		ns
t_h	Hold time CP to D_3		0.00		0.00		0.00		ns
t_s	Setup time P_n to CP		1.60		1.60		1.60		ns
t_h	Hold time CP to P_n		0.00		0.00		0.00		ns
t_s	Setup time $D_0/\overline{CET}$, $\overline{CEP}$ to CP		1.80		1.80		1.80		ns
t_h	Hold time CP to $D_0/\overline{CET}$, $\overline{CEP}$		0.00		0.00		0.00		ns
t_s	Setup time S_n to CP		3.60		3.60		3.60		ns
t_h	Hold time CP to S_n		–0.4		–0.4		–0.4		ns
t_R	Release time MR to CP		2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High, MR, CP	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

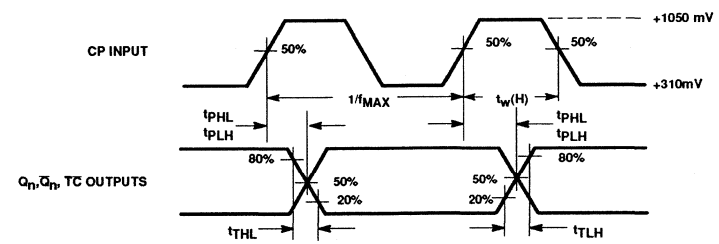
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX	
f_{MAX}	Maximum shift frequency CP	Waveform 1	250		250		250		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.85 0.85	2.15 2.15	0.85 0.85	2.15 2.15	0.85 0.85	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		1.80 1.80	4.60 4.60	1.80 1.80	4.40 4.40	1.80 1.80	5.00 5.00	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	1.20 1.20	2.75 2.75	1.35 1.35	2.75 2.75	1.20 1.20	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to $\overline{TC}$		2.10 2.10	4.60 4.60	2.10 2.10	4.60 4.60	2.10 2.10	4.80 4.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $D_0/\overline{CET}$ to $\overline{TC}$	Waveform 3	1.40 1.40	3.00 3.00	1.40 1.40	3.00 3.00	1.40 1.40	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{TC}$		1.40 1.40	4.60 4.60	1.60 1.60	4.60 4.60	1.60 1.60	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, $\overline{TC}$	Waveform 1	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns
t_s	Setup time D_3 to CP	Waveform 2	1.40		1.40		1.40		ns
t_h	Hold time CP to D_3		0.00		0.00		0.00		ns
t_s	Setup time P_n to CP		1.60		1.60		1.60		ns
t_h	Hold time CP to P_n		0.00		0.00		0.00		ns
t_s	Setup time $D_0/\overline{CET}$, $\overline{CEP}$ to CP		1.80		1.80		1.80		ns
t_h	Hold time CP to $D_0/\overline{CET}$, $\overline{CEP}$		0.00		0.00		0.00		ns
t_s	Setup time S_n to CP		3.60		3.60		3.60		ns
t_h	Hold time CP to S_n		–0.4		–0.4		–0.4		ns
t_R	Release time MR to CP		2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High, MR, CP	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

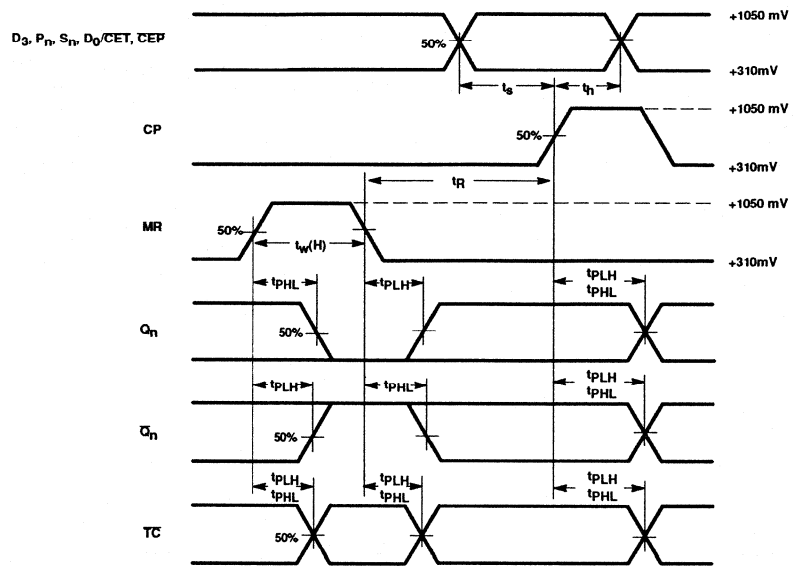
AC WAVEFORMS



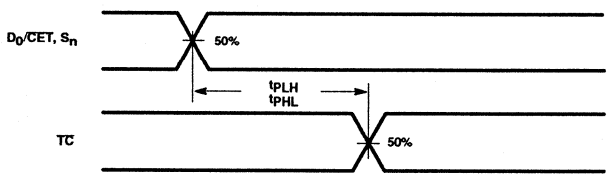
Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

AC WAVEFORMS



Waveform 2. Reset, Setup and Hold Times



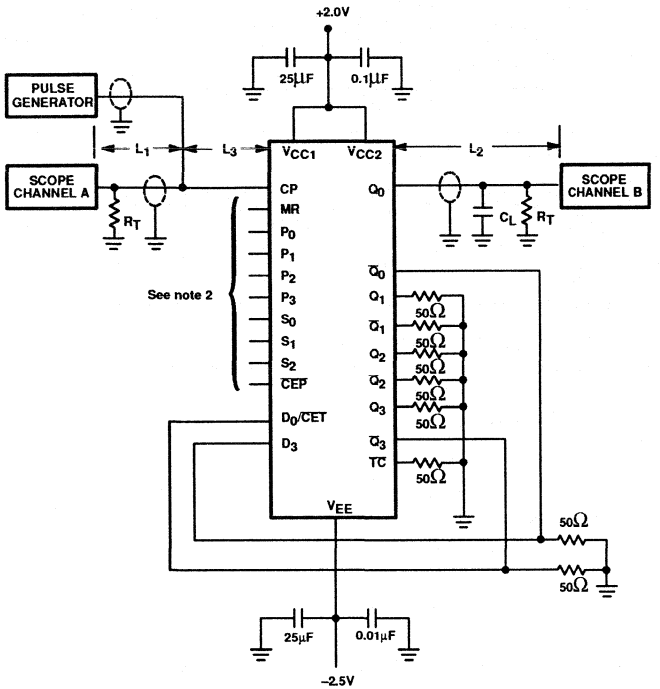
Waveform 3. Data Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Counter/Shift Register

100136

SHIFT FREQUENCY TEST CIRCUIT

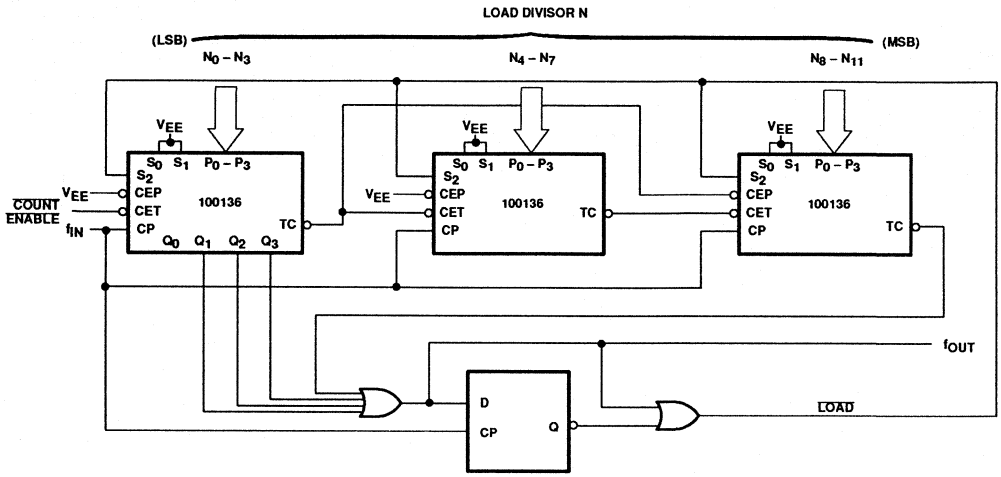


NOTES:

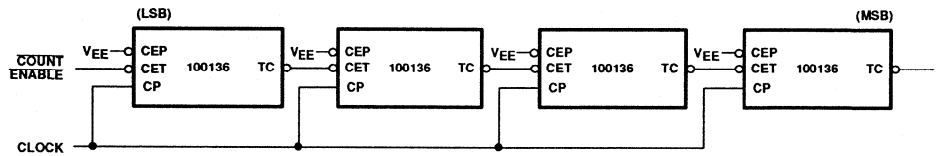
1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.
9. While S_0 through S_2 are set fo Parallel Load mode, a four–bit word is entered at inputs P_0 through P_3. Then, So through S2 can be set for Right shift or Left Shift mode, whereby a bit pattern will advance across the outputs with every rising edge of the clock pulse CP. The wires connecting $\overline{Q}_0$ to D_3 and $\overline{Q}_3$ to D_0/CET ensure circular shifting and should be as short as possible. The shift frequency is determined from the bit pattern as seen by Scope Channel B.

APPLICATION CIRCUITS

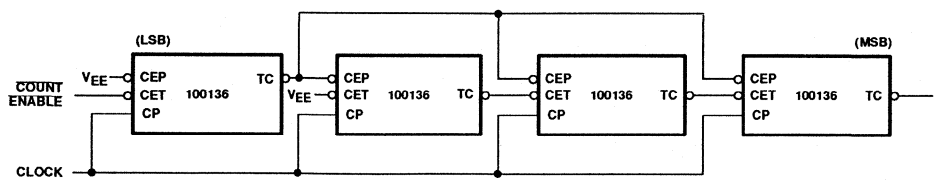
3–STAGE DIVIDER USING PARALLEL LOAD AND COUNT DOWN MODES



SLOW EXPANSION SCHEME FOR COUNTING AND RIGHT SHIFT



FAST EXPANSION SCHEME FOR COUNTING



Philips Components

Document No.	853–0619
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100141

4–Bit Universal Shift Register

FEATURES

- **Typical propagation delay: 1.7ns**
- **Typical supply current ($-I_{EE}$): 175mA**

DESCRIPTION

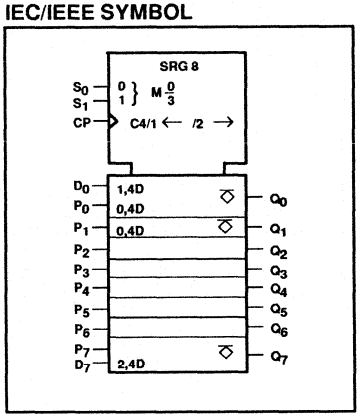
The 100141 is an 8–bit shift register with D–type flip–flops. There are two selection inputs, S_0 and S_1, allowing Parallel Load, Left Shift, Right Shift, and Hold modes. Unused inputs must be tied Low (to V_{IL} or V_{EE}).

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Serial Data Inputs
$P_0 - P_7$	Parallel Data Inputs
CP	Clock Input
S_0, S_1	Select Inputs
$Q_0 - Q_7$	Data Outputs

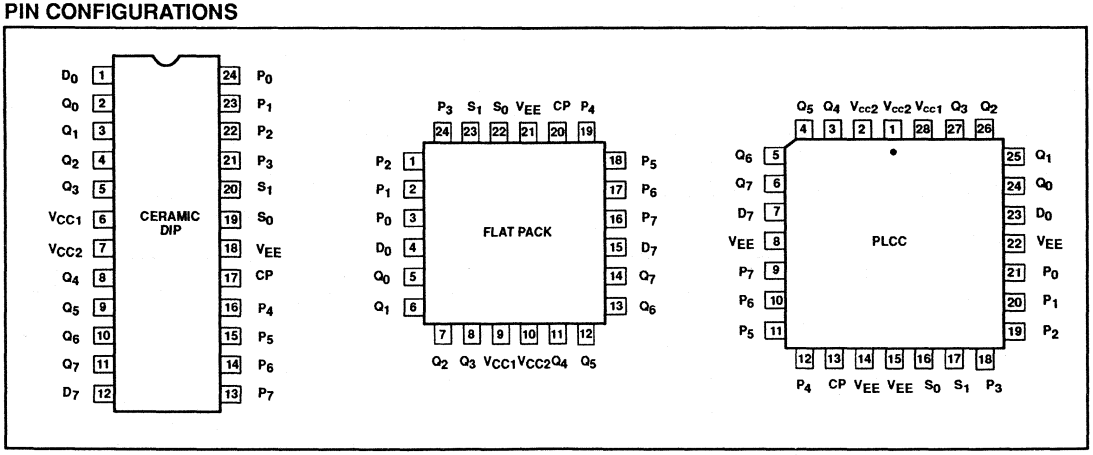
IEC/IEEE SYMBOL



ORDERING INFORMATION

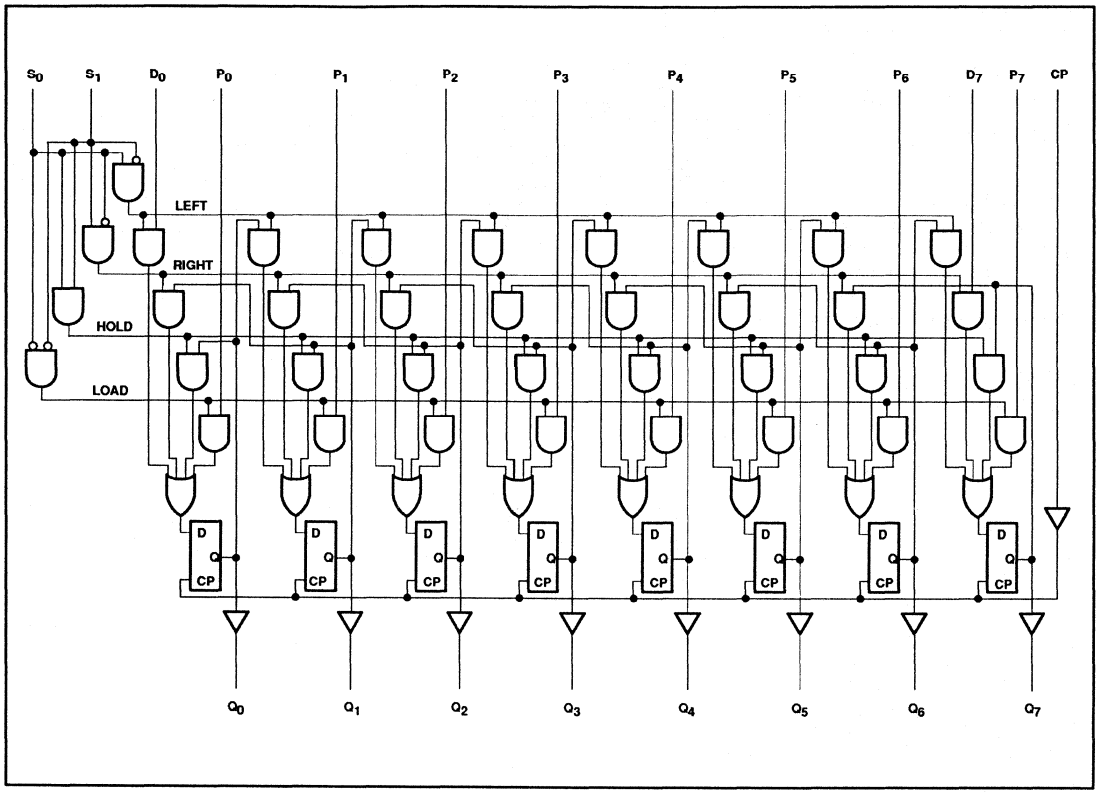
PACKAGES	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100141F
24–Pin Ceramic Flat Pack	100141Y
28–Pin PLCC	100141A

PIN CONFIGURATIONS



Shift Register 100141

LOGIC DIAGRAM



FUNCTION TABLE

FUNCTION	INPUTS					OUTPUTS							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Parallel Load into Register	X	X	L	L	↑	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X X	L H	L L	H H	↑ ↑	Q_6 Q_6	Q_5 Q_5	Q_4 Q_4	Q_3 Q_3	Q_2 Q_2	Q_1 Q_1	Q_0 Q_0	L H
Shift Right	L H	X X	H H	L L	↑ ↑	L H	Q_7 Q_7	Q_6 Q_6	Q_5 Q_5	Q_4 Q_4	Q_3 Q_3	Q_2 Q_2	Q_1 Q_1
Hold	X X X	X X X	H X X	H X X	X H L	← No Change →							

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low–to–High transition

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	CP	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					550	µA
		D_n, P_n, S_n						220	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			119	175	238	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum shift frequency CP	Waveform 1	275		275		275		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	0.90 0.90	2.40 2.40	1.10 1.10	2.40 2.40	1.10 1.10	2.55 2.55	ns ns
t_{TLH} t_{THL}	Transition time		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n, P_n to CP	Waveform 2	1.40		1.40		1.70		ns
t_h	Hold time CP to D_n, P_n		0.60		0.60		0.60		ns
t_s	Setup time S_n to CP	Waveform 2	3.80		3.80		3.80		ns
t_h	Hold time CP to S_n		0.10		0.10		0.10		ns
$t_w(H)$	Pulse width High CP	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum shift frequency CP	Waveform 1	275		275		275		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	0.90 0.90	2.40 2.40	1.10 1.10	2.40 2.40	1.10 1.10	2.55 2.55	ns ns
t_{TLH} t_{THL}	Transition time		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n, P_n to CP	Waveform 2	1.40		1.40		1.70		ns
t_h	Hold time CP to D_n, P_n		0.60		0.60		0.60		ns
t_s	Setup time S_n to CP	Waveform 2	3.80		3.80		3.80		ns
t_h	Hold time CP to S_n		0.10		0.10		0.10		ns
$t_w(H)$	Pulse width High CP	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum shift frequency CP	Waveform 1	300		300		300		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	0.90 0.90	2.20 2.20	1.10 1.10	2.20 2.20	1.10 1.10	2.35 2.35	ns ns
t_{TLH} t_{THL}	Transition time		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n, P_n to CP	Waveform 2	1.20		1.20		1.50		ns
t_h	Hold time CP to D_n, P_n		0.50		0.50		0.50		ns
t_s	Setup time S_n to CP	Waveform 2	2.80		2.80		3.20		ns
t_h	Hold time CP to S_n		0.00		0.00		0.00		ns
$t_w(H)$	Pulse width High CP	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

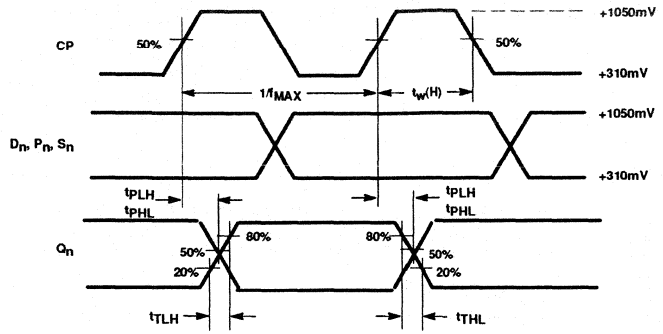
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

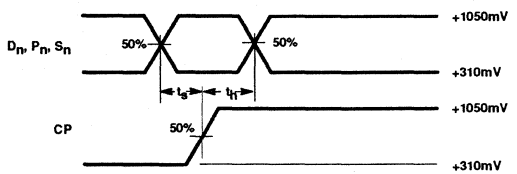
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum shift frequency CP	Waveform 1	300		300		300		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	0.90 0.90	2.20 2.20	1.10 1.10	2.20 2.20	1.10 1.10	2.35 2.35	ns ns
t_{TLH} t_{THL}	Transition time		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n, P_n to CP	Waveform 2	1.20		1.20		1.50		ns
t_h	Hold time CP to D_n, P_n		0.50		0.50		0.50		ns
t_s	Setup time S_n to CP	Waveform 2	2.80		2.80		3.20		ns
t_h	Hold time CP to S_n		0.00		0.00		0.00		ns
$t_w(H)$	Pulse width High CP	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



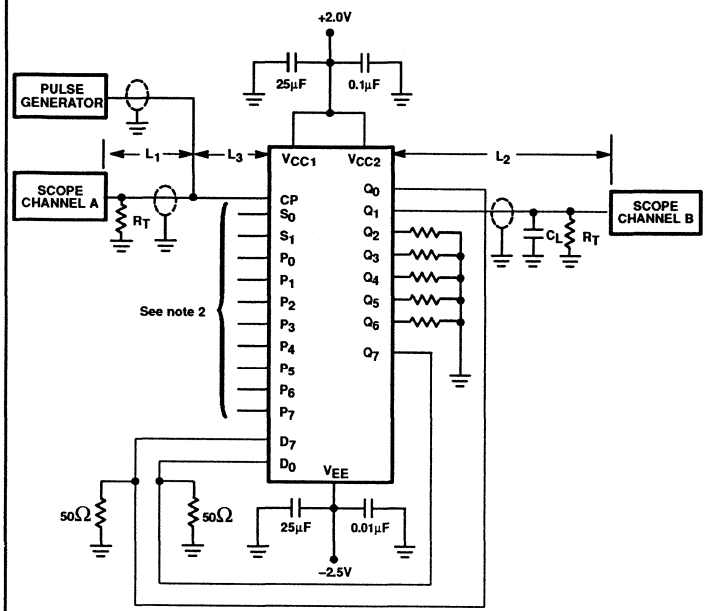
Waveform 1. Propagation Delay and Transition Times



Waveform 2. Data Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

SHIFT FREQUENCY TEST CIRCUIT



NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.
9. While S_0 and S_2 are set for Parallel Load mode, an eight–bit word of alternating zeros and ones is entered at inputs P_0 through P_7. Then, S_0 and S_1 can be set for Right shift or Left Shift mode, whereby the alternating bit pattern will advance across the outputs with every rising edge of the clock pulse (CP). The wires connecting Q_7 to D_0 and Q_0 to D_7 ensure circular shifting and should be as short as possible. The frequency of the resulting square wave, measurable at any Q_n output, is the shift frequency.

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Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100150

Hex D–Type Latch

FEATURES

- **Typical propagation delay: 0.85ns for the data inputs, 1.2ns for the enable inputs**
- **Typical supply current ($-I_{EE}$): 102mA**

DESCRIPTION

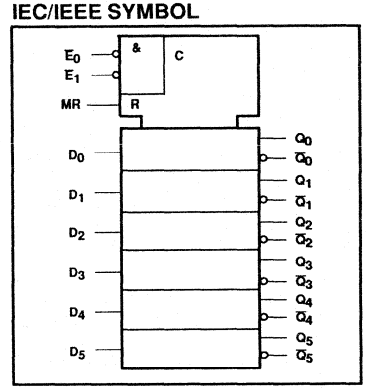
The 100150 contains six D–type latches, with True and Complementary outputs, a pair of common enables (E_0, E_1) and a common Master Reset (MR). A Q output follows its D input when both E_0 or E_1 are Low. When either E_0 or E_1 (or both) are High, a latch stores the last valid data present on its D input before E_0 or E_1 goes High. The MR input overrides all other inputs and makes the Q output Low.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
E_0, E_1	Common Enable Inputs
MR	Master Reset Input
$Q_0 - Q_5$	True Data Outputs
$\overline{Q}_0 - \overline{Q}_5$	Complementary Data Outputs

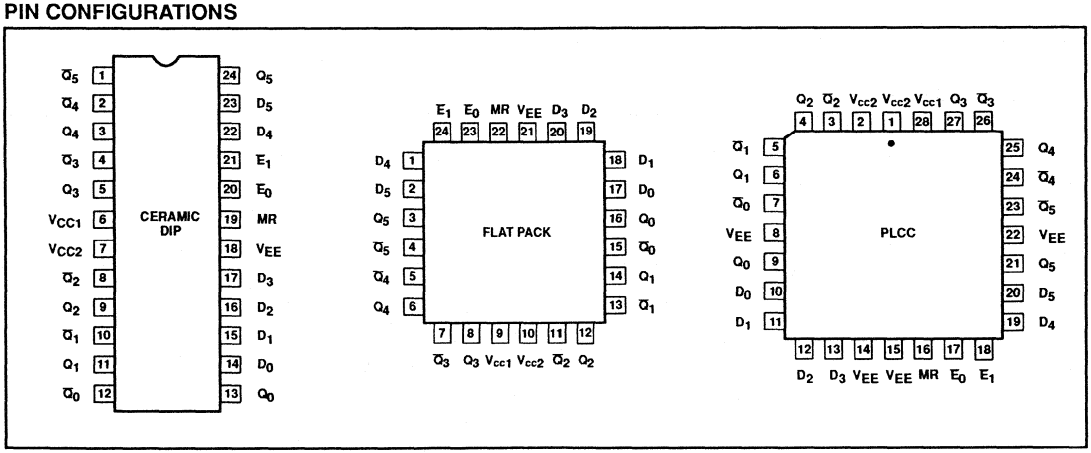
IEC/IEEE SYMBOL



ORDERING INFORMATION

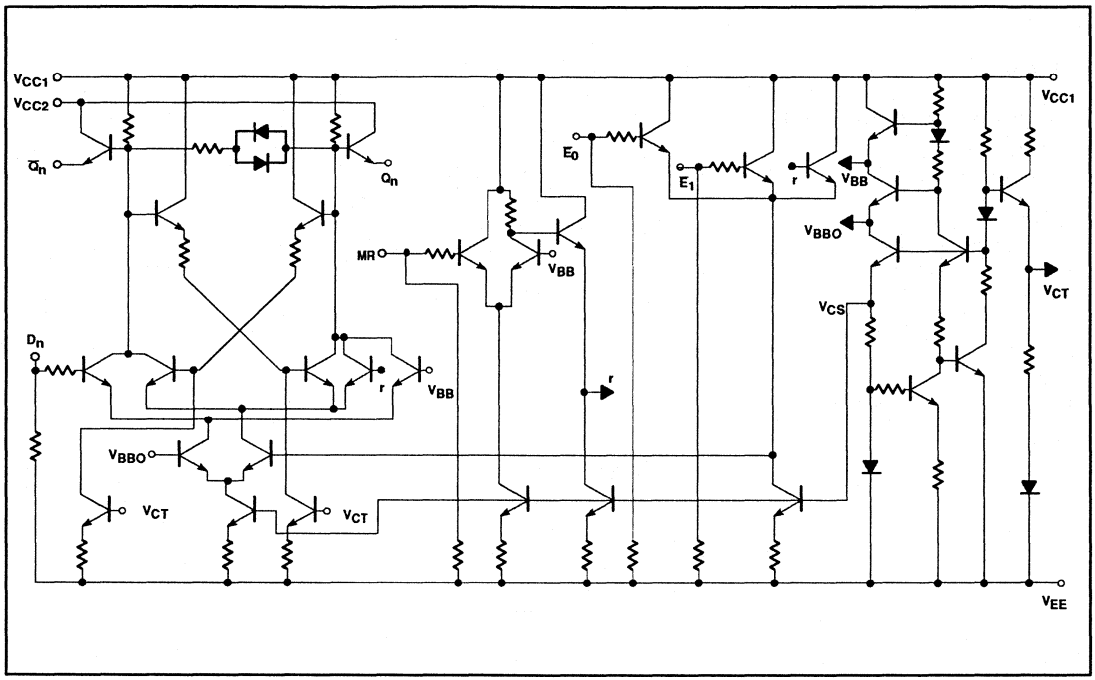
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100150F
24–Pin Ceramic Flat Pack	100150Y
28–Pin PLCC	100150A

PIN CONFIGURATIONS

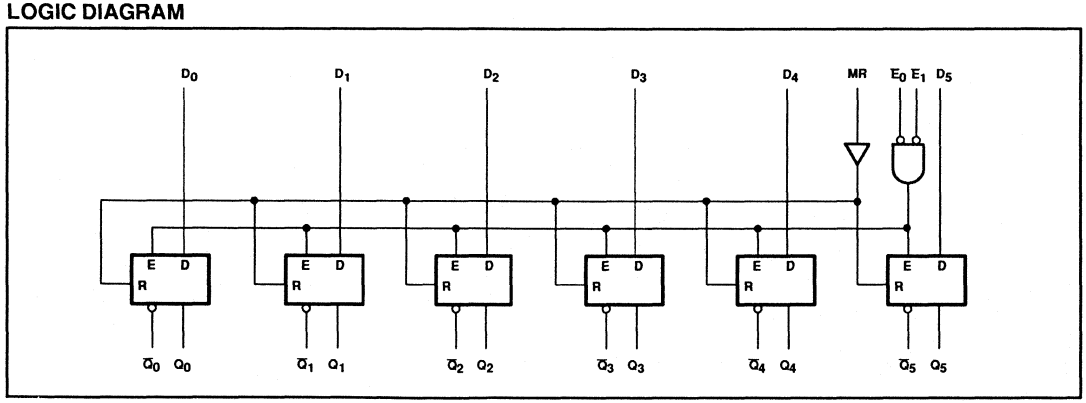


Latch 100150

SIMPLIFIED SCHEMATIC



LOGIC DIAGRAM



Latch | 100150

FUNCTION TABLE (Each Latch)

INPUTS				OUTPUTS	
D_n	$\overline{E}_0$	$\overline{E}_1$	MR	Q_n	$\overline{Q}_n$
H L	L L	L L	L L	H L	L H
X X	X H	H X	L L	Latched* Latched*	Latched* Latched*
X	X	X	H	L	H

NOTES:
* MR signal level present on latch outputs just before rising transition of enable line is held on latch outputs.
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	MR	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					450	µA
		D_n						340	µA
		$\overline{E}_n$						520	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			79	102	159	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.50 1.50	0.50 0.50	1.40 1.40	0.50 0.50	1.50 1.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n or $\overline{Q}_n$		0.75 0.75	2.05 2.05	0.75 0.75	1.85 1.85	0.75 0.75	2.05 2.05	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.40 2.40	0.90 0.90	2.40 2.40	0.90 0.90	2.60 2.60	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 2	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns
t_s	Setup time, D_n to $\overline{E}_n$	Waveform 3	0.70		0.70		0.70		ns
t_h	Hold time, $\overline{E}_n$ to D_n	Waveform 3	0.70		0.70		0.70		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	2.10		2.10		2.10		ns
$t_w(L)$	Pulse width Low $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High MR	Waveform 2	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.50 1.50	0.50 0.50	1.40 1.40	0.50 0.50	1.50 1.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n or $\overline{Q}_n$		0.75 0.75	2.05 2.05	0.75 0.75	1.85 1.85	0.75 0.75	2.05 2.05	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.40 2.40	0.90 0.90	2.40 2.40	0.90 0.90	2.60 2.60	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 2	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns
t_s	Setup time, D_n to $\overline{E}_n$	Waveform 3	0.70		0.70		0.70		ns
t_h	Hold time, $\overline{E}_n$ to D_n	Waveform 3	0.70		0.70		0.70		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	2.10		2.10		2.10		ns
$t_w(L)$	Pulse width Low $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High MR	Waveform 2	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.30 1.30	0.50 0.50	1.20 1.20	0.50 0.50	1.30 1.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n or $\overline{Q}_n$		0.75 0.75	1.85 1.85	0.75 0.75	1.65 1.65	0.75 0.75	1.85 1.85	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.20 2.20	0.90 0.90	2.20 2.20	0.90 0.90	2.40 2.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 2	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns
t_s	Setup time, D_n to $\overline{E}_n$	Waveform 3	0.60		0.60		0.60		ns
t_h	Hold time, $\overline{E}_n$ to D_n	Waveform 3	0.60		0.60		0.60		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	2.00		2.00		2.00		ns
$t_w(L)$	Pulse width Low $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High MR	Waveform 2	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

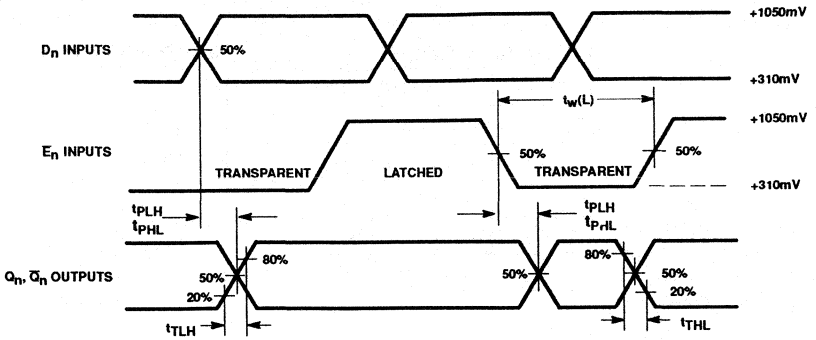
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

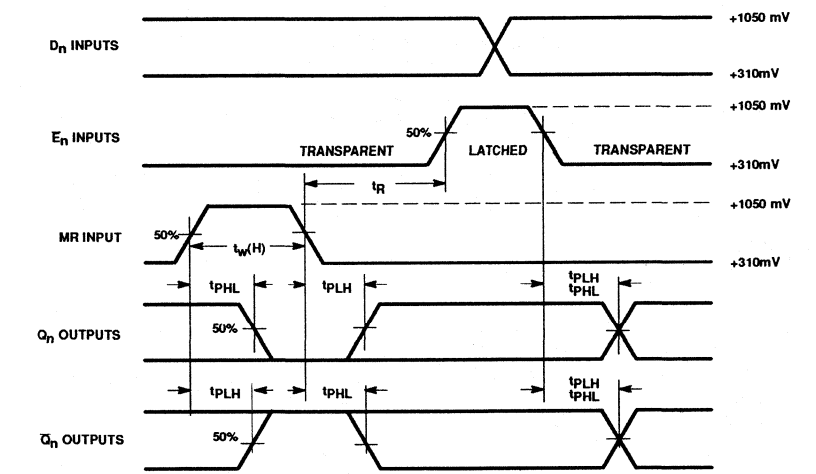
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.30 1.30	0.50 0.50	1.20 1.20	0.50 0.50	1.30 1.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n or $\overline{Q}_n$		0.75 0.75	1.85 1.85	0.75 0.75	1.65 1.65	0.75 0.75	1.85 1.85	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.20 2.20	0.90 0.90	2.20 2.20	0.90 0.90	2.40 2.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 2	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns
t_s	Setup time, D_n to $\overline{E}_n$	Waveform 3	0.60		0.60		0.60		ns
t_h	Hold time, $\overline{E}_n$ to D_n	Waveform 3	0.60		0.60		0.60		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	2.00		2.00		2.00		ns
$t_w(L)$	Pulse width Low $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns
$t_w(H)$	Pulse width High MR	Waveform 2	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

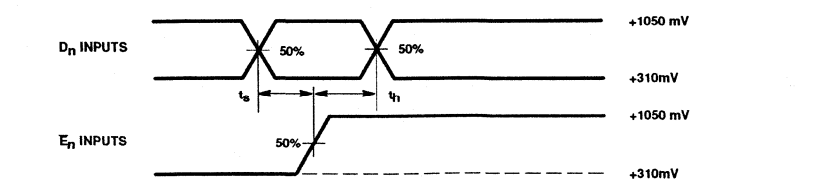
AC WAVEFORMS



Waveform 1. Propagation Delays and Transition Times



Waveform 2. Reset Timing



Waveform 3. Data Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Philips Components

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ECL Products	

100151

Hex D–Type Master–Slave Flip–Flop

FEATURES

- **Typical propagation delay: 1.7ns**
- **Typical supply current ($-I_{EE}$): 137mA**

DESCRIPTION

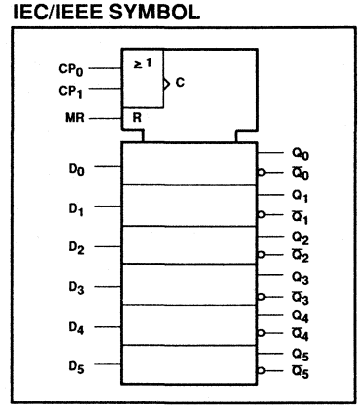
The 100151 contains six flip–flops with Complement and True data outputs, a master reset (MR) and a pair of common clock inputs. Data enters the flip–flop on the Low–to–High transition of one of two clock inputs.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	Data Inputs
CP_0, CP_1	Common Clock Inputs
MR	Master Reset Input
$Q_0 - Q_5$	True Data Outputs
$\overline{Q}_0 - \overline{Q}_5$	Complementary Data Outputs

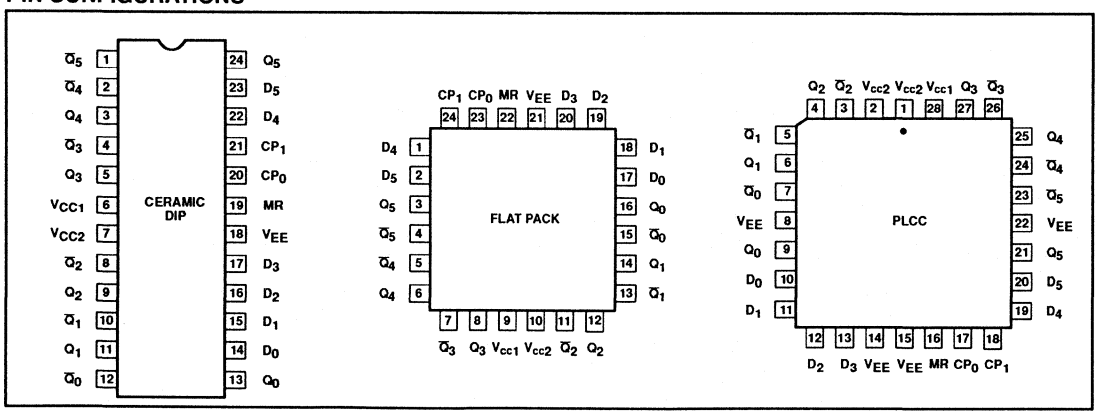
IEC/IEEE SYMBOL



ORDERING INFORMATION

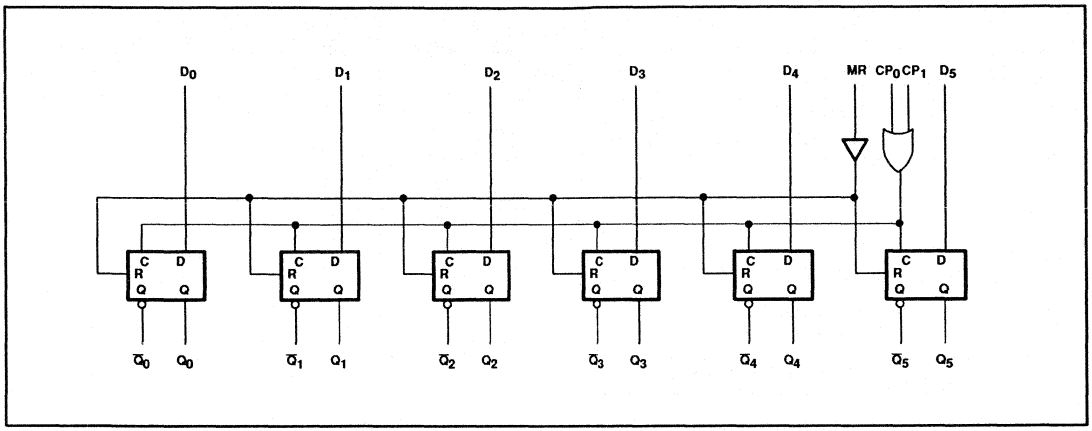
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100151F
24–Pin Ceramic Flat Pack	100151Y
28–Pin PLCC	100151A

PIN CONFIGURATIONS



Flip–Flop 100151

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
D_n	CP_0	CP_1	MR	$\overline{Q}_n$	Q_n
H	L	↑	L	L	H
L	L	↑	L	H	L
H	↑	L	L	L	H
L	↑	L	L	H	L
X	X	H	L	NC	NC
X	H	X	L	NC	NC
X	X	X	H	H	L
X	L	L	L	NC	NC

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
NC = No change
↑ = Low–to–High transition

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

V_{CC1} = V_{CC2} = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to input input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	MR	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					450	µA
		D_n						340	µA
		$\overline{E}_n$						520	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			98	137	210	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.

NOTES (CONTINUED):

3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1	375		375		375		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.20 2.20	0.80 0.80	2.20 2.20	0.90 0.90	2.40 2.40	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveform 2	0.80 0.80	2.90 2.90	0.80 0.80	3.00 3.00	0.90 0.90	3.10 3.10	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.70 1.70	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time, D_n to CP_n	Waveform 2	0.70		0.70		0.70		ns
t_h	Hold time, CP_n to D_n		0.70		0.70		0.70		ns
t_R	Release time, MR to CP_n		2.30		2.30		2.30		ns
t_w(H)	Pulse width CP_n, MR	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1	375		375		375		
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.20 2.20	0.80 0.80	2.20 2.20	0.90 0.90	2.40 2.40	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveform 2	0.80 0.80	2.90 2.90	0.80 0.80	3.00 3.00	0.90 0.90	3.10 3.10	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.70 1.70	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time, D_n to CP_n	Waveform 2	0.95		0.90		0.95		ns
t_h	Hold time, CP_n to D_n		0.70		0.70		0.70		ns
t_R	Release time, MR to CP_n		2.30		2.30		2.30		ns
t_wH)	Pulse width CP_n, MR	Waveforms 1,2	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1	375		375		375		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.00 2.00	0.80 0.80	2.00 2.00	0.90 0.90	2.20 2.20	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveform 2	0.80 0.80	2.70 2.70	0.80 0.80	2.80 2.80	0.90 0.90	2.90 2.90	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.70 1.70	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time, D_n to CP_n	Waveform 2	0.60		0.60		0.60		ns
t_h	Hold time, CP_n to D_n		0.60		0.60		0.60		ns
t_R	Release time, MR to CP_n		2.20		2.20		2.50		ns
$t_w(H)$	Pulse width CP_n, MR	Waveforms 1,2	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

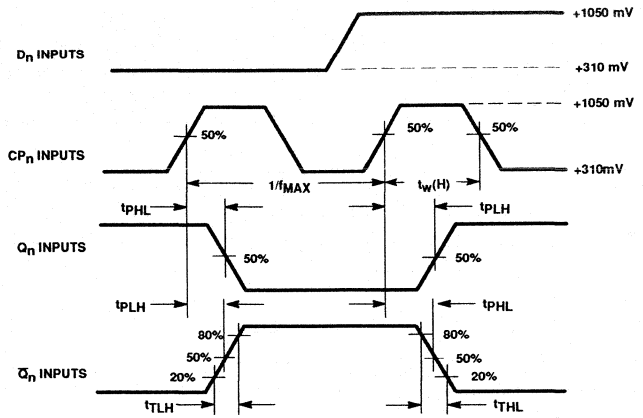
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

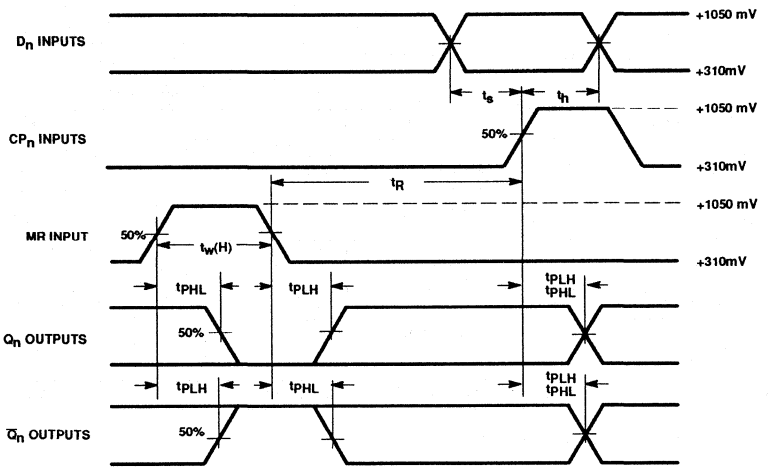
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1	375		375		375		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveforms 1,2	0.80 0.80	2.00 2.00	0.80 0.80	2.00 2.00	0.90 0.90	2.20 2.20	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n or $\overline{Q}_n$	Waveform 2	0.80 0.80	2.70 2.70	0.80 0.80	2.80 2.80	0.90 0.90	2.90 2.90	ns ns
t_{TLH} t_{THL}	Transition time Q_n or $\overline{Q}_n$	Waveform 1	0.45 0.45	1.70 1.70	0.45 0.45	1.60 1.60	0.45 0.45	1.70 1.70	ns ns
t_s	Setup time, D_n to CP_n	Waveform 2	0.75		0.70		0.75		ns
t_h	Hold time, CP_n to D_n		0.60		0.60		0.60		ns
t_R	Release time, MR to CP_n		2.20		2.20		2.50		ns
$t_w(H)$	Pulse width CP_n, MR	Waveforms 1,2	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



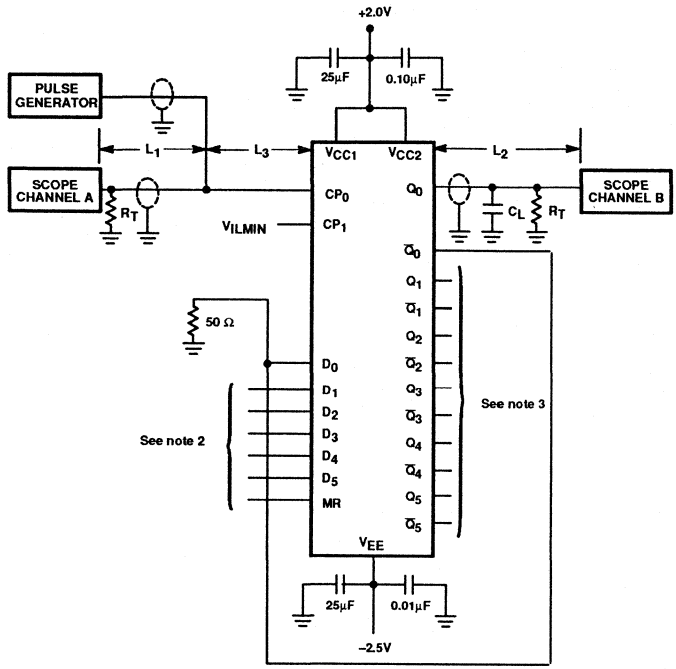
Waveform 1. Propagation Delays and Transition Times



Waveform 2. Reset, Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

SHIFT FREQUENCY TEST CIRCUIT



NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

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Status	Product Specification
ECL Products	

100155
Quad 2–Way Multiplexer–Latch

FEATURES

- **Typical propagation delay: 1.1ns**
- **Typical supply current ($-I_{EE}$): 93mA**

DESCRIPTION

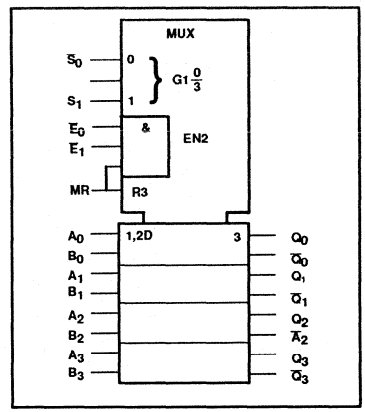
The 100155 is a multiplexer that switches one of two 4–bit inputs, A or B, through a latch, to the outputs (Q_n, $\overline{Q}_n$). This part can also perform an OR function on A and B. The select lines $\overline{S}_0$ and S_1 decide whether word A, word B, or A + B will be sent to the latch. When enables $\overline{E}_0$ and $\overline{E}_1$ are Low, the latch presents the selected input word to the outputs (Q_n, $\overline{Q}_n$). When either $\overline{E}_0$ or $\overline{E}_1$ go High, the data currently at the outputs are latched. If the Master Reset line (MR) is High, Q will be Low, and $\overline{Q}$ will be High regardless of the level of the other outputs.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_3$, $B_0 - B_3$	Data inputs
$\overline{E}_0$, $\overline{E}_1$	Enable inputs
$\overline{S}_0$, S_1	Data select inputs
MR	Master reset inputs
$Q_0 - Q_3$	True data outputs
$\overline{Q}_0 - \overline{Q}_3$	Complemetary data outputs

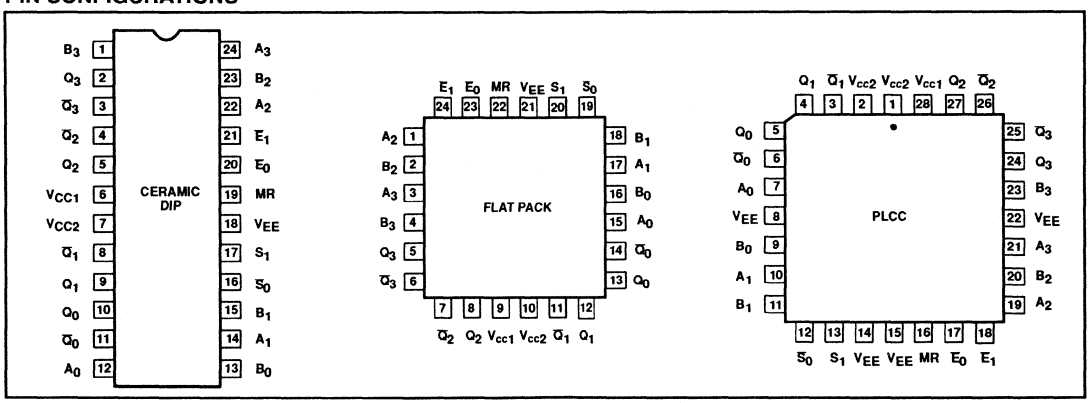
IEC/IEEE SYMBOL



ORDERING INFORMATION

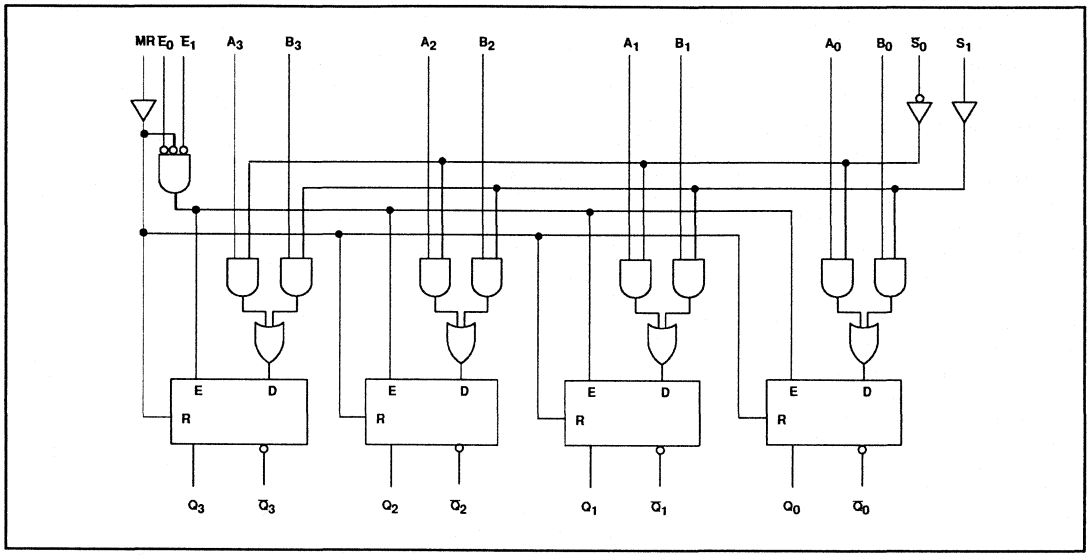
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100155F
24–Pin Ceramic Flat Pack	100155Y
28–Pin PLCC	100155A

PIN CONFIGURATIONS



Multiplexer–Latch 100155

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS	
Reset	Enable		Select		Data			
MR	$\overline{E}_0$	$\overline{E}_1$	$\overline{S}_0$	S_1	A_n	B_n	Q_n	$\overline{Q}_n$
H	X	X	X	X	X	X	L	H
L	L	L	H	H	X	H	H	L
L	L	L	H	H	X	L	L	H
L	L	L	L	L	H	X	H	L
L	L	L	L	L	L	X	L	H
L	L	L	H	L	X	X	L	H
L	L	L	L	H	X	H	H	L
L	L	L	L	H	H	X	H	L
L	L	L	L	H	L	L	L	H
L	H	X	X	X	X	X	Latched*	Latched*
L	X	H	X	X	X	X	Latched*	Latched*

NOTES:
* = Signal level present on latch outputs just before rising transition of enable line is held on latch outputs.
H = High voltage level
L = Low voltage level
X = Don't care
NC = No change

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electyrical characteristics will vary slightly from their specified values.

Multiplexer–Latch 100155

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	$\overline{S}_0$, S_1		One input under test at V_{IHMAX}, other inputs at V_{ILMIN}.				220	µA
		E_0, $\overline{E}_1$	$\overline{S}_0$ at V_{ILMIN}., S_1 at V_{IHMAX}.					350	µA
		A_n, B_n						340	µA
		MR						430	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}, other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			66	93	133	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_n, $\overline{Q}_n$	Waveform 1	0.50 0.50	1.90 1.90	0.60 0.60	1.85 1.85	0.50 0.50	1.90 1.90	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 to Q_n, $\overline{Q}_n$		1.50 1.50	3.50 3.50	1.50 1.50	3.40 3.40	1.50 1.50	3.50 3.50	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to Q_n, $\overline{Q}_n$	Waveform 1,2	0.90 0.90	2.50 2.50	1.00 1.00	2.40 2.40	1.00 1.00	2.50 2.50	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	0.90 0.90	3.00 3.00	0.90 0.90	2.90 2.90	0.90 0.90	3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1	0.60 0.60	2.20 2.20	0.60 0.60	2.10 2.10	0.45 0.45	2.20 2.20	ns ns
t_s	Setup time, A_n, B_n to E_n	Waveform 3	0.90		0.90		0.90		ns
t_h	Hold time, E_n to A_n, B_n		0.40		0.40		0.40		ns
t_s	Setup time, $\overline{S}_0$, S_1 to E_n		2.40		2.40		2.70		ns
t_h	Hold time, E_n to $\overline{S}_0$, S_1		–0.6		–0.6		–0.6		ns
t_R	Release time, MR to E_n	Waveform 2	1.50		1.50		1.50		ns
$t_w(H)$	Pulse width, MR	Waveform 2	2.50		2.50		2.50		ns
$t_w(L)$	Pulse width, E_n	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_n, $\overline{Q}_n$	Waveform 1	0.50 0.50	1.90 1.90	0.60 0.60	1.85 1.85	0.50 0.50	1.90 1.90	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 to Q_n, $\overline{Q}_n$		1.50 1.50	3.50 3.50	1.50 1.50	3.40 3.40	1.50 1.50	3.50 3.50	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.90 0.90	2.50 2.50	1.00 1.00	2.40 2.40	1.00 1.00	2.50 2.50	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	0.90 0.90	3.00 3.00	0.90 0.90	2.90 2.90	0.90 0.90	3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1	0.60 0.60	2.20 2.20	0.60 0.60	2.10 2.10	0.45 0.45	2.20 2.20	ns ns
t_s	Setup time, A_n, B_n to E_n	Waveform 3	0.90		0.90		0.90		ns
t_h	Hold time, E_n to A_n, B_n		0.40		0.40		0.40		ns
t_s	Setup time, S_0, S_1 to E_n		2.40		2.40		2.70		ns
t_h	Hold time, E_n to S_0, S_1		–0.6		–0.6		–0.6		ns
t_R	Release time, MR to E_n	Waveform 2	1.50		1.50		1.50		ns
$t_w(H)$	Pulse width, MR	Waveform 2	2.50		2.50		2.50		ns
$t_w(L)$	Pulse width, E_n	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_n, $\overline{Q}_n$	Waveform 1	0.50 0.50	1.70 1.70	0.60 0.60	1.65 1.65	0.50 0.50	1.70 1.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 to Q_n, $\overline{Q}_n$		1.50 1.50	3.30 3.30	1.50 1.50	3.20 3.20	1.50 1.50	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.90 0.90	2.30 2.30	1.00 1.00	2.20 2.20	1.00 1.00	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	0.90 0.90	2.80 2.80	0.90 0.90	2.70 2.70	0.90 0.90	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1	0.60 0.60	2.20 2.20	0.60 0.60	2.10 2.10	0.45 0.45	2.20 2.20	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}_n$	Waveform 3	0.80		0.80		0.80		ns
t_h	Hold time, $\overline{E}_n$ to A_n, B_n		0.30		0.30		0.30		ns
t_s	Setup time, $\overline{S}_0$, S_1 to $\overline{E}_n$		2.60		2.60		2.60		ns
t_h	Hold time, $\overline{E}_n$ to $\overline{S}_0$, S_1		–0.8		–0.8		–0.8		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	1.40		1.40		1.40		ns
$t_{w(H)}$	Pulse width, MR	Waveform 2	2.50		2.50		2.50		ns
$t_{w(L)}$	Pulse width, $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

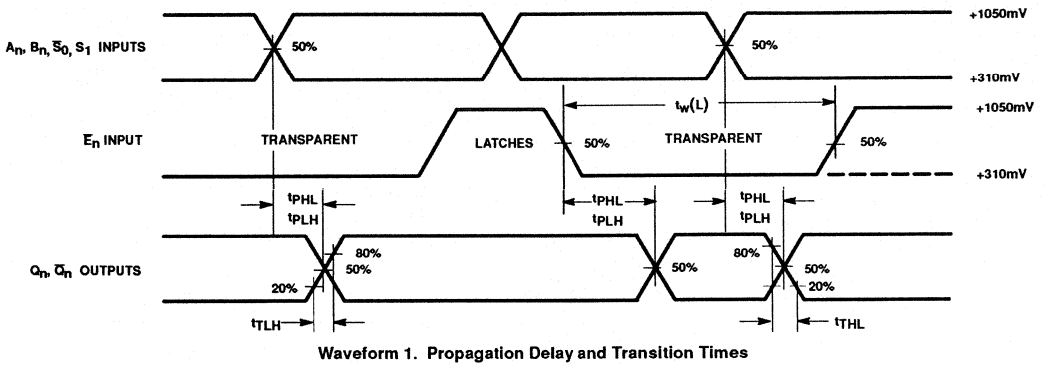
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

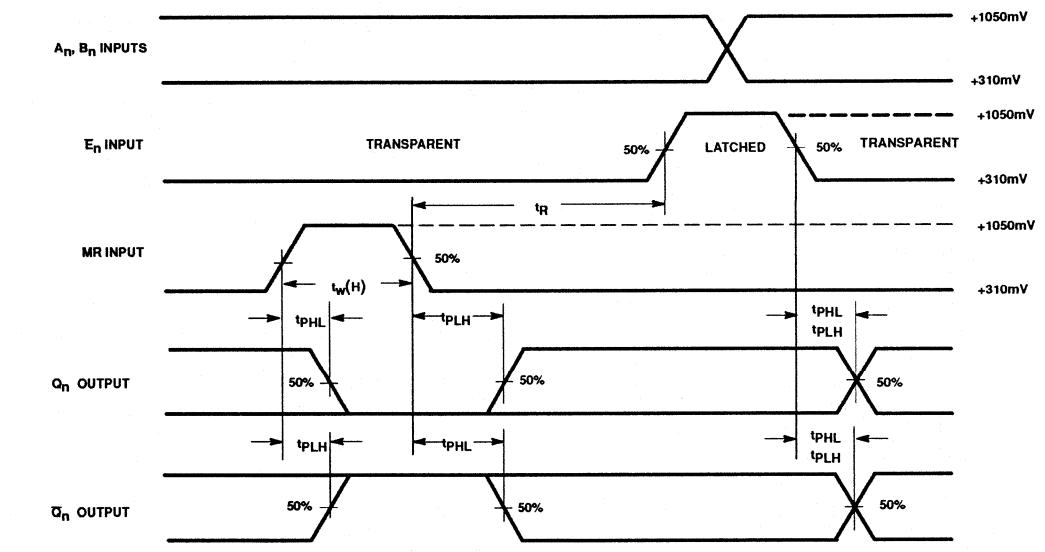
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_n, $\overline{Q}_n$	Waveform 1	0.50 0.50	1.70 1.70	0.60 0.60	1.65 1.65	0.50 0.50	1.70 1.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 to Q_n, $\overline{Q}_n$		1.50 1.50	3.30 3.30	1.50 1.50	3.20 3.20	1.50 1.50	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n, $\overline{Q}_n$	Waveforms 1,2	0.90 0.90	2.30 2.30	1.00 1.00	2.20 2.20	1.00 1.00	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n, $\overline{Q}_n$	Waveform 2	0.90 0.90	2.80 2.80	0.90 0.90	2.70 2.70	0.90 0.90	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1	0.60 0.60	2.20 2.20	0.60 0.60	2.10 2.10	0.45 0.45	2.20 2.20	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}_n$	Waveform 3	0.80		0.80		0.80		ns
t_h	Hold time, $\overline{E}_n$ to A_n, B_n		0.30		0.30		0.30		ns
t_s	Setup time, $\overline{S}_0$, S_1 to $\overline{E}_n$		2.60		2.60		2.60		ns
t_h	Hold time, $\overline{E}_n$ to $\overline{S}_0$, S_1		–0.8		–0.8		–0.8		ns
t_R	Release time, MR to $\overline{E}_n$	Waveform 2	1.40		1.40		1.40		ns
$t_{w(H)}$	Pulse width, MR	Waveform 2	2.50		2.50		2.50		ns
$t_{w(L)}$	Pulse width, $\overline{E}_n$	Waveform 1	2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

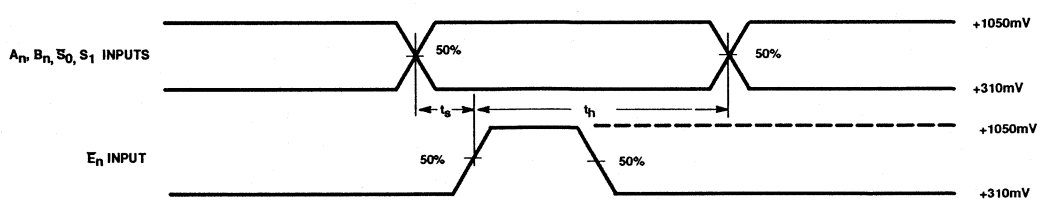
AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times



Waveform 2. Reset Timing



Waveform 3. Setup and Hold times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

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ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100158

Shift Matrix

FEATURES

- **Typical propagation delay: 1.9ns**
- **Typical supply current ($-I_{EE}$): 118mA**

DESCRIPTION

The 100158 contains a combinatorial network which performs the function of an 8–bit Shift Matrix. Three control lines (S_n) are internally decoded to define the number of places which an 8–bit word, present at the inputs (D_n), is shifted to the right. The shifted word appears on the outputs Q_n. A Mode Control is provided which, if Low, forces Low all outputs to the left of the one that contains D_7. This operation is sometimes referred to as low backfill. If M is High, a circular shift is performed, such that D_0 appears at the output just to the left of the one that contains D_7. This operation is commonly referred to as barrel shifting.

All unused inputs can be left open due to integrated pull–down resistors.

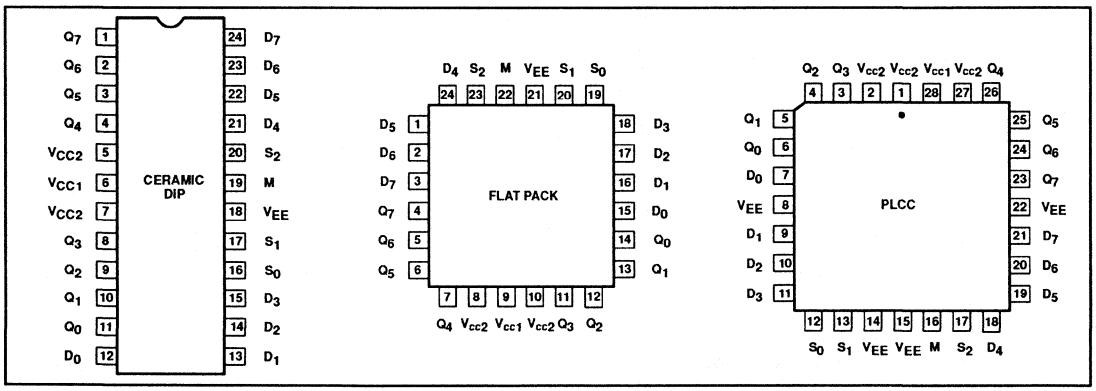
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
$S_0 - S_2$	Select Inputs
M	Mode Control Input
$Q_0 - Q_7$	Data Outputs

ORDERING INFORMATION

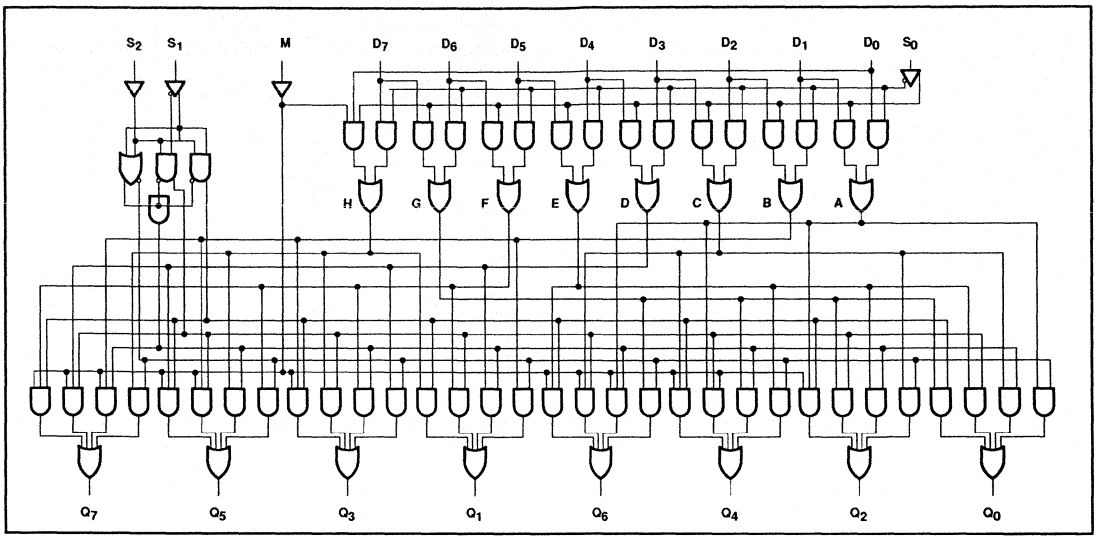
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100158F
24–Pin Ceramic Flat Pack	100158Y
28–Pin PLCC	100158A

PIN CONFIGURATIONS



Shift Matrix 100158

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS							
M	S_2	S_1	S_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
X	L	L	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	L	L	H	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1
L	L	H	L	L	L	D_7	D_6	D_5	D_4	D_3	D_2
L	L	H	H	L	L	L	D_7	D_6	D_5	D_4	D_3
L	H	L	L	L	L	L	L	D_7	D_6	D_5	D_4
L	H	L	H	L	L	L	L	L	D_7	D_6	D_5
L	H	H	L	L	L	L	L	L	L	D_7	D_6
L	H	H	H	L	L	L	L	L	L	L	D_7
H	L	L	H	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1
H	L	H	L	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2
H	L	H	H	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3
H	H	L	L	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4
H	H	L	H	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5
H	H	H	L	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6
H	H	H	H	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified·

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					220	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}			84	118	205	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.10 1.10	3.00 3.00	1.10 1.10	2.90 2.90	1.10 1.10	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n		1.15 1.15	4.40 4.40	1.25 1.25	4.40 4.40	1.15 1.15	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n		1.70 1.70	4.50 4.50	1.70 1.70	4.50 4.50	1.70 1.70	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.10 1.10	3.00 3.00	1.10 1.10	2.90 2.90	1.10 1.10	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n		1.15 1.15	4.40 4.40	1.25 1.25	4.40 4.40	1.15 1.15	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n		1.70 1.70	4.50 4.50	1.70 1.70	4.50 4.50	1.70 1.70	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.10 1.10	2.80 2.80	1.10 1.10	2.70 2.70	1.10 1.10	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n		1.15 1.15	4.20 4.20	1.25 1.25	4.20 4.20	1.15 1.15	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n		1.70 1.70	4.30 4.30	1.70 1.70	4.30 4.30	1.70 1.70	4.60 4.60	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

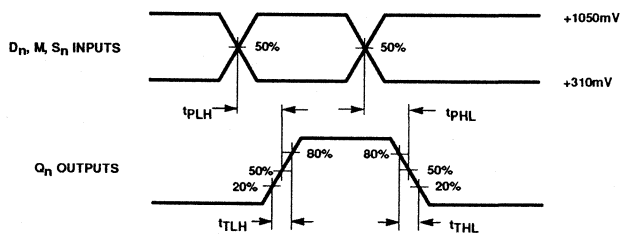
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.10 1.10	2.80 2.80	1.10 1.10	2.70 2.70	1.10 1.10	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n		1.15 1.15	4.20 4.20	1.25 1.25	4.20 4.20	1.15 1.15	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n		1.70 1.70	4.30 4.30	1.70 1.70	4.30 4.30	1.70 1.70	4.60 4.60	ns ns
t_{TLH} t_{THL}	Transition time Q_n		0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	0.50 0.50	2.20 2.20	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–0625
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100160

Dual Parity Generator/8–Bit Comparator

FEATURES

- **Typical propagation delay: 1.8ns**
- **Typical supply current ($-I_{EE}$): 78mA**

DESCRIPTION

The 100160 acts as both a dual parity bit generator and an eight–bit comparator. The part accepts two eight–bit words as inputs (DA and DB). The parity bit QA (or QB) takes on a logic level such that the number of bits among DA and QA (DB and QB) that are high is odd. Thus the nine–bit word comprising DA and QA (DB and QB) possesses the property of odd parity. The Expansion Input XA (XB) can be used to expand the allowable word size of DA (or DB). Then parity bits can be generated for input words of 16 bits or more. The comparator function determines whether two 8–bit input words are equivalent or not. If each pair of Exclusive–OR gate inputs agree, then the comparator output $\overline{C}$ goes low. (See Logic Diagram.)

All unused inputs can be left open due to integrated pull–down resistors.

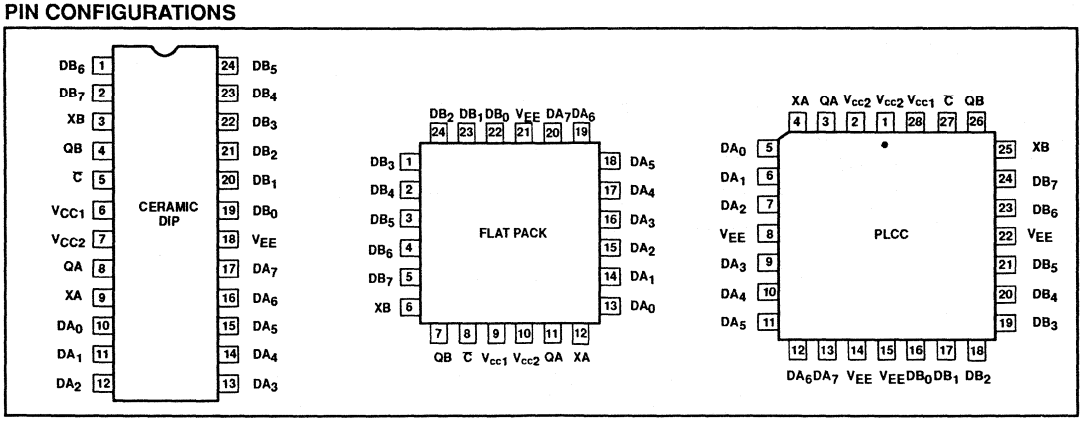
PIN DESCRIPTION

PINS	DESCRIPTION
DA_n, DB_n	Data Inputs
XA, XB	Expansion Inputs
$\overline{C}$	Compare Output
QA, QB	Odd Parity Outputs

ORDERING INFORMATION

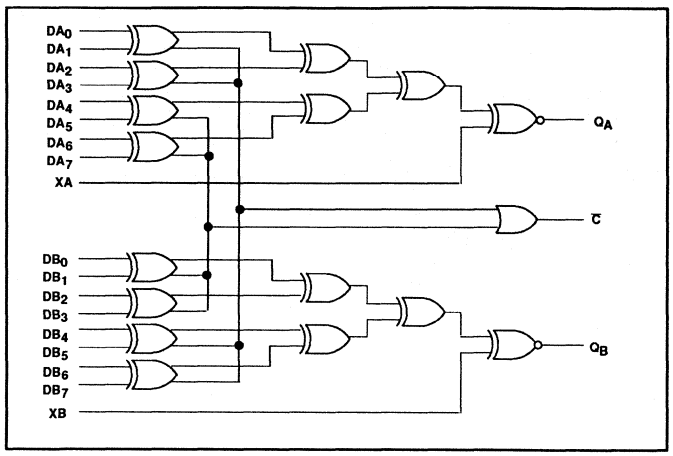
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100160F
24–Pin Ceramic Flat Pack	100160Y
28–Pin PLCC	100160A

PIN CONFIGURATIONS



Parity Generator / Comparator 100160

LOGIC DIAGRAM



FUNCTION TABLE FOR PARITY BIT GENERATION

INPUTS	OUTPUT
DA_n	QA
DB_n	QB
Odd number of bits are high	L
Even number of bits are high	H

NOTES:
H = High voltage level
L = Low voltage level

FUNCTION TABLE FOR COMPARATOR ACTION

INPUTS	OUTPUT
DAn and DBn	$\overline{C}$
$DA_0 = DA_1$, and $DA_2 = DA_3$ and $DA_4 = DA_5$ and $DA_6 = DA_7$ and $DB_0 = DB_1$, and $DB_2 = DB_3$ and $DB_4 = DB_5$ and $DB_6 = DB_7$	L
All other combinations	H

NOTES:
H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, $T_A = 0°C$ to $+85°C$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0 ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					240	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}			57	78	115	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to QA, QB	Waveform 1	1.30 1.30	4.30 4.30	1.30 1.30	4.10 4.10	1.30 1.30	4.30 4.30	ns ns
t_{PLH} t_{PHL}	Propagation delay XA, XB to QA, QB		0.50 0.50	1.60 1.60	0.50 0.50	1.60 1.60	0.50 0.50	1.60 1.60	ns ns
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to $\overline{C}$		1.20 1.20	3.30 3.30	1.20 1.20	3.10 3.10	1.20 1.20	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time QA, QB, $\overline{C}$		0.40 0.40	1.70 1.70	0.40 0.40	1.65 1.65	0.40 0.40	1.65 1.65	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to QA, QB	Waveform 1	1.30 1.30	4.30 4.30	1.30 1.30	4.10 4.10	1.30 1.30	4.30 4.30	ns ns
t_{PLH} t_{PHL}	Propagation delay XA, XB to QA, QB		0.50 0.50	1.60 1.60	0.50 0.50	1.60 1.60	0.50 0.50	1.60 1.60	ns ns
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to $\overline{C}$		1.20 1.20	3.30 3.30	1.20 1.20	3.10 3.10	1.20 1.20	3.30 3.30	ns ns
t_{TLH} t_{THL}	Transition time QA, QB, $\overline{C}$		0.40 0.40	1.70 1.70	0.40 0.40	1.65 1.65	0.40 0.40	1.65 1.65	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{groind}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to QA, QB	Waveform 1	1.30 1.30	4.10 4.10	1.30 1.30	3.90 3.90	1.30 1.30	4.10 4.10	ns ns
t_{PLH} t_{PHL}	Propagation delay XA, XB to QA, QB		0.50 0.50	1.40 1.40	0.50 0.50	1.40 1.40	0.50 0.50	1.40 1.40	ns ns
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to $\overline{C}$		1.20 1.20	3.10 3.10	1.20 1.20	2.90 2.90	1.20 1.20	3.10 3.10	ns ns
t_{TLH} t_{THL}	Transition time QA, QB, $\overline{C}$		0.40 0.40	1.70 1.70	0.40 0.40	1.65 1.65	0.40 0.40	1.65 1.65	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

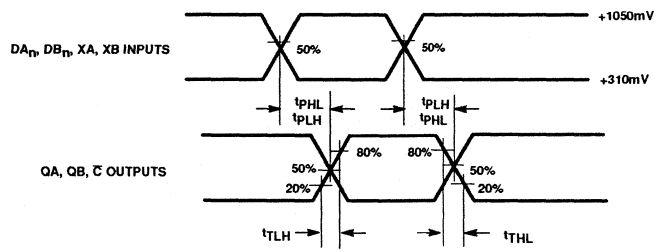
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to QA, QB	Waveform 1	1.30 1.30	4.10 4.10	1.30 1.30	3.90 3.90	1.30 1.30	4.10 4.10	ns ns
t_{PLH} t_{PHL}	Propagation delay XA, XB to QA, QB		0.50 0.50	1.40 1.40	0.50 0.50	1.40 1.40	0.50 0.50	1.40 1.40	ns ns
t_{PLH} t_{PHL}	Propagation delay DA_n, DB_n to $\overline{C}$		1.20 1.20	3.10 3.10	1.20 1.20	2.90 2.90	1.20 1.20	3.10 3.10	ns ns
t_{TLH} t_{THL}	Transition time QA, QB, $\overline{C}$		0.40 0.40	1.70 1.70	0.40 0.40	1.65 1.65	0.40 0.40	1.65 1.65	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Philips Components

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Status	Product Specification
ECL Products	

100163

Dual 8–Input Multiplexer

FEATURES

- **Typical propagation delay: 1.25ns**
- **Typical supply current ($-I_{EE}$): 125mA**

DESCRIPTION

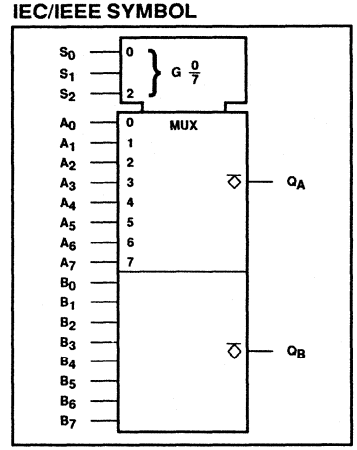
The 100163 circuit is a dual 8–input multiplexer. The three data select inputs ($S_0 - S_2$) switch one of the eight data inputs in each multiplexer to its corresponding output.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_7$, $B_0 - B_7$	Data Inputs
$S_0 - S_2$	Data Select Inputs
Q_A, Q_B	Data Outputs

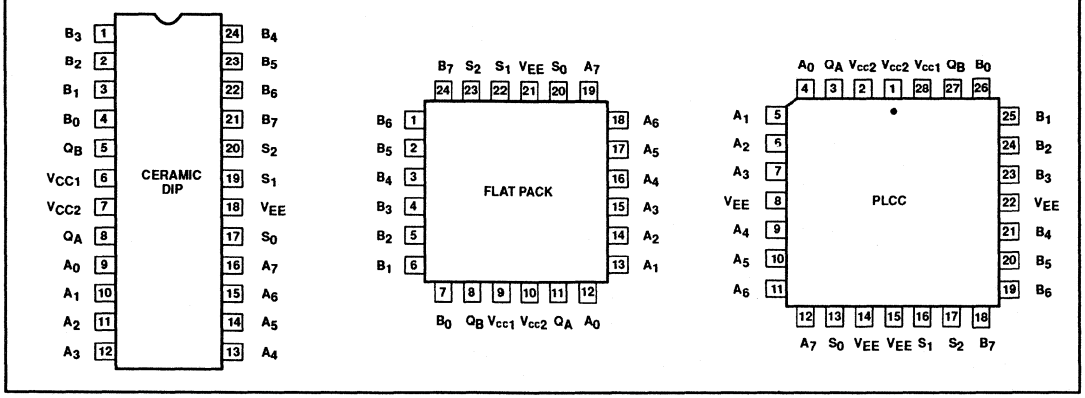
IEC/IEEE SYMBOL



ORDERING INFORMATION

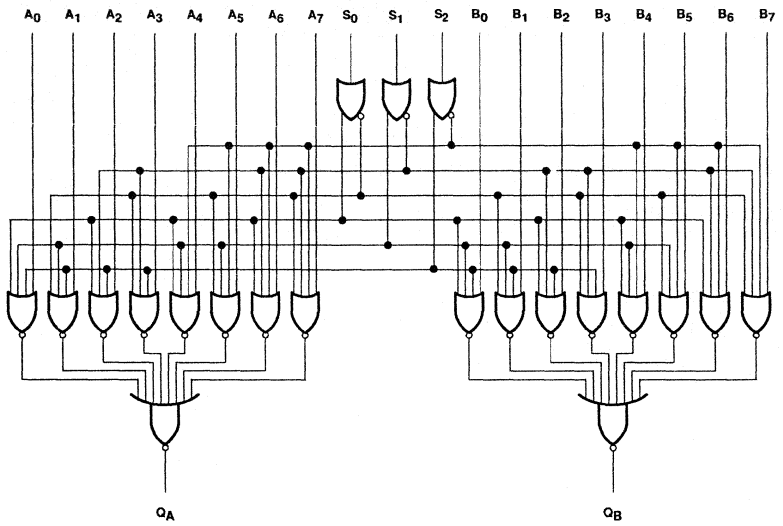
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100163F
24–Pin Ceramic Flat Pack	100163Y
28–Pin PLCC	100163A

PIN CONFIGURATIONS



Multiplexer 100163

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS										OUTPUTS
Select			Data							
S_2	S_1	S_0	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	Q_A Q_B
L	L	L	X	X	X	X	X	X	X	L	L
L	L	L	X	X	X	X	X	X	X	H	H
L	L	H	X	X	X	X	X	X	L	X	L
L	L	H	X	X	X	X	X	X	H	X	H
L	H	L	X	X	X	X	X	L	X	X	L
L	H	L	X	X	X	X	X	H	X	X	H
L	H	H	X	X	X	X	L	X	X	X	L
L	H	H	X	X	X	X	H	X	X	X	H
H	L	L	X	X	X	L	X	X	X	X	L
H	L	L	X	X	X	H	X	X	X	X	H
H	L	H	X	X	L	X	X	X	X	X	L
H	L	H	X	X	H	X	X	X	X	X	H
H	H	L	X	L	X	X	X	X	X	X	L
H	H	L	X	H	X	X	X	X	X	X	H
H	H	H	L	X	X	X	X	X	X	X	L
H	H	H	H	X	X	X	X	X	X	X	H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

Multiplexer | 100163

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	S_n	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					265	µA
		A_n, B_n						340	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			76	125	161	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.2V$ to $-4.8V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_A, Q_B	Waveform 1	0.55 0.55	1.90 1.90	0.60 0.60	1.90 1.90	0.65 0.65	2.00 2.00	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_A, Q_B		1.10 1.10	2.80 2.80	1.10 1.10	2.80 2.80	1.20 1.20	3.10 3.10	ns ns
t_{TLH} t_{THL}	Transition time Q_A, Q_B		0.50 0.50	1.75 1.75	0.50 0.50	1.70 1.70	0.50 0.50	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_A, Q_B	Waveform 1	0.55 0.55	1.90 1.90	0.60 0.60	1.90 1.90	0.65 0.65	2.00 2.00	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_A, Q_B		1.10 1.10	2.80 2.80	1.10 1.10	2.80 2.80	1.20 1.20	3.10 3.10	ns ns
t_{TLH} t_{THL}	Transition time Q_A, Q_B		0.50 0.50	1.75 1.75	0.50 0.50	1.70 1.70	0.50 0.50	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.2V$ to $-4.8V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_A, Q_B	Waveform 1	0.55 0.55	1.70 1.70	0.60 0.60	1.70 1.70	0.65 0.65	1.80 1.80	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_A, Q_B		1.10 1.10	2.60 2.60	1.10 1.10	2.60 2.60	1.20 1.20	2.90 2.90	ns ns
t_{TLH} t_{THL}	Transition time Q_A, Q		0.50 0.50	1.75 1.75	0.50 0.50	1.70 1.70	0.50 0.50	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

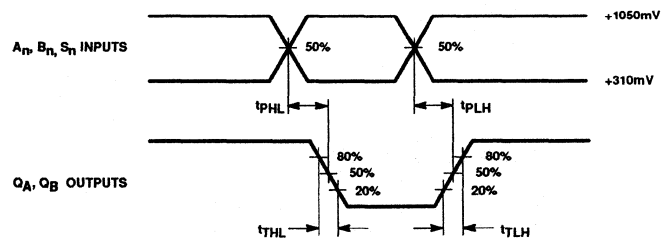
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to Q_A, Q_B	Waveform 1	0.55 0.55	1.70 1.70	0.60 0.60	1.70 1.70	0.65 0.65	1.80 1.80	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_A, Q_B		1.10 1.10	2.60 2.60	1.10 1.10	2.60 2.60	1.20 1.20	2.90 2.90	ns ns
t_{TLH} t_{THL}	Transition time Q_A, Q_B		0.50 0.50	1.75 1.75	0.50 0.50	1.70 1.70	0.50 0.50	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Philips Components

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Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100164

16–Input Multiplexer

FEATURES

- **Typical propagation delay: 1.60ns**
- **Typical supply current ($-I_{EE}$): 71mA**

DESCRIPTION

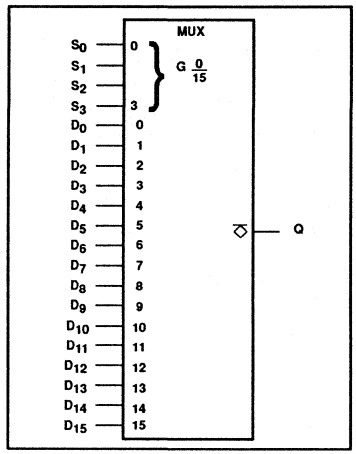
The 100164 is a 16–input multiplexer. Four data select inputs (S_n) choose one of the 16 data inputs (D_n) to be gated to the output (Q).

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_{15}$	Data Inputs
$S_0 - S_3$	Data Select Inputs
Q	Data Output

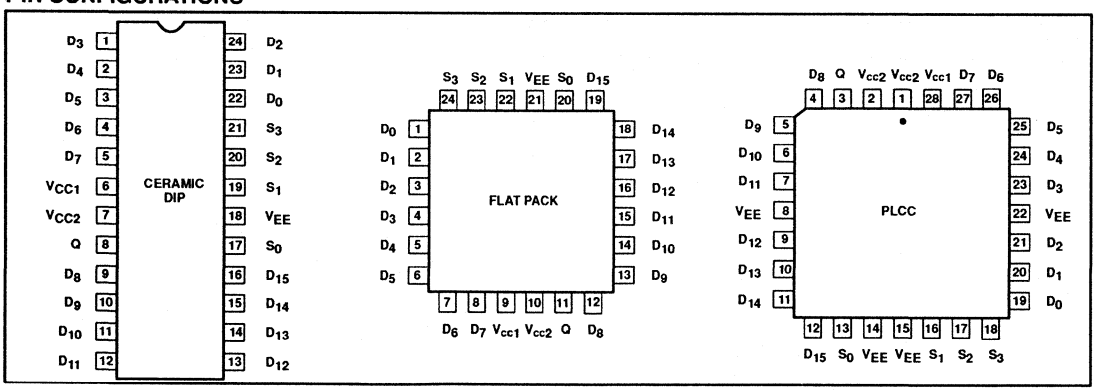
IEC/IEEE SYMBOL



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100164F
24–Pin Ceramic Flat Pack	100164Y
28–Pin PLCC	100164A

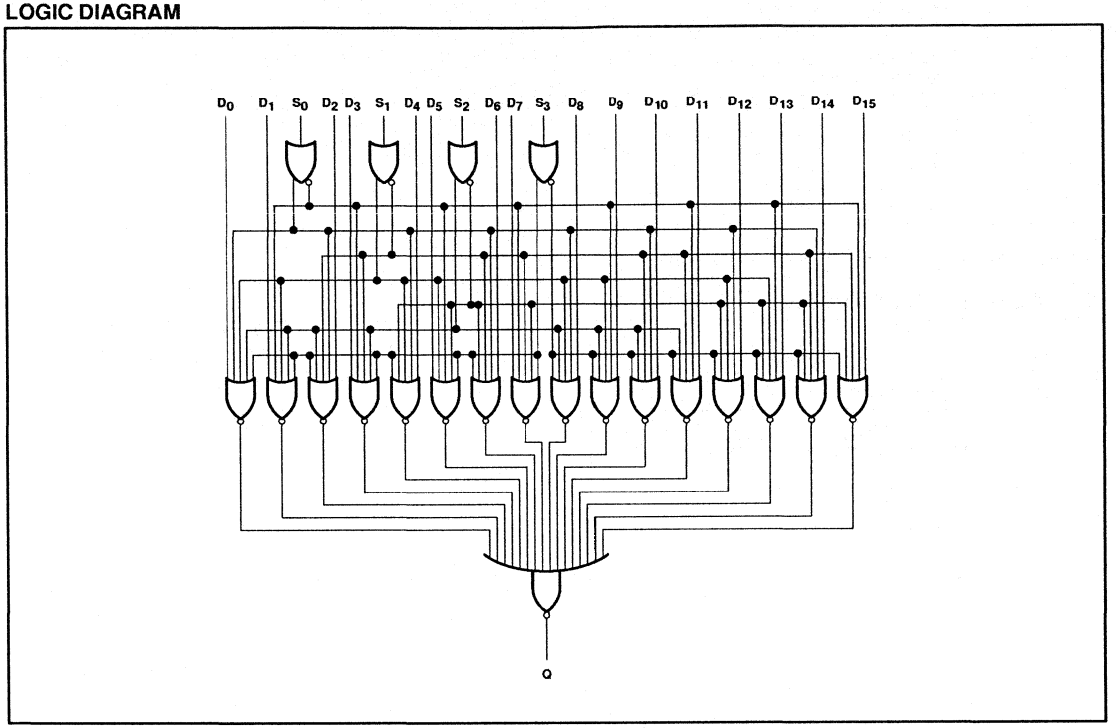
PIN CONFIGURATIONS



Multiplexer

100164

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS				OUTPUT
S_3	S_2	S_1	S_0	Q
L	L	L	L	D_0
L	L	L	H	D_1
L	L	H	L	D_2
L	L	H	H	D_3
L	H	L	L	D_4
L	H	L	H	D_5
L	H	H	L	D_6
L	H	H	H	D_7
H	L	L	L	D_8
H	L	L	H	D_9
H	L	H	L	D_{10}
H	L	H	H	D_{11}
H	H	L	L	D_{12}
H	H	L	H	D_{13}
H	H	H	L	D_{14}
H	H	H	H	D_{15}

NOTES:
H = High voltage level
L = Low voltage level

Multiplexer 100164

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

Multiplexer | 100164

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	D_n	One input under test at V_{IHMAX}. Other inputs at $V_{IL\,MIN}$.					240	µA
		S_0, S_1						240	µA
		S_2 S_3						240	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			49	71	105	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} =$ ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	Max.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q	Waveform 1	0.80 0.80	2.20 2.20	0.90 0.90	2.35 2.35	0.90 0.90	2.55 2.55	ns ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q		1.45 1.45	3.20 3.20	1.45 1.45	3.20 3.20	1.45 1.45	3.60 3.60	ns ns
t_{PLH} t_{PHL}	Propagation delay S_2, S_3 to Q		1.10 1.10	2.50 2.50	1.10 1.10	2.50 2.50	1.10 1.10	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q		0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} =$ ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	Max.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q	Waveform 1	0.80 0.80	2.20 2.20	0.90 0.90	2.35 2.35	0.90 0.90	2.55 2.55	ns ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q		1.45 1.45	3.20 3.20	1.45 1.45	3.20 3.20	1.45 1.45	3.60 3.60	ns ns
t_{PLH} t_{PHL}	Propagation delay S_2, S_3 to Q		1.10 1.10	2.50 2.50	1.10 1.10	2.50 2.50	1.10 1.10	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time Q		0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} =$ ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	REFERENCE	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	Max.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q	Waveform 1	0.80 0.80	2.00 2.00	0.90 0.90	2.15 2.15	0.90 0.90	2.35 2.35	ns ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q		1.45 1.45	3.00 3.00	1.45 1.45	3.00 3.00	1.45 1.45	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay S_2, S_3 to Q		1.10 1.10	2.30 2.30	1.10 1.10	2.30 2.30	1.10 1.10	2.60 2.60	ns ns
t_{TLH} t_{THL}	Transition time Q		0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

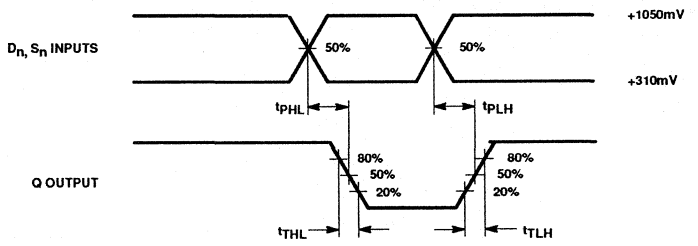
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	Max.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q	Waveform 1	0.80 0.80	2.00 2.00	0.90 0.90	2.15 2.15	0.90 0.90	2.35 2.35	ns ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q		1.45 1.45	3.00 3.00	1.45 1.45	3.00 3.00	1.45 1.45	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay S_2, S_3 to Q		1.10 1.10	2.30 2.30	1.10 1.10	2.30 2.30	1.10 1.10	2.60 2.60	ns ns
t_{TLH} t_{THL}	Transition time Q		0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power andf signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–0628
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100165

Universal Priority Encoder

FEATURES

- **Typical propagation delay: 2.5ns**
- **Typical supply current ($-I_{EE}$): 125mA**

DESCRIPTION

100165 is a Universal Priority Encoder with latches on the inputs. A Mode Control line (M) determines one of two possible modes of operation: When M is High, the device functions as an 8–bit priority encoder. When M is Low, the device operates as two independent 4–bit priority encoders.

In the 8–bit encoder mode, the priority of the data input decreases in going from D_0 to D_7. Thus, D_0 has the high priority and D_7 has the lowest. The bit–pattern on the data outputs ($Q_0 - Q_2$, $\overline{Q}_0 - \overline{Q}_2$) identifies the highest priority data input at a High logic level. For expansion, the Group Signal output GS_0 can be connected to the Output Enable $\overline{OE}$ of another, lower priority 100165. Outputs Q_3, $\overline{Q}_3$ and GS_1 are not used in this mode.

In the dual 4–bit encoder mode, $D_0 - D_3$, Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$, and GS_0 are associated with one encoder; $D_4 - D_7$, Q_2, Q_3, $\overline{Q}_2$, $\overline{Q}_3$, and GS_1 are associated with the other. The priority of the data input decreases in going from D_0 to D_3 (or from D_4 to D_7). A bit–pattern on the data outputs Q_0 and Q_1 (or Q_2 and Q_3) identifies the highest priority data input at a High logic level. For expansion, GS_0 (GS_1) can be connected to the $\overline{OE}$ of another, lower priority 100165.

There is one latch at each data input (D_n). When the Enable input $\overline{E}$ is Low, these latches are transparent. When $\overline{E}$ goes High, the data at the inputs are latched. $\overline{E}$ functions the same way for both modes of operation.

When the Output Enable $\overline{OE}$ is High, $Q_0 - Q_3$ are forced to a Low logic level and GS_n are forced High. $\overline{OE}$ functions the same way for both modes of operation.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

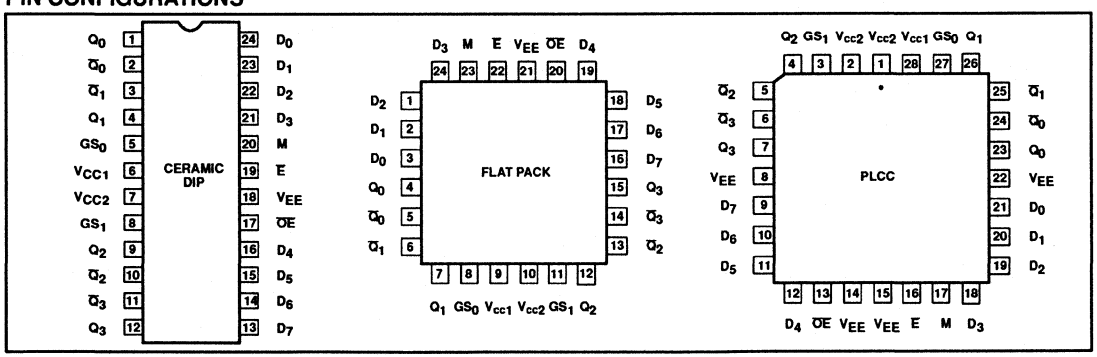
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
M	Mode Control Input
$\overline{E}$	Latch Enable Input (Active Low)
$\overline{OE}$	Output Enable Input (Active Low)
GS_0, GS_1	Group Signal Outputs
$Q_0 - Q_3$	True Data Outputs
$\overline{Q}_0 - \overline{Q}_3$	Complementary Data Outputs

ORDERING INFORMATION

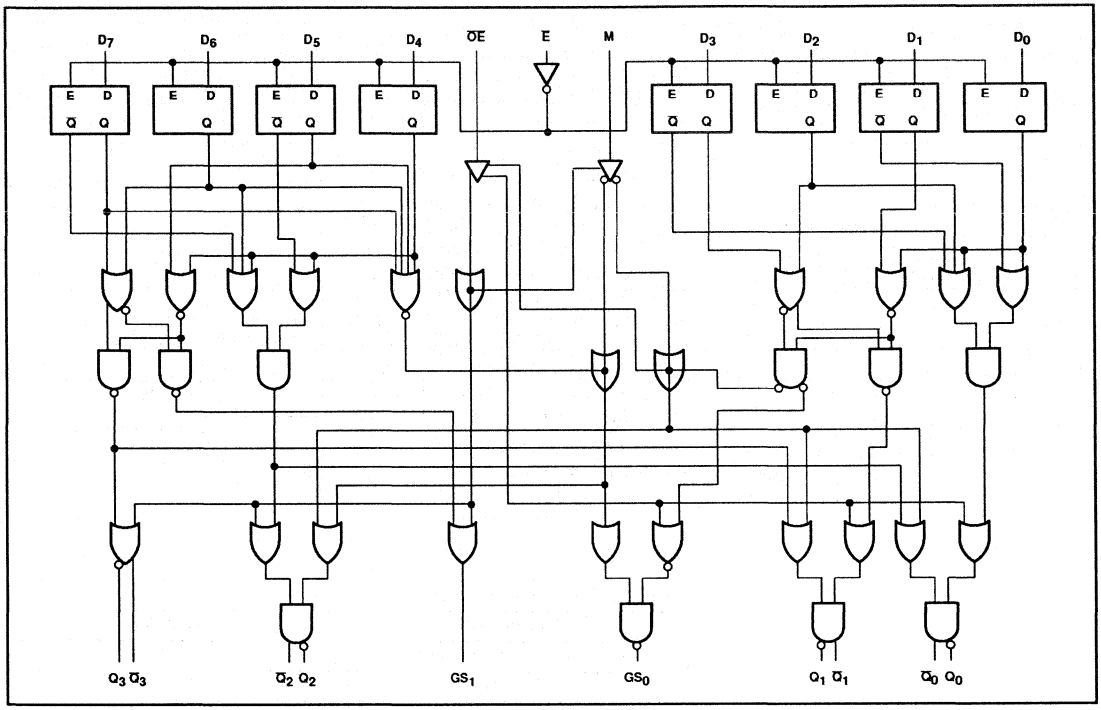
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100165F
24–Pin Ceramic Flat Pack	100165Y
28–Pin PLCC	100165A

PIN CONFIGURATIONS



Encoder 100165

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS											OUTPUTS					
$\overline{E}$	$\overline{OE}$	M	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q_0	Q_1	Q_2	Q_3	GS_0	GS_1
L	L	L	H	X	X	X					L	L			H	
L	L	L	L	H	X	X					H	L			H	
L	L	L	L	L	H	X					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	X	X	X			L	L		H
L	L	L					L	H	X	X			H	L		H
L	L	L					L	L	H	X			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	X	X	X	X	X	X	X	L	L	L	L	H	H
L	L	H	L	H	X	X	X	X	X	X	H	L	L	L	H	H
L	L	H	L	L	H	X	X	X	X	X	L	H	L	L	H	H
L	L	H	L	L	L	H	X	X	X	X	H	H	L	L	H	H
L	L	H	L	L	L	L	H	X	X	X	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	X	X	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	X	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	H	H
H	L	L	X	X	X	X	X	X	X	X	Determined by $D_0 - D_7$ when $\overline{E}$ was Low and M = L					
H	L	H	X	X	X	X	X	X	X	X	Determined by $D_0 - D_7$ when $\overline{E}$ was Low and M = H					

NOTES:

H = High voltage level
L = Low voltage level
X = Don't care
Blank = Not Applicable

Encoder 100165

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					230	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}			77	125	200	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX	MIN.	MAX	MIN.	MAX	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.10 1.10	4.10 4.10	1.10 1.10	4.10 4.10	1.10 1.10	4.60 4.60	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to GS_n		1.10 1.10	4.10 4.10	1.10 1.10	4.10 4.10	1.10 1.10	4.60 4.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Q_n, $\overline{Q}_n$	Waveform 2	1.00 1.00	3.30 3.30	1.00 1.00	3.30 3.30	1.00 1.00	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to GS_n		1.00 1.00	3.30 3.30	1.00 1.00	3.30 3.30	1.00 1.00	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.90 0.90	3.60 3.60	1.00 1.00	3.60 3.60	1.00 1.00	3.80 3.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n, $\overline{Q}_n$, GS_n	Waveforms 1,2	1.40 1.40	4.70 4.70	1.40 1.40	4.60 4.60	1.40 1.40	5.00 5.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to $\overline{E}$	Waveform 3	1.10		1.00		1.10		ns
t_h	Hold time $\overline{E}$ to D_n		1.30		1.30		1.30		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX	MIN.	MAX	MIN.	MAX	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.10 1.10	4.10 4.10	1.10 1.10	4.10 4.10	1.10 1.10	4.60 4.60	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to GS_n		1.10 1.10	4.10 4.10	1.10 1.10	4.10 4.10	1.10 1.10	4.60 4.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Q_n, $\overline{Q}_n$	Waveform 2	1.00 1.00	3.30 3.30	1.00 1.00	3.30 3.30	1.00 1.00	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to GS_n		1.00 1.00	3.30 3.30	1.00 1.00	3.30 3.30	1.00 1.00	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.90 0.90	3.60 3.60	1.00 1.00	3.60 3.60	1.00 1.00	3.80 3.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n, $\overline{Q}_n$, GS_n	Waveforms 1,2	1.40 1.40	4.70 4.70	1.40 1.40	4.60 4.60	1.40 1.40	5.00 5.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to $\overline{E}$	Waveform 3	1.10		1.00		1.10		ns
t_h	Hold time $\overline{E}$ to D_n		1.30		1.30		1.30		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX	MIN.	MAX	MIN.	MAX	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.10 1.10	3.90 3.90	1.10 1.10	3.90 3.90	1.10 1.10	4.40 4.40	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to GS_n		1.10 1.10	3.90 3.90	1.10 1.10	3.90 3.90	1.10 1.10	4.40 4.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Q_n, $\overline{Q}_n$	Waveform 2	1.00 1.00	3.10 3.10	1.00 1.00	3.10 3.10	1.00 1.00	3.20 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to GS_n		1.00 1.00	3.10 3.10	1.00 1.00	3.10 3.10	1.00 1.00	3.20 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.90 0.90	3.40 3.40	1.00 1.00	3.40 3.40	1.00 1.00	3.60 3.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n, $\overline{Q}_n$, GS_n	Waveforms 1,2	1.40 1.40	4.50 4.50	1.40 1.40	4.40 4.40	1.40 1.40	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to $\overline{E}$	Waveform 3	0.90		0.80		0.90		ns
t_h	Hold time $\overline{E}$ to D_n		1.10		1.10		1.10		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

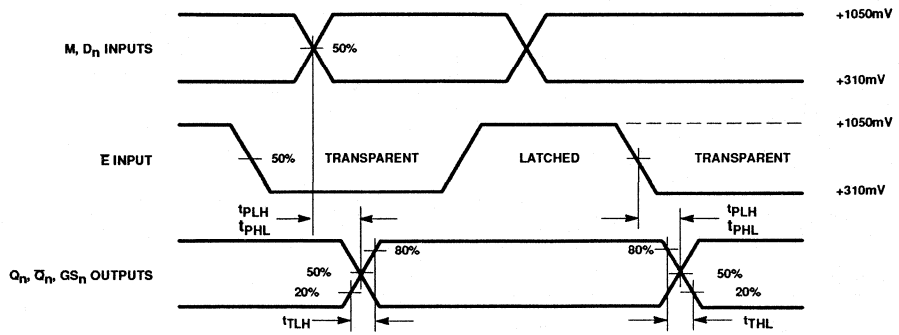
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

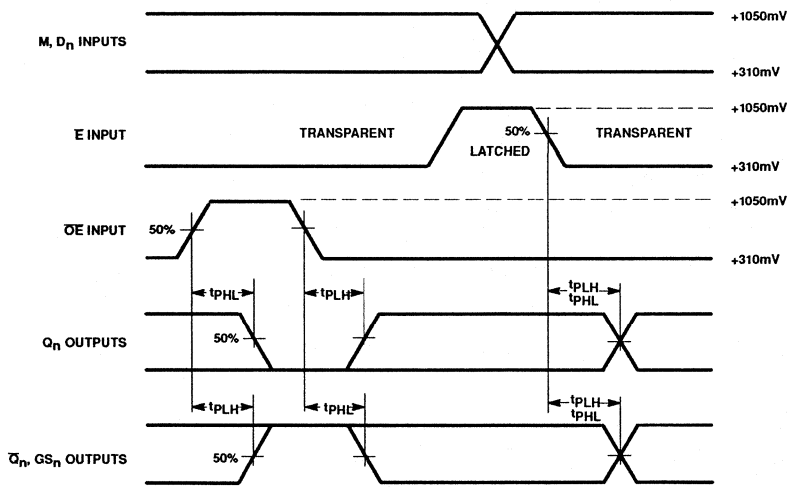
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX	MIN.	MAX	MIN.	MAX	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.10 1.10	3.90 3.90	1.10 1.10	3.90 3.90	1.10 1.10	4.40 4.40	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to GS_n		1.10 1.10	3.90 3.90	1.10 1.10	3.90 3.90	1.10 1.10	4.40 4.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Q_n, $\overline{Q}_n$	Waveform 2	1.00 1.00	3.10 3.10	1.00 1.00	3.10 3.10	1.00 1.00	3.20 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to GS_n		1.00 1.00	3.10 3.10	1.00 1.00	3.10 3.10	1.00 1.00	3.20 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.90 0.90	3.40 3.40	1.00 1.00	3.40 3.40	1.00 1.00	3.60 3.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n, $\overline{Q}_n$, GS_n	Waveforms 1,2	1.40 1.40	4.50 4.50	1.40 1.40	4.40 4.40	1.40 1.40	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to $\overline{E}$	Waveform 3	0.90		0.80		0.90		ns
t_h	Hold time $\overline{E}$ to D_n		1.10		1.10		1.10		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

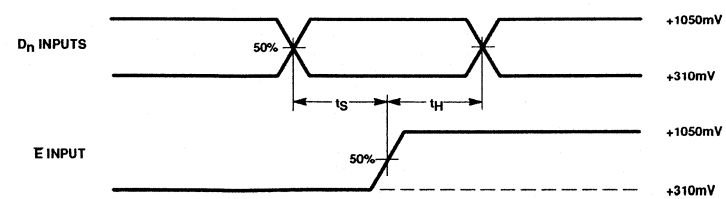
AC WAVEFORMS



Waveform 1. Propagation Delays and Transition Times



Waveform 2. Output Enable Timing



Waveform 3. Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

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Status	Product Specification
ECL Products	

100166

9–Bit Comparator

FEATURES

- **Typical propagation delay: 2.3ns**
- **Typical supply current ($-I_{EE}$): 140mA**

DESCRIPTION

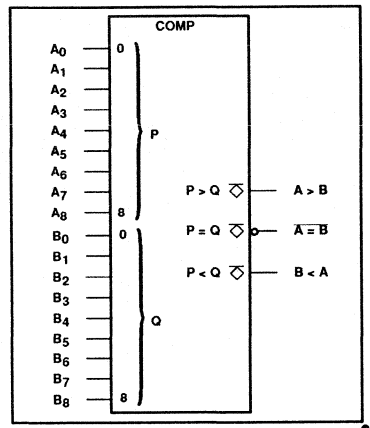
The 100166 is a 9–bit Comparator which compares the arithmetic values of two 9–bit words (A and B) and indicates whether one word is greater than, less than, or equal to the other one.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_8$	A Data Inputs
$B_0 - B_8$	B Data Inputs
A > B	A Greater Than B Output
B > A	B Greater Than A Output
$\overline{A = B}$	A Equal to B Output (Active Low)

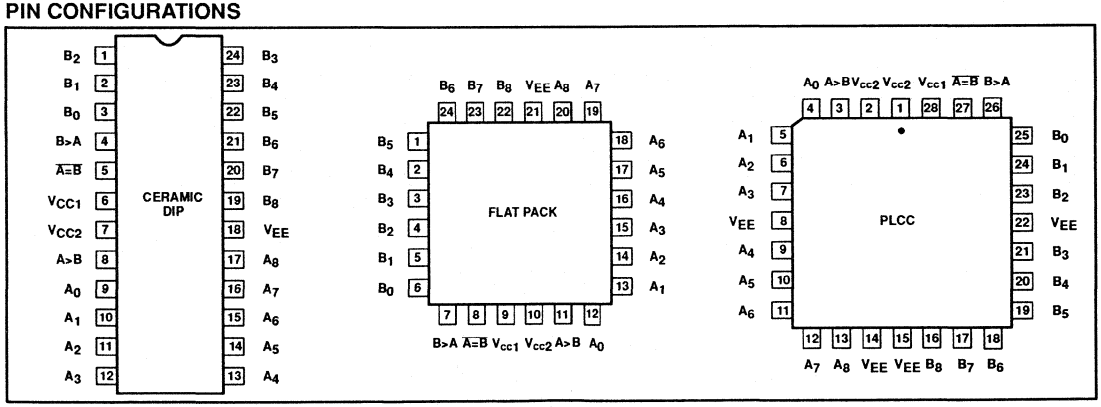
IEC/IEEE SYMBOL



ORDERING INFORMATION

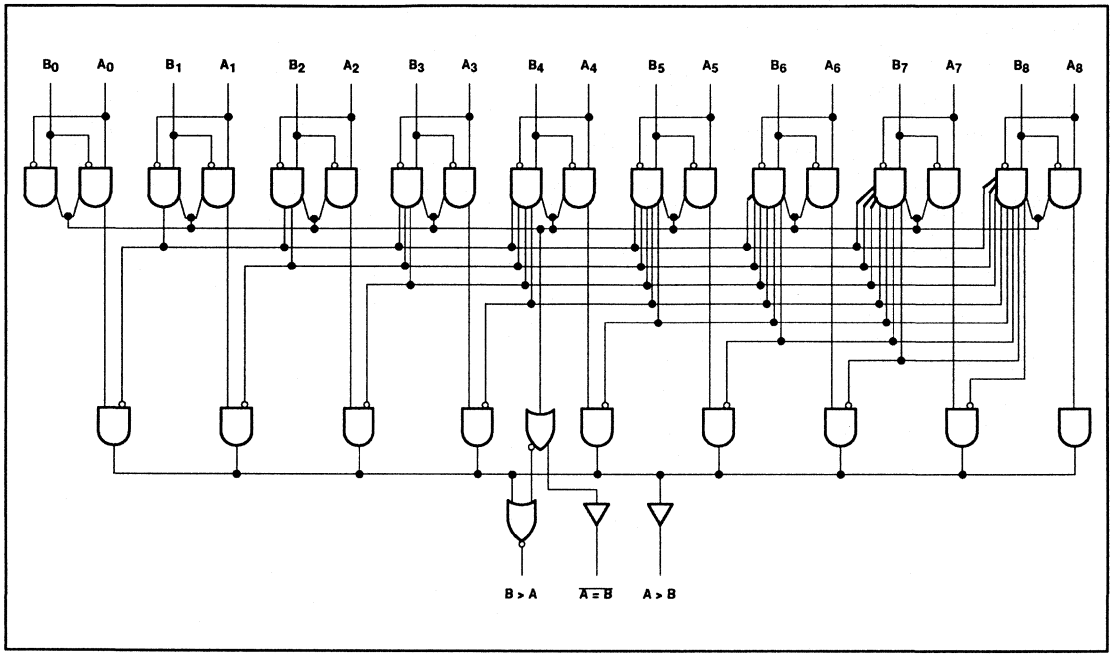
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100166F
24–Pin Ceramic Flat Pack	100166Y
28–Pin PLCC	100166A

PIN CONFIGURATIONS



Comparator 100166

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS		
A_0, B_0	A_1, B_1	A_2, B_2	A_3, B_3	A_4, B_4	A_5, B_5	A_6, B_6	A_7, B_7	A_8, B_8	A > B	B > A	$\overline{A = B}$
								H L	H	L	H
								L H	L	H	H
							H L	$A_8 = B_8$	H	L	H
							L H	$A_8 = B_8$	L	H	H
						H L	$A_7 = B_7$	$A_8 = B_8$	H	L	H
						L H	$A_7 = B_7$	$A_8 = B_8$	L	H	H
					H L	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	H	L	H
					L H	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	L	H	H
				H L	$A_5 = B_5$	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	H	L	H
				L H	$A_5 = B_5$	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	L	H	H
			H L	$A_4 = B_4$	$A_5 = B_5$	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	H	L	H
			L H	$A_4 = B_4$	$A_5 = B_5$	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	L	H	H
		H L	$A_3 = B_3$	$A_4 = B_4$	$A_5 = B_5$	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	H	L	H
		L H	$A_3 = B_3$	$A_4 = B_4$	$A_5 = B_5$	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	L	H	H
	H L	$A_2 = B_2$	$A_3 = B_3$	$A_4 = B_4$	$A_5 = B_5$	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	H	L	H
	L H	$A_2 = B_2$	$A_3 = B_3$	$A_4 = B_4$	$A_5 = B_5$	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	L	H	H
H L	$A_1 = B_1$	$A_2 = B_2$	$A_3 = B_3$	$A_4 = B_4$	$A_5 = B_5$	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	H	L	H
L H	$A_1 = B_1$	$A_2 = B_2$	$A_3 = B_3$	$A_4 = B_4$	$A_5 = B_5$	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	L	H	H
$A_0 = B_0$	$A_1 = B_1$	$A_2 = B_2$	$A_3 = B_3$	$A_4 = B_4$	$A_5 = B_5$	$A_6 = B_6$	$A_7 = B_7$	$A_8 = B_8$	L	L	L

NOTES:
H = High voltage level
L = Low voltage level
Blank = Don't care

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					250	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}			119	140	238	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C MIN.	LIMITS T_A = 0°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH}	Propagation delay	Waveform 1	1.40	3.50	1.40	3.50	1.40	3.90	ns
t_{PHL}	Any input to any output		1.40	3.50	1.40	3.50	1.40	3.90	ns
t_{TLH}	Transition time for all outputs		0.45	1.60	0.45	1.60	0.45	1.60	ns
t_{THL}			0.45	1.60	0.45	1.60	0.45	1.60	ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay Any input to any output	Waveform 1	1.40 1.40	3.50 3.50	1.40 1.40	3.50 3.50	1.40 1.40	3.90 3.90	ns ns
t_{TLH} t_{THL}	Transition time for all outputs		0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay Any input to any output	Waveform 1	1.40 1.40	3.30 3.30	1.40 1.40	3.30 3.30	1.40 1.40	3.70 3.70	ns ns
t_{TLH} t_{THL}	Transition time for all outputs		0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

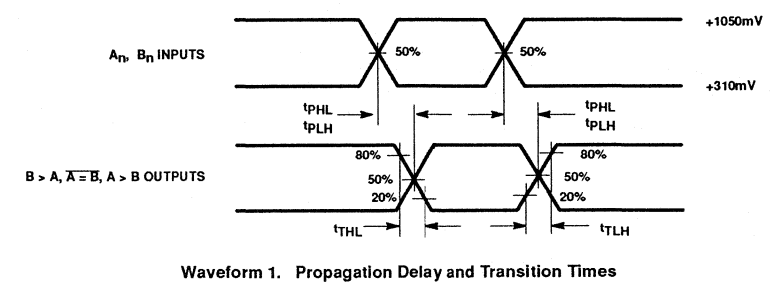
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Any input to any output	Waveform 1	1.40 1.40	3.30 3.30	1.40 1.40	3.30 3.30	1.40 1.40	3.70 3.70	ns ns
t_{TLH} t_{THL}	Transition time for all outputs		0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

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Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100170

Demultiplexer/Decoder

FEATURES

- **Typical propagation delay: 1.8ns**
- **Typical supply current ($-I_{EE}$): 110mA**

DESCRIPTION

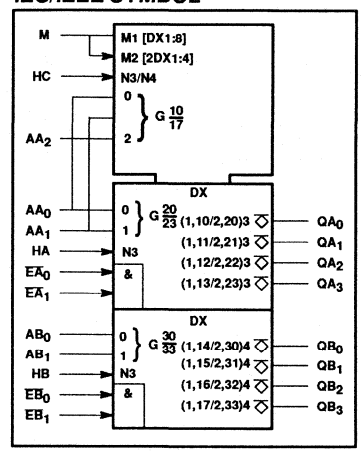
The 100170 operates as a Dual 1–of–4 Decoder, or as a Single 1–of–8 Decoder; the operating mode is fixed by the Mode Control input (M). The inputs HA, HB, HC determine whether the outputs are active Low or High. In the 1–of–8 mode, the two pairs of active Low Enables can be tied together ($\overline{EA}_0$ to $\overline{EB}_0$, $\overline{EA}_1$ to $\overline{EB}_1$), to provide two active Low Enables ($\overline{E}_0$ and $\overline{E}_1$, respectively).

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$AA_0 - AA_2$	Address Inputs
AB_0, AB_1	Address Inputs
$\overline{EA}_0$, $\overline{EA}_1$	Enable Inputs
$\overline{EB}_0$, $\overline{EB}_1$	Enable Inputs
M	Mode Control Input
HA, HB	Polarity Select Inputs
HC	Common Polarity Select Input
$QA_0 - QA_3$	Data Outputs
$QB_0 - QB_3$	Data Outputs

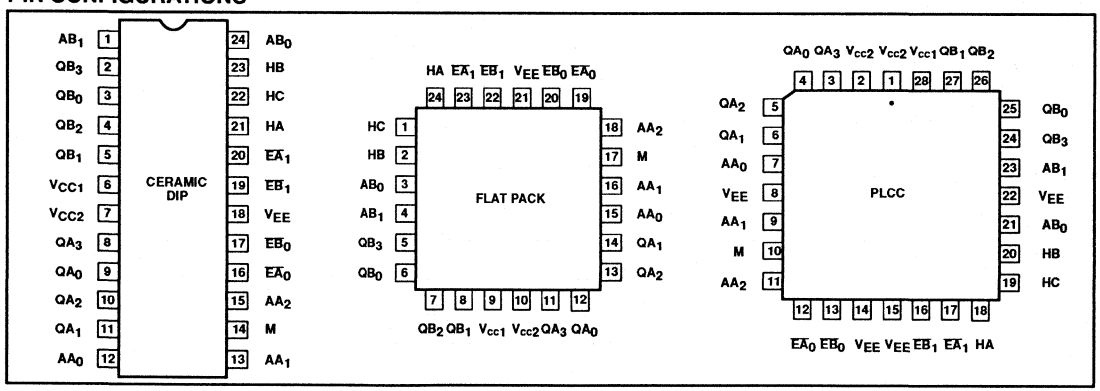
IEC/IEEE SYMBOL



ORDERING INFORMATION

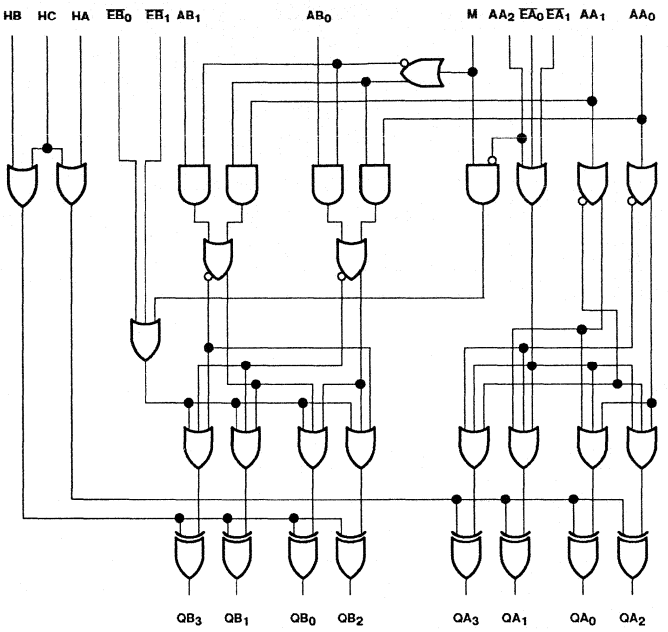
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100170F
24–Pin Ceramic Flat Pack	100170Y
28–Pin PLCC	100170A

PIN CONFIGURATIONS



Demultiplexer/Decoder 100170

LOGIC DIAGRAM



FUNCTION TABLE (Dual 1–of–4 Mode) M = AA_2 = HC = Low

INPUTS				OUTPUTS							
				HA = HB = High				HA = HB = Low			
$\overline{EA_0}$ $\overline{EB_0}$	$\overline{EA_1}$ $\overline{EB_1}$	AA_1 AB_1	AA_0 AB_0	QA_0 QB_0	QA_1 QB_1	QA_2 QB_2	QA_3 QB_3	QA_0 QB_0	QA_1 QB_1	QA_2 QB_2	QA_3 QB_3
H X	X H	X X	X X	L L	L L	L L	L L	H H	H H	H H	H H
L L L L	L L L L	L L H H	L H L H	H L L L	L H L L	L L H L	L L L H	L H H H	H L H H	H H L H	H H H L

NOTES:
H = High voltage level
L = Low voltage evel
X = Don't care

Demultiplexer/Decoder 100170

FUNCTION TABLE (Single 1–of–8 Mode)

M = High, HA = HB = Low, AB_0 and AB_1 are "don't care".

INPUTS					OUTPUTS													
					HC = High								HC = Low					
$\overline{E}_0$	E_1	AA_0	AA_1	AA_2	QA_0	QA_1	QA_2	QA_3	QB_0	QB_1	QB_2	QB_3	QA_0	QA_1	QA_2	QA_3	QB_0	QB_1	QB_2	QB_3
H	X	X	X	X	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
X	H	X	X	X	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	L	L	L	L	L	H	L	H	H	H	H	H	H
L	L	L	H	L	L	L	H	L	L	L	L	L	H	H	L	H	H	H	H	H
L	L	H	H	L	L	L	L	H	L	L	L	L	H	H	H	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	L	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	L	L	L	L	L	H	L	L	H	H	H	H	H	L	H	H
L	L	L	H	H	L	L	L	L	L	L	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
$\overline{E}_0$ = $\overline{EA}_0$ and $\overline{EB}_0$ wired together.
$\overline{E}_1$ = $\overline{EA}_1$ and $\overline{EB}_1$ wired together.

ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	HC, AA_n	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					310	µA
		All others						250	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}.			76	110	153	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C MIN.	LIMITS T_A = 0°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH} t_{PHL}	Propagation delay EA_n to QA_n, $\overline{EB}_n$ to QB_n	Waveform 1	0.80 0.80	2.30 2.30	0.80 0.80	2.20 2.20	0.80 0.80	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay AB_n to QB_n, AA_n to QA_n and QB_n		0.95 0.95	2.80 2.80	0.95 1.00	2.70 2.70	1.00 1.00	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay HA to QA_n, HB to QB_n, HC to QA_n and QB_n		1.00 1.00	3.00 3.00	1.00 1.00	2.90 2.90	1.00 1.00	3.00 3.00	ns ns
t_{PLH} t_{PHL}	Propagation delay M to QB_n		1.50 1.50	3.90 3.90	1.60 1.60	3.80 3.80	1.60 1.60	3.90 3.90	ns ns
t_{TLH} t_{THL}	Transition time QA_n, QB_n		0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	ns ns

NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay $\overline{EA}_n$ to QA_n, $\overline{EB}_n$ to QB_n	Waveform 1	0.80 0.80	2.30 2.30	0.80 0.80	2.20 2.20	0.80 0.80	2.30 2.30	ns ns
t_{PLH} t_{PHL}	Propagation delay AB_n to QB_n, AA_n to QA_n and QB_n		0.95 1.00	2.80 2.80	0.95 1.00	2.70 2.70	1.00 1.00	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay HA to QA_n, HB to QB_n, HC to QA_n and QB_n		1.00 1.00	3.00 3.00	1.00 1.00	2.90 2.90	1.00 1.00	3.00 3.00	ns ns
t_{PLH} t_{PHL}	Propagation delay M to QB_n		1.50 1.50	3.90 3.90	1.60 1.60	3.80 3.80	1.60 1.60	3.90 3.90	ns ns
t_{TLH} t_{THL}	Transition time QA_n, QB_n		0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay $\overline{EA}_n$ to QA_n, $\overline{EB}_n$ to QB_n	Waveform 1	0.80 0.80	2.10 2.10	0.80 0.80	2.00 2.00	0.80 0.80	2.10 2.10	ns ns
t_{PLH} t_{PHL}	Propagation delay AB_n to QB_n, AA_n to QA_n and QB_n		0.95 0.95	2.60 2.60	0.95 1.00	2.50 2.50	1.00 1.00	2.70 2.70	ns ns
t_{PLH} t_{PHL}	Propagation delay HA to QA_n, HB to QB_n, HC to QA_n and QB_n		1.00 1.00	2.80 2.80	1.00 1.00	2.70 2.70	1.00 1.00	2.80 2.80	ns ns
t_{PLH} t_{PHL}	Propagation delay M to QB_n		1.50 1.50	3.70 3.70	1.60 1.60	3.60 3.60	1.60 1.60	3.70 3.70	ns ns
t_{TLH} t_{THL}	Transition time QA_n, QB_n		0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

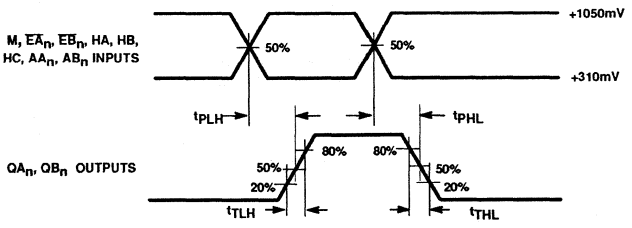
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay $\overline{EA}_n$ to QA_n, $\overline{EB}_n$ to QB_n	Waveform 1	0.80 0.80	2.10 2.10	0.80 0.80	2.00 2.00	0.80 0.80	2.10 2.10	ns ns
t_{PLH} t_{PHL}	Propagation delay AB_n to QB_n, AA_n to QA_n and QB_n		0.95 0.95	2.60 2.60	0.95 1.00	2.50 2.50	1.00 1.00	2.70 2.70	ns ns
t_{PLH} t_{PHL}	Propagation delay HA to QA_n, HB to QB_n, HC to QA_n and QB_n		1.00 1.00	2.80 2.80	1.00 1.00	2.70 2.70	1.00 1.00	2.80 2.80	ns ns
t_{PLH} t_{PHL}	Propagation delay M to QB_n		1.50 1.50	3.70 3.70	1.60 1.60	3.60 3.60	1.60 1.60	3.70 3.70	ns ns
t_{TLH} t_{THL}	Transition time QA_n, QB_n		0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	0.45 0.45	1.60 1.60	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–0631
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100171

Triple 4–Input Multiplexer

FEATURES

- **Typical propagation delay: 1.10ns**
- **Typical supply current ($-I_{EE}$): 83mA**

DESCRIPTION

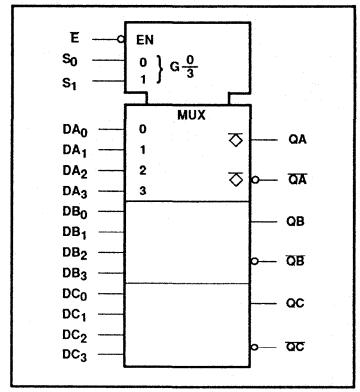
The 100171 is a triple, 4–input multiplexer with True outputs (QA, QB, QC) and Complementary outputs ($\overline{QA}$, $\overline{QB}$, $\overline{QC}$) and two common select inputs (S_n). For each of the three multiplexer units, the S_n lines gates one of four possible data inputs (for example, DA_n) to the corresponding outputs (in this case, QA and $\overline{QA}$). A High on the enable input ($\overline{E}$) forces all True outputs Low and all Complementary outputs High.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$DB_0 - DB_3$	Data Inputs
$DC_0 - DC_3$	Data Inputs
S_0, S_1	Select Inputs
$\overline{E}$	Enable Input
QA, QB, QC	True Data Outputs
$\overline{QA}$, $\overline{QB}$, $\overline{QC}$	Complementary Data Outputs

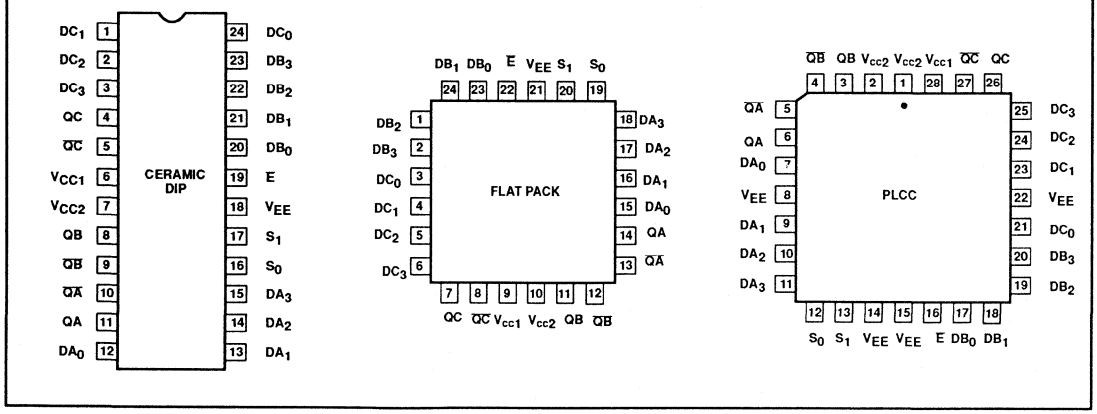
IEC/IEEE SYMBOL



ORDERING INFORMATION

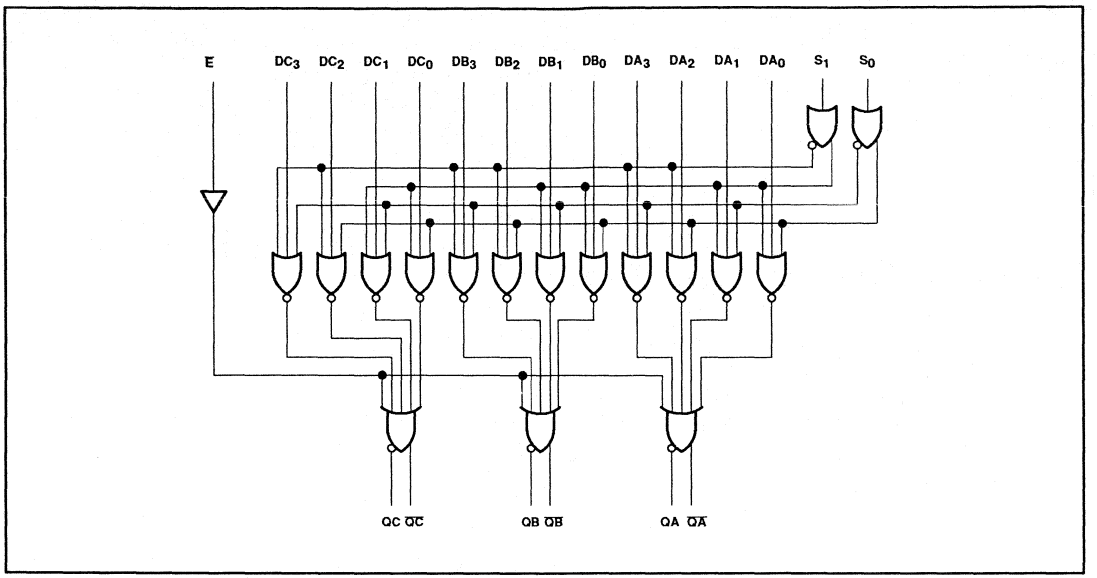
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100171F
24–Pin Ceramic Flat Pack	100171Y
28–Pin PLCC	100171A

PIN CONFIGURATIONS



Multiplexer 100171

LOGIC DIAGRAM



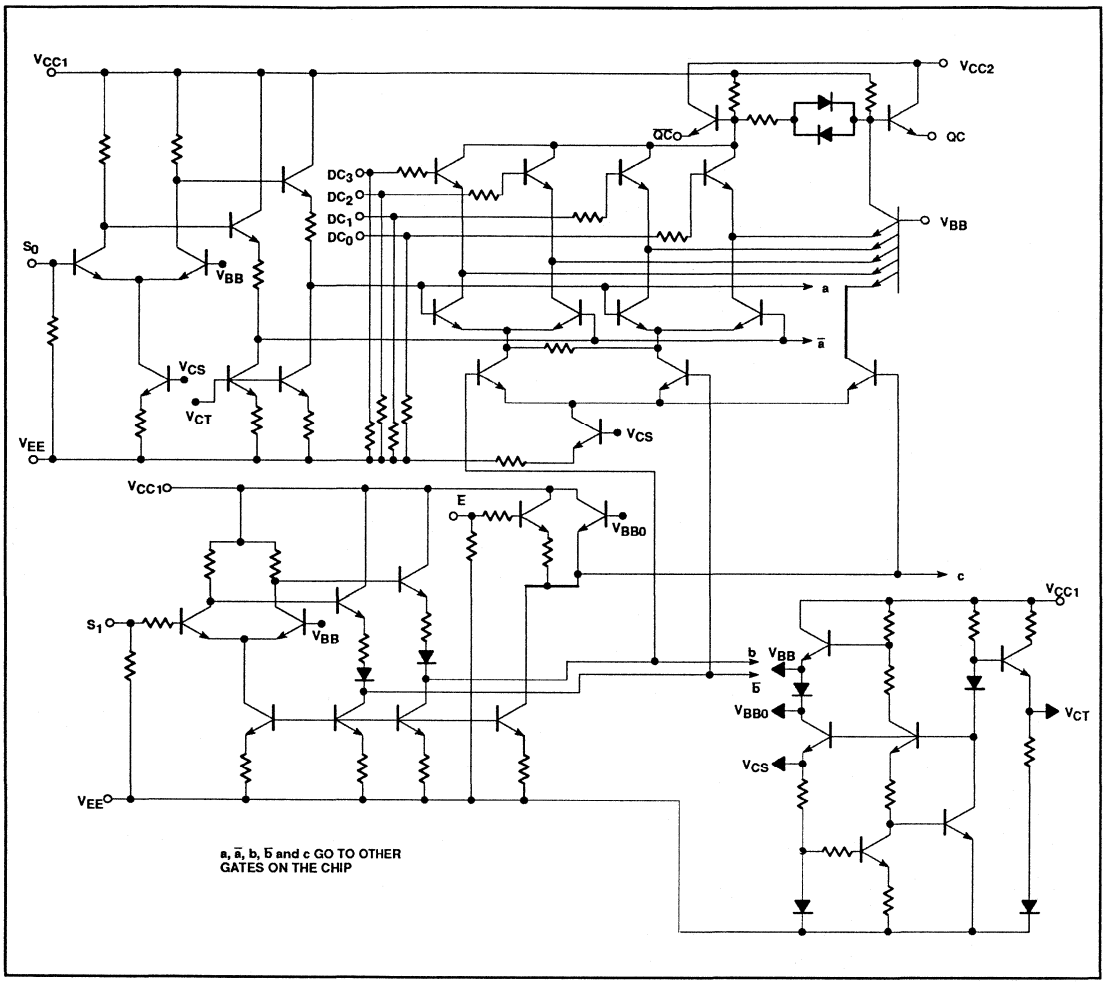
FUNCTION TABLE

INPUTS							OUTPUTS	
$\overline{E}$	S_1	S_0	DA_0 DB_0 DC_0	DA_1 DB_1 DC_1	DA_2 DB_2 DC_2	DA_3 DB_3 DC_3	$\overline{QA}$ $\overline{QB}$ $\overline{QC}$	QA QB QC
H	X	X	X	X	X	X	H	L
L L	L L	L L	L H	X X	X X	X X	H L	L H
L L	L L	H H	X X	L H	X X	X X	H L	L H
L L	H H	L L	X X	X X	L H	X X	H L	L H
L L	H H	H H	X X	X X	X X	L H	H L	L H

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

Multiplexer 100171

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	DA_n, DB_n, DC_n	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					340	µA
		A_n						300	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			56	83	114	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.

NOTES (CONTINUED):
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n to QA and $\overline{QA}$, DB_n to QB and $\overline{QB}$, DC_n to QC and $\overline{QC}$	Waveform 1	0.45 0.45	1.70 1.70	0.45 0.45	1.60 1.60	0.50 0.50	1.70 1.70	ns ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to all outputs		0.90 0.90	2.40 2.40	0.90 0.90	2.60 2.60	1.00 1.00	3.00 3.00	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to all outputs		0.65 0.65	2.40 2.40	0.65 0.65	2.30 2.30	0.75 0.75	2.40 2.40	ns ns
t_{TLH} t_{THL}	Transition time for all outputs		0.45 0.45	1.70 1.70	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n to QA and $\overline{QA}$, DB_n to QB and $\overline{QB}$, DC_n to QC and $\overline{QC}$	Waveform 1	0.45 0.45	1.70 1.70	0.45 0.45	1.60 1.60	0.50 0.50	1.70 1.70	ns ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to all outputs		0.90 0.90	2.40 2.40	0.90 0.90	2.60 2.60	1.00 1.00	3.00 3.00	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to all outputs		0.65 0.65	2.40 2.40	0.65 0.65	2.30 2.30	0.75 0.75	2.40 2.40	ns ns
t_{TLH} t_{THL}	Transition time for all outputs		0.45 0.45	1.70 1.70	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n to QA and $\overline{QA}$, DB_n to QB and $\overline{QB}$, DC_n to QC and $\overline{QC}$	Waveform 1	0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.50 0.50	1.50 1.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to all outputs		0.90 0.90	2.20 2.20	0.90 0.90	2.40 2.40	1.00 1.00	2.80 2.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to all outputs		0.65 0.65	2.20 2.20	0.65 0.65	2.10 2.10	0.75 0.75	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time for all outputs		0.45 0.45	1.70 1.70	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

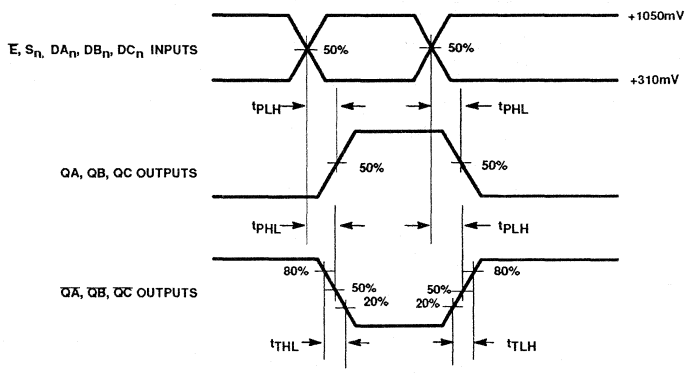
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay DA_n to QA and $\overline{QA}$, DB_n to QB and $\overline{QB}$, DC_n to QC and $\overline{QC}$	Waveform 1	0.45 0.45	1.50 1.50	0.45 0.45	1.40 1.40	0.50 0.50	1.50 1.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to all outputs		0.90 0.90	2.20 2.20	0.90 0.90	2.40 2.40	1.00 1.00	2.80 2.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to all outputs		0.65 0.65	2.20 2.20	0.65 0.65	2.10 2.10	0.75 0.75	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time for all outputs		0.45 0.45	1.70 1.70	0.45 0.45	1.50 1.50	0.45 0.45	1.50 1.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–0632
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100175

Translator

FEATURES

- **Typical propagation delay from D_n to Q_n: 2.2ns**
- **Typical propagation delay from $\overline{E}_n$ to Q_n: 2.7ns**
- **Typical supply current ($-I_{EE}$): 67mA**

DESCRIPTION

The 100175 is composed of five latches, each with one data input and one data output. A Master Reset input (MR) and two Enable inputs ($\overline{E}_0$, $\overline{E}_1$) preside over all the latches. A Q_n output follows its D_n input when both $\overline{E}_0$ and $\overline{E}_1$ are Low. When either $\overline{E}_0$ or $\overline{E}_1$ (or both) go High, the latches store the last valid data present on their D_n inputs. The MR input forces the Q_n outputs Low if either $\overline{E}_0$ or $\overline{E}_1$ (or both) are High. The inputs are 100K compatible and the outputs are 10K compatible.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

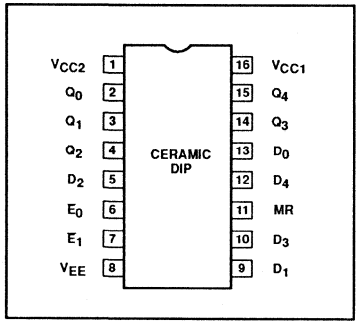
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_4$	Data inputs (100K ECL compatible)
MR	Master reset input (100K ECL compatible)
$\overline{E}_0$, $\overline{E}_1$	Enable input (100K ECL compatible)
$Q_0 - Q_4$	Data outputs (10K ECL compatible)

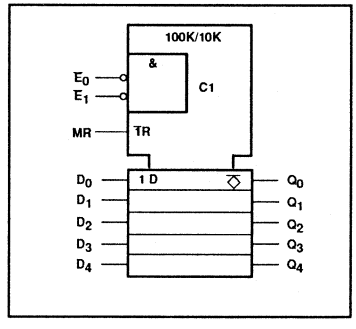
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Ceramic DIP (300 mils wide)	100175F

PIN CONFIGURATION

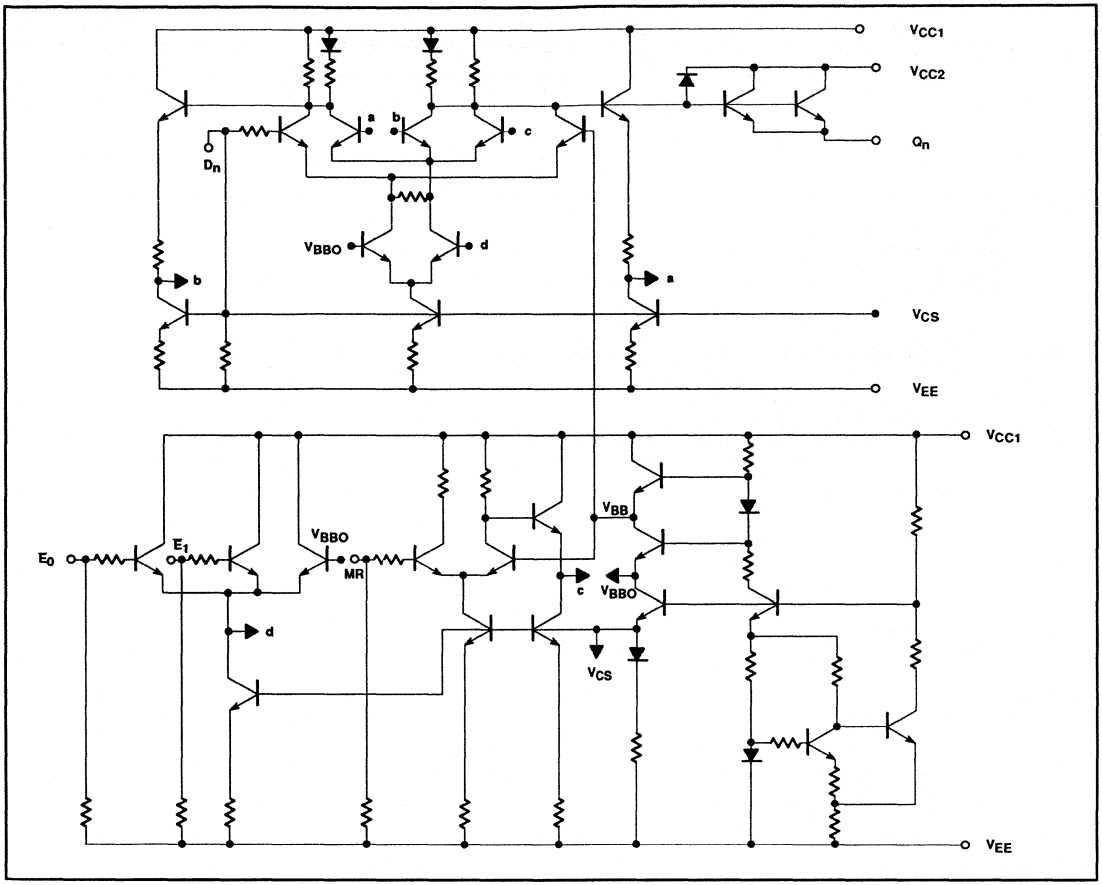


IEC/IEEE

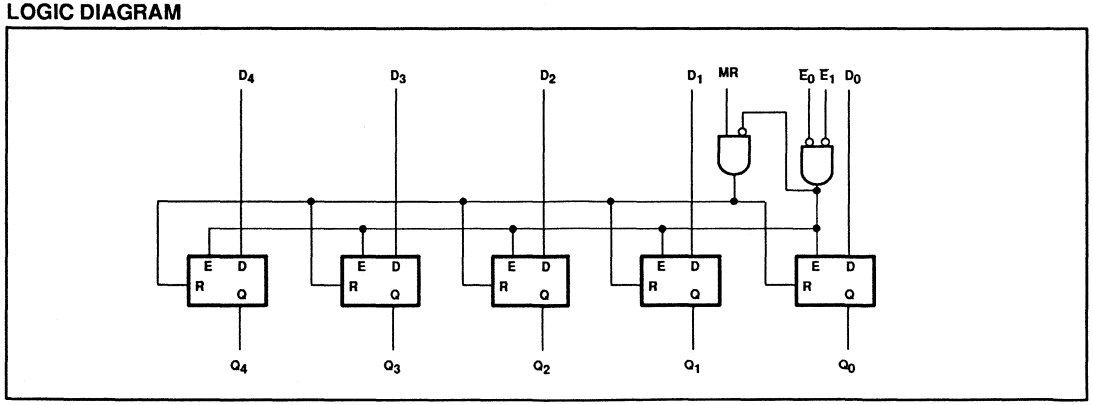


Translator | 100175

SIMPLIFIED SCHEMATIC



LOGIC DIAGRAM



Translator 100175

FUNCTION TABLE

INPUTS				OUTPUT
D_n	$\overline{E}_0$	$\overline{E}_1$	MR	Q_n
H	L	L	X	H
L	L	L	X	L
X	H	X	L	NC
X	X	H	L	NC
X	H	X	H	L
X	X	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
NC = No change

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–5.7	–5.2		V
V_{IH}	High level input voltage	V_{EE} = –5.2V ± 0.010V	–1165		–880	mV
V_{IL}	Low level input voltage	V_{EE} = –5.2V ± 0.010V	–1810		–1475	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

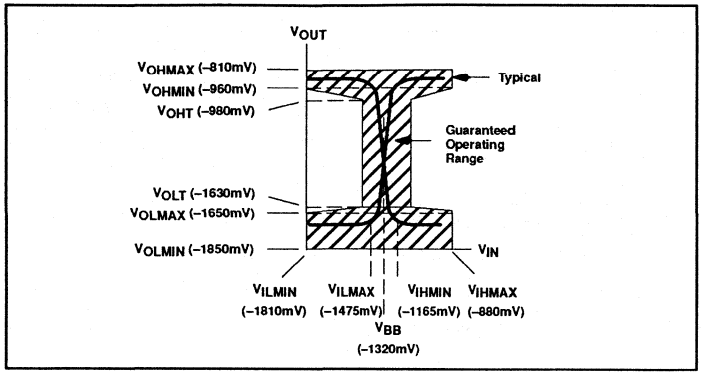
$V_{CC1} = V_{CC2}$ =ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to −2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	$T_A = 0°C$	−1000		−840	mV
					$T_A = +25°C$	−960		−810	mV
					$T_A = +85°C$	−890		−700	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	$T_A = 0°C$	−1020			mV
					$T_A = +25°C$	−980			mV
					$T_A = +85°C$	−910			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	$T_A = 0°C$			−1645	mV
					$T_A = +25°C$			−1630	mV
					$T_A = +85°C$			−1595	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	$T_A = 0°C$	−1870		−1665	mV
					$T_A = +25°C$	−1850		−1650	mV
					$T_A = +85°C$	−1825		−1615	mV
I_{IH}	High level input current	MR input	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					650	µA
		All others						290	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}.			50	67	102	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation		$V_{EE} = -4.68V$, $T_A = +25°C$				0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation						0.250		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

TRANSFER CHARACTERISTIC



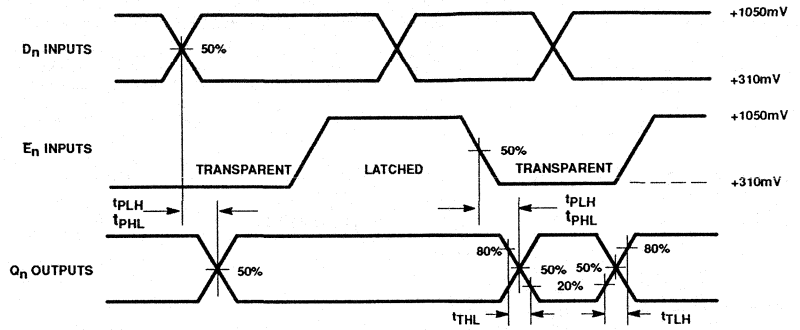
AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$

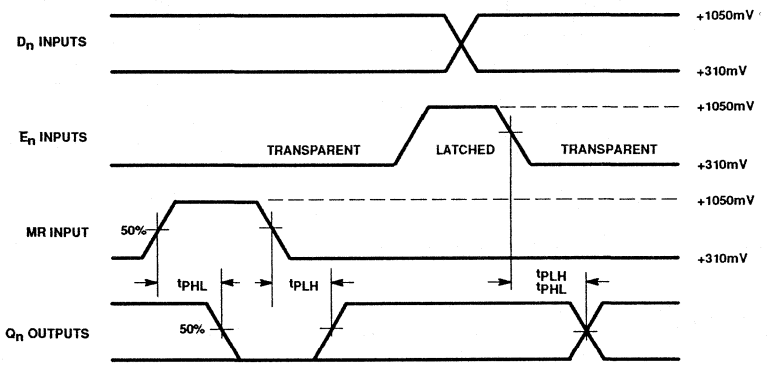
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	3.40 3.40	1.00 1.00	3.40 3.40	1.00 1.00	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n		1.00 1.00	4.30 4.30	1.00 1.00	4.30 4.30	1.00 1.00	4.30 4.30	ns ns
t_{PLH} t_{PHL}	Propagation delay MR to Q_n	Waveform 2	1.00 1.00	3.90 3.90	1.00 1.00	3.90 3.90	1.00 1.00	3.90 3.90	ns ns
t_{TLH} t_{THL}	Transition time Q_n	Waveform 1	0.90 0.90	3.50 3.50	1.00 1.00	3.50 3.50	0.90 0.90	3.50 3.50	ns ns
t_s	Setup time, D_n to $\overline{E}_n$	Waveform 3	2.5		2.5		2.5		ns
t_h	Hold time, $\overline{E}_n$ to D_n	Waveform 3	0.5		0.5		0.5		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

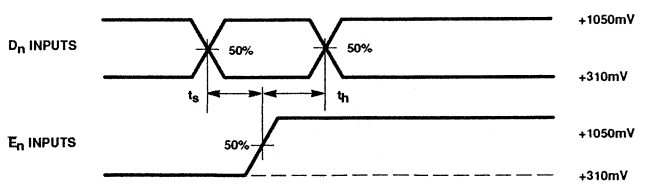
AC WAVEFORMS



Waveform 1. Propagation Delays and Transition Times



Waveform 2. Reset Timing

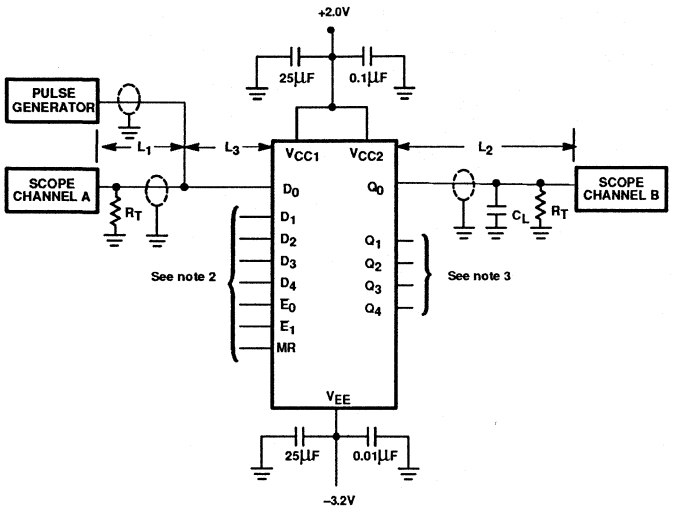


Waveform 3. Data Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Translator 100175

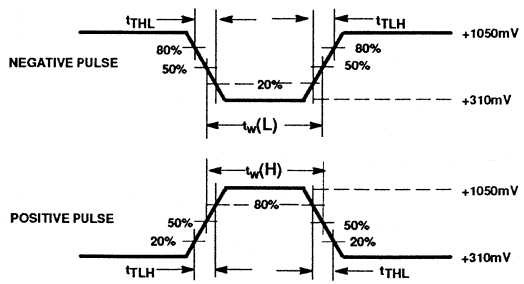
AC TEST CIRCUIT



NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T = 0V$ (system ground)				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
100K ECL	740mV$_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Philips Components

Document No.	853–1437
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Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100179

Carry Look–Ahead Generator

FEATURES

- **Typical propagation delay: 1.9ns**
- **Typical supply current ($-I_{EE}$): 150mA**

DESCRIPTION

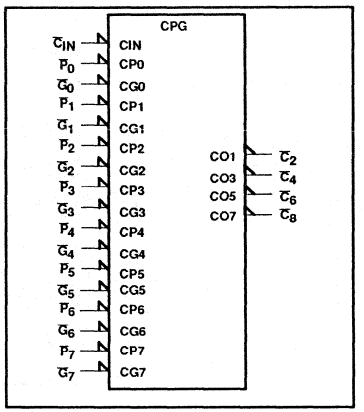
The 100179 is a high–speed, Carry Look–Ahead Generator intended for use with the 100180 6–bit Fast Adder and the 100181 4–bit ALU.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$\overline{C}_{IN}$	Carry Input (active Low)
$\overline{P}_0 - \overline{P}_7$	Carry Look–Ahead Propagate inputs (active Low)
$\overline{G}_0 - \overline{G}_7$	Carry Look–Ahead Generate inputs. (active–Low)
$\overline{C}_2, \overline{C}_4, \overline{C}_6, \overline{C}_8$	Carry Outputs (active–Low)

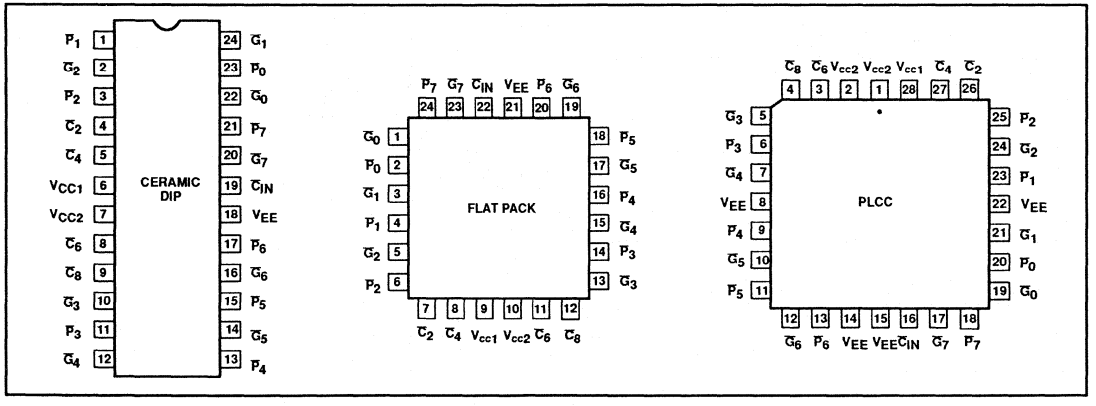
IEC/IEEE SYMBOL



ORDERING INFORMATION

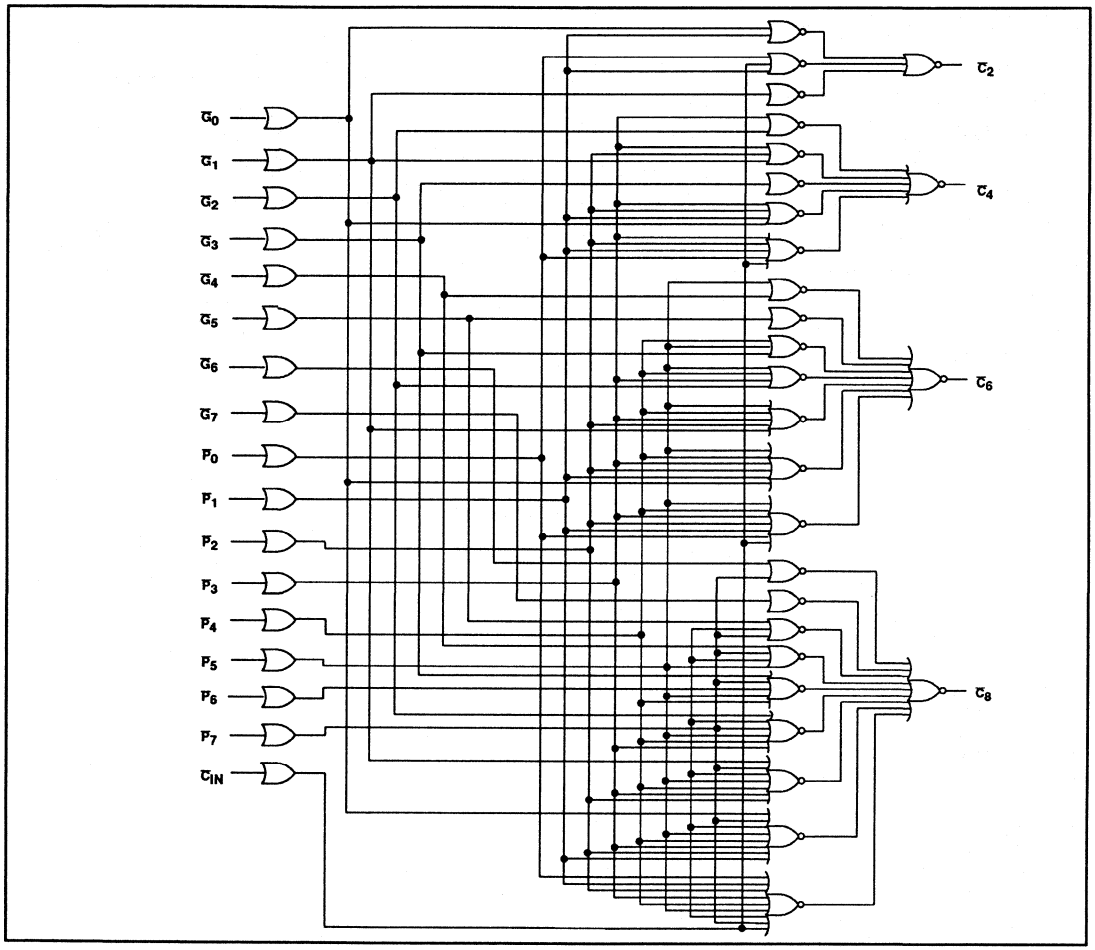
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100179F
24–Pin Ceramic Flat Pack	100179Y
28–Pin PLCC	100179A

PIN CONFIGURATIONS



Carry Look–Ahead Generator 100179

LOGIC DIAGRAM



FUNCTION TABLE FOR $\overline{C}_2$ OUTPUT

INPUTS					OUTPUT
$\overline{C}_{IN}$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{C}_2$
X	X	X	L	X	L
X	L	X	X	L	L
L	X	L	X	L	L
All other combinations					H

NOTES:

$\overline{C}_2 = \overline{G}_1 \bullet (\overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_1 + \overline{P}_0 + \overline{C}_{IN})$

H = High voltage level
L = Low voltage level
X = Don't care

Carry Look–Ahead Generator 100179

FUNCTION TABLE FOR $\overline{C}_4$ OUTPUT

INPUTS									OUTPUT
$\overline{C}_{IN}$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{C}_4$
X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	L	X	X	L	L
X	X	X	L	X	X	L	X	L	L
X	L	X	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	L
All other combinations									H

NOTES:

$\overline{C}_4 = \overline{G}_3 \bullet (\overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_{IN})$

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE FOR $\overline{C}_6$ OUTPUT

INPUTS													OUTPUT
$\overline{C}_{IN}$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{G}_4$	$\overline{P}_4$	$\overline{G}_5$	$\overline{P}_5$	$\overline{C}_6$
X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations													H

NOTES:

$\overline{C}_6 = \overline{G}_5 \bullet (\overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet$
$(\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_{IN})$

H = High voltage level
L = Low voltage level
X = Don't care

Carry Look–Ahead Generator 100179

FUNCTION TABLE FOR $\overline{C}_8$ OUTPUT

INPUTS																	OUTPUT
$\overline{C}_{IN}$	$\overline{G}_0$	P_0	$\overline{G}_1$	P_1	$\overline{G}_2$	P_2	$\overline{G}_3$	P_3	$\overline{G}_4$	P_4	$\overline{G}_5$	P_5	$\overline{G}_6$	P_6	$\overline{G}_7$	P_7	$\overline{C}_8$
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations																	H

NOTES:

$\overline{C}_8 = \overline{G}_7 \bullet (P_7 + \overline{G}_6) \bullet (P_7 + P_6 + \overline{G}_5) \bullet (P_7 + P_6 + P_5 + \overline{G}_4) \bullet (P_7 + P_6 + P_5 + P_4 + \overline{G}_3) \bullet (P_7 + P_6 + P_5 + P_4 + P_3 + \overline{G}_2) \bullet$
$(P_7 + P_6 + P_5 + P_4 + P_3 + P_2 + \overline{G}_1) \bullet (P_7 + P_6 + P_5 + P_4 + P_3 + P_2 + P_1 + \overline{G}_0) \bullet (P_7 + P_6 + P_5 + P_4 + P_3 + P_2 + P_1 + P_0 + \overline{C}_{IN})$

H = High Voltage Level
L = Low Voltage Level
X = Don't care

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

Carry Look–Ahead Generator | 100179

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs Loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	$\overline{C}_{IN}, \overline{G}_0 - \overline{G}_7$	One input under test at V_{IHMAX}, other inputs at V_{ILMIN}.					250	µA
		$\overline{P}_0 - \overline{P}_7$	One input under test at V_{IHMAX}, other inputs at V_{ILMIN}.					340	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}, other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}.			100	150	220	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground. V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$, $\overline{G}_n$, $\overline{P}_n$ to $\overline{C}_2$, $\overline{C}_4$, $\overline{C}_6$, $\overline{C}_8$	Waveform 1	1.10 1.10	2.90 2.90	1.10 1.10	2.90 2.90	1.10 1.10	3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time $\overline{C}_2$, $\overline{C}_4$, $\overline{C}_6$, $\overline{C}_8$		0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$, $\overline{G}_n$, $\overline{P}_n$ to $\overline{C}_2$, $\overline{C}_4$, $\overline{C}_6$, $\overline{C}_8$	Waveform 1	1.10 1.10	2.90 2.90	1.10 1.10	2.90 2.90	1.10 1.10	3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time $\overline{C}_2$, $\overline{C}_4$, $\overline{C}_6$, $\overline{C}_8$		0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	0.45 0.45	1.80 1.80	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$, $\overline{G}_n$, $\overline{P}_n$ to $\overline{C}_2$, $\overline{C}_4$, $\overline{C}_6$, $\overline{C}_8$	Waveform 1	1.10 1.10	2.70 2.70	1.10 1.10	2.70 2.70	1.10 1.10	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time $\overline{C}_2$, $\overline{C}_4$, $\overline{C}_6$, $\overline{C}_8$		0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

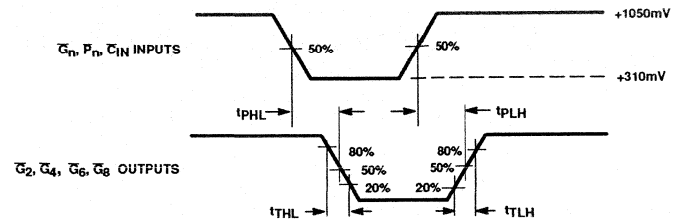
Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$, $\overline{G}_n$, $\overline{P}_n$ to $\overline{C}_2$, $\overline{C}_4$, $\overline{C}_6$, $\overline{C}_8$	Waveform 1	1.10 1.10	2.70 2.70	1.10 1.10	2.70 2.70	1.10 1.10	2.80 2.80	ns ns
t_{TLH} t_{THL}	Transition time $\overline{C}_2$, $\overline{C}_4$, $\overline{C}_6$, $\overline{C}_8$		0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	0.45 0.45	1.70 1.70	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

Carry Look–Ahead Generator 100179

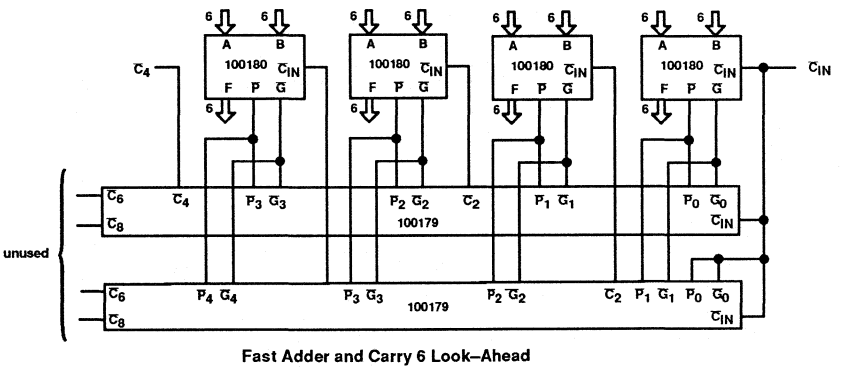
AC WAVEFORMS



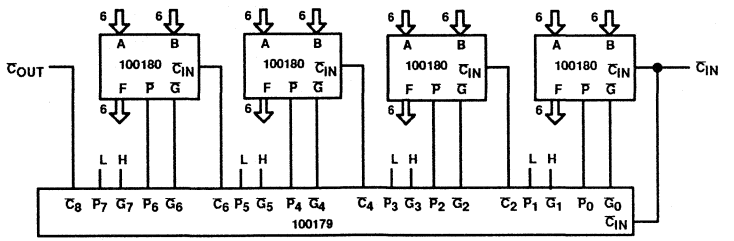
Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

APPLICATIONS INFORMATION



Fast Adder and Carry 6 Look–Ahead



24–Bit Adder Using One Carry Look–Ahead

Document No.	853–0633
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100180

High Speed 8–Bit Adder

FEATURES

- **Typical propagation delay: 2.35ns**
- **Typical supply current ($-I_{EE}$): 205mA**

DESCRIPTION

The 100180 is a high–speed adder that can add two six–bit operands (A_n, B_n) and an Active–Low carry input ($\overline{C}_{IN}$).

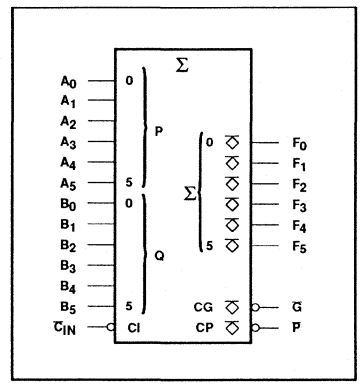
The sum is presented on the function outputs (F_n). When used in conjuction with the 100179, the carry generate and propagate outputs ($\overline{G}$ and $\overline{P}$) allow more than one 100180 to add operands larger than 6–bits.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_5$	Operand A Inputs
$B_0 - B_5$	Operand B Inputs
$\overline{C}_{IN}$	Carry Input (Active–Low)
$\overline{G}$	Carry Generate Output (Active–Low)
$\overline{P}$	Carry Propagate Output (Active–Low)
$F_0 - F_5$	Function Outputs

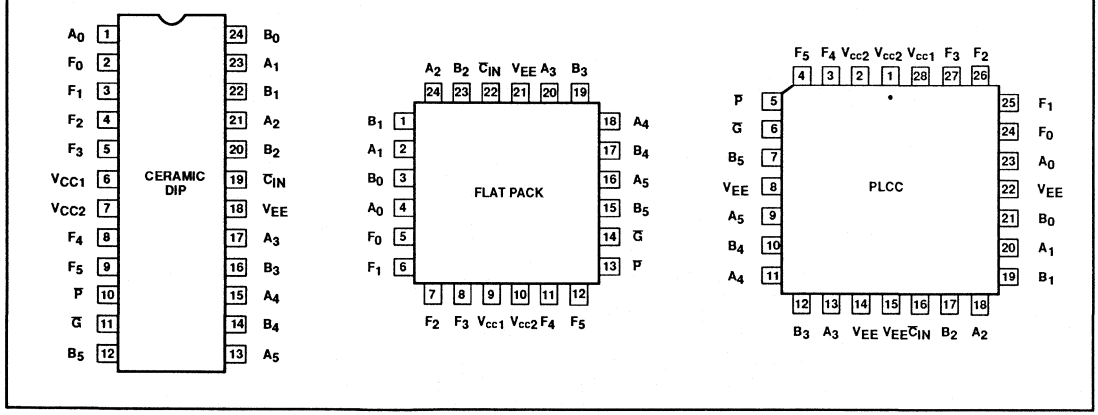
IEC/IEEE SYMBOL



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100180F
24–Pin Ceramic Flat Pack	100180Y
28–Pin PLCC	100180A

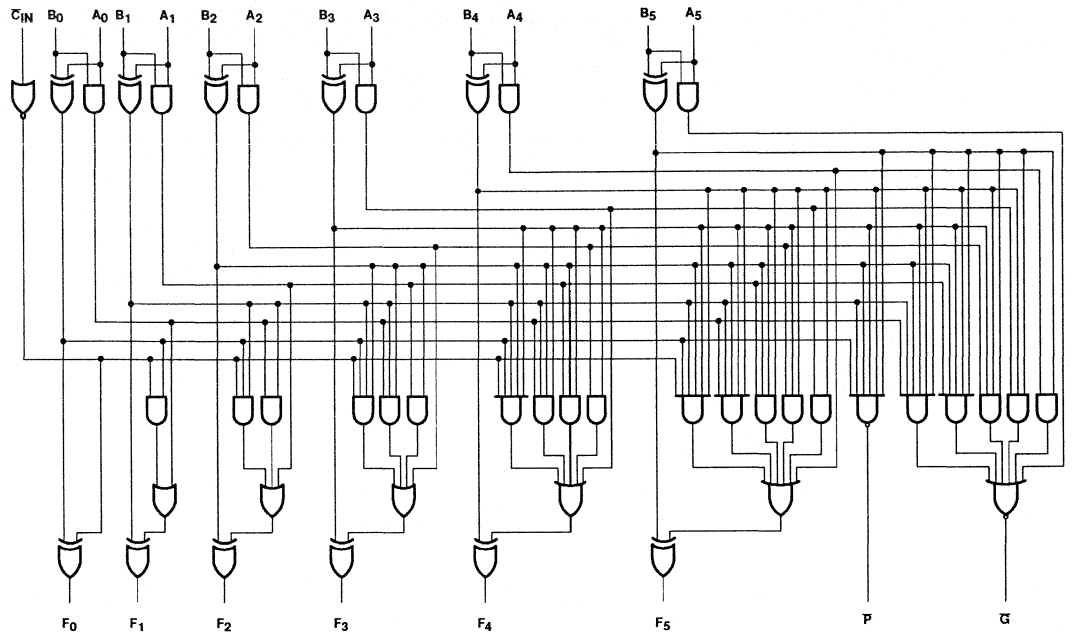
PIN CONFIGURATIONS



Adder

100180

LOGIC DIAGRAM



LOGIC EQUATIONS

$P_i = A_i \oplus B_i$

$G_i = A_i B_i$

$i = 0, 1, 2, 3, 4, 5$

$F_0 = P_0 \oplus C_{IN}$

$F_1 = P_1 \oplus (G_0 + P_0 C_{IN})$

$F_2 = P_2 \oplus (G_1 + P_1 G_0 + P_1 P_0 C_{IN})$

$F_3 = P_3 \oplus (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{IN})$

$F_4 = P_4 \oplus (G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_{IN})$

$F_5 = P_5 \oplus (G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 G_0 + P_4 P_3 P_2 P_1 P_0 C_{IN})$

$\overline{P} = \overline{P_0 P_1 P_2 P_3 P_4 P_5}$

$\overline{G} = \overline{G_5 + P_5 G_4 + P_5 P_4 G_3 + P_5 P_4 P_3 G_2 + P_5 P_4 P_3 P_2 G_1 + P_5 P_4 P_3 P_2 P_1 G_0}$

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electyrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					220	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}.			135	205	290	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = 0°C MIN.	LIMITS T_A = 0°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10 1.10	4.70 4.70	1.10 1.10	4.60 4.60	1.10 1.10	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$		1.00 1.00	3.00 3.00	1.00 1.00	3.00 3.00	1.00 1.00	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{G}$		1.10 1.10	3.90 3.90	1.20 1.20	3.80 3.80	1.20 1.20	3.90 3.90	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		0.90 0.90	4.00 4.00	0.90 0.90	3.90 3.90	0.90 0.90	4.00 4.00	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{P}$, $\overline{G}$		0.45 0.45	2.30 2.30	0.45 0.45	2.20 2.20	0.45 0.45	2.30 2.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10 1.10	4.70 4.70	1.10 1.10	4.60 4.60	1.10 1.10	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$		1.00 1.00	3.00 3.00	1.00 1.00	3.00 3.00	1.00 1.00	3.30 3.30	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{G}$		1.10 1.10	3.90 3.90	1.20 1.20	3.80 3.80	1.20 1.20	3.90 3.90	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		0.90 0.90	4.00 4.00	0.90 0.90	3.90 3.90	0.90 0.90	4.00 4.00	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{P}$, $\overline{G}$		0.45 0.45	2.30 2.30	0.45 0.45	2.20 2.20	0.45 0.45	2.30 2.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10 1.10	4.50 4.50	1.10 1.10	4.40 4.40	1.10 1.10	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$		1.00 1.00	2.80 2.80	1.00 1.00	2.80 2.80	1.00 1.00	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{G}$		1.10 1.10	3.70 3.70	1.20 1.20	3.60 3.60	1.20 1.20	3.70 3.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		0.90 0.90	3.80 3.80	0.90 0.90	3.70 3.70	0.90 0.90	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{P}$, $\overline{G}$		0.45 0.45	2.30 2.30	0.45 0.45	2.20 2.20	0.45 0.45	2.30 2.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

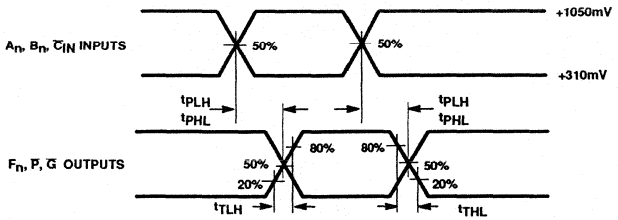
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	1.10 1.10	4.50 4.50	1.10 1.10	4.40 4.40	1.10 1.10	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to P		1.00 1.00	2.80 2.80	1.00 1.00	2.80 2.80	1.00 1.00	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{G}$		1.10 1.10	3.70 3.70	1.20 1.20	3.60 3.60	1.20 1.20	3.70 3.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		0.90 0.90	3.80 3.80	0.90 0.90	3.70 3.70	0.90 0.90	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{P}$, $\overline{G}$		0.45 0.45	2.30 2.30	0.45 0.45	2.20 2.20	0.45 0.45	2.30 2.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–1442
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100181

4–Bit Binary/BCD ALU

FEATURES

- **Typical propagation delay: 2.10ns**
- **Typical supply current ($-I_{EE}$): 205mA**

DESCRIPTION

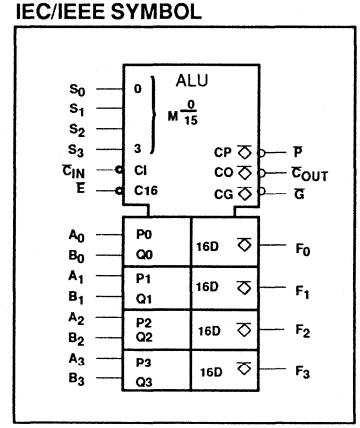
The 100181 is a 4–bit, binary/BCD arithmetic logic unit which performs eight arithmetic operations and eight logic operations on two four–bit words. Arithmetic and logic operations are selected by four select inputs (S_0–S_3). The circuit performs BCD as well as binary arithmetic. The A_n and B_n inputs accept the function arguments. The F_n outputs yield the function result. The circuit contains four output latches, which are transparent when the enable input ($\overline{E}$) is low. The Carry Input ($\overline{C}_{IN}$), Carry Output ($\overline{C}_{OUT}$), Carry Lookahead Propagate ($\overline{P}$), and Carry Lookahead Generate ($\overline{G}$) lines allow for parallel operation with two or more devices.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_3$	Operand A Inputs
$B_0 - B_3$	Operand B Inputs
$\overline{C}_{IN}$	Carry Input (Active–Low)
$S_0 - S_3$	Function Select Inputs
$\overline{E}$	Latch Enable input (Active Low)
$\overline{G}$	Carry Lookahead Generate Output (Active–Low)
$\overline{P}$	Carry Lookahead Propagate Output (Active–Low)
$\overline{C}_{OUT}$	Carry Output (Active–Low)
$F_0 - F_3$	Function Outputs

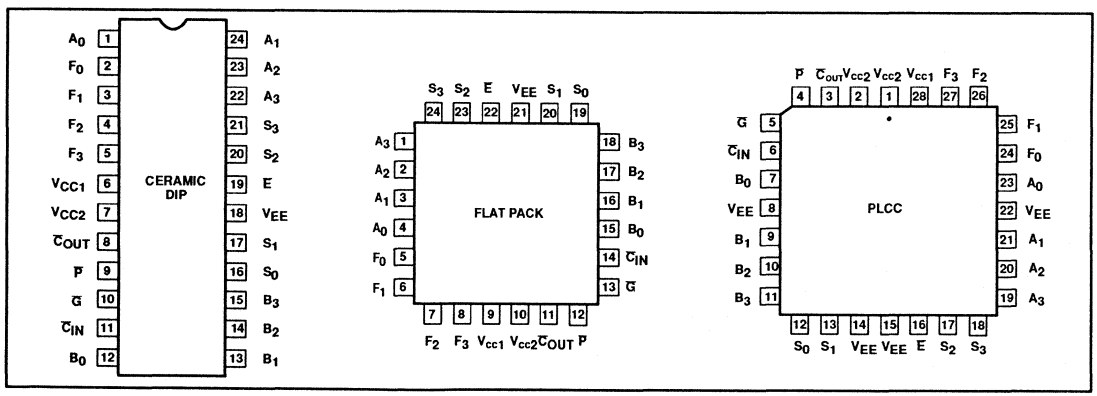
IEC/IEEE SYMBOL



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100181F
24–Pin Ceramic Flat Pack	100181Y
28–Pin PLCC	100181A

PIN CONFIGURATIONS



BINARY ARITHMETIC

When a binary addition operation is performed, F = A plus B plus C_{IN}, where A, B, and F are expressed in binary code.

For binary subtraction, F = A minus B plus C_{IN} = A plus B^1 plus C_{IN} where A and B are binary words and the superscript 1 designates one's complement. The circuit automatically takes the one's complement of word B by inverting bits B_0 through B_3. If the result is positive, then $\overline{C}_{OUT}$ will be low and the difference less one will be expressed in binary at F. If the result is negative or zero, $\overline{C}_{OUT}$ will be high and the difference will be expressed in one's complement at F. If a result in two's complement is desired, force $\overline{C}_{IN}$ low, since $F^2 = F^1 + 1$ (A superscript 2 denotes two's complement). The preceding description for binary subtraction holds true for the F = B minus A plus C_{IN} operation as well. Just switch the A and B variables.

BCD ARITHMETIC

When a BCD addition operation is performed, F = A plus B plus C_{IN}, where A, B, and F are expressed in BCD code.

The circuit automatically adds a +6 code correction to word B. Define a temporary variable F' = A plus B plus C_{IN} plus 6. If F' < 16, then a –6 code correction is performed: F = F' – 6 = A plus B plus C_{IN}. If F' ≥ 16, no further code correction is necessary, and F = F' = A plus B plus C_{IN} plus 6.

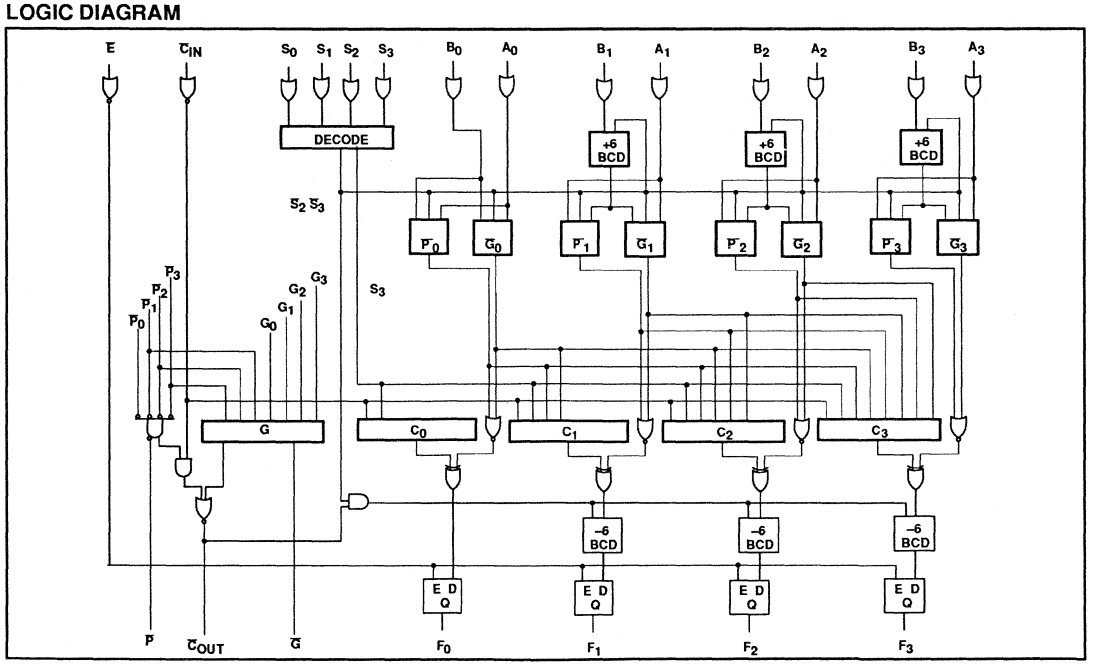
For BCD subtraction, F = A minus B plus $\overline{C}_{IN}$ = A plus B^9 plus C_{IN} where A and B are BCD words and the superscript 9 designates nine's complement. The circuit automatically takes the nine's complement of word B and then adds a +6 code correction. Define a temporary variable F' = A plus B^9 plus C_{IN} plus 6. If F' < 16, then a –6 code correction is performed: F = F' – 6 = A plus B^9 plus C_{IN}. if F' ≥ 16, no further code correction is necessary and F = F' = A plus B' plus C_{IN} plus 6. If the result is positive, then $\overline{C}_{OUT}$ will be low and the difference less one will be expressed in binary at F. If the result is negative or zero, $\overline{C}_{OUT}$ will be high and the difference will be expressed in nine's complement at F. If a result in 10's complement is desired, force $\overline{C}_{IN}$ low, since $F^{10} = F^9 + 1$ (A superscript 10 denotes 10's complement).

The preceding description for BCD subtraction holds true for the F = B minus A plus C_{IN} operation as well. Just switch the A and the B variables.

THE CARRY

Arithmetic on words larger than 4-bits can be performed by operating two or more 100181's together in parallel fashion. There are two possible arrangements: In the ripple–carry configuration, $\overline{C}_{OUT}$ of one stage is connected to $\overline{C}_{IN}$ of the next stage. The carry–lookahead configuration uses $\overline{P}$ and $\overline{G}$ in association with the 100179 (the Carry Lookahead Generator) or other external logic. With the addition of the 100179 chip, the carry–lookahead method offers faster adder throughput than the ripple–carry method. $\overline{P}$ goes low when a binary addition operation produces fifteen (nine for BCD), or when a minus operation produces zero. $\overline{G}$ goes low when the binary sum of A and B is greater than 15 (nine for BCD), or the difference of A and B is greater than zero.

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS				FUNCTION	OUTPUTS	
S_3	S_2	S_1	S_0		G_n	P_n
L	L	L	L	F = A plus B plus C_{IN} (BCD addition)	$A_n X_n$	$A_n + X_n$
L	L	L	H	F = A minus B plus C_{IN} (BCD subtraction)	$A_n Y_n$	$A_n + Y_n$
L	L	H	L	F = B minus A plus C_{IN} (BCD subtraction)	$A^9_n X_n$	$A^9_n + X_n$
L	L	H	H	F = 0 minus B plus C_{IN} (BCD subtraction)	0	Y_n
L	H	L	L	F = A plus B plus C_{IN} (Binary addition)	$A_n B_n$	$A_n + B_n$
L	H	L	H	F = A minus B plus C_{IN} (Binary subtraction)	$A_n \overline{B}_n$	$A_n + \overline{B}_n$
L	H	H	L	F = B minus A plus C_{IN} (Binary subtraction)	$\overline{A}_n B_n$	$\overline{A}_n + B_n$
L	H	H	H	F = 0 minus B plus C_{IN} (Binary subtraction)	0	$\overline{B}_n$
H	L	L	L	$F_n = A_n B_n + \overline{A}_n \overline{B}_n$ (Equivalence)	$A_n B_n$	$A_n + B_n$
H	L	L	H	$F_n = A_n \overline{B}_n + \overline{A}_n B_n$ (Exclusive OR)	$A_n \overline{B}_n$	$A_n + \overline{B}_n$
H	L	H	L	$F_n = A_n + B_n$ (OR)	A_n	$\overline{B}_n$
H	L	H	H	$F_n = A_n$	A_n	1
H	H	L	L	$F_n = \overline{B}_n$ (NOT)	0	B_n
H	H	L	H	$F_n = B_n$	0	$\overline{B}_n$
H	H	H	L	$F_n = A_n B_n$ (AND)	0	$\overline{A}_n + \overline{B}_n$
H	H	H	H	$F_n = 0$	0	1

NOTES:
H = High voltage level
L = Low voltage level
Overscore designates one's complement. Superscript "9" designates nine's complement.
All operations are described by $F_n = \overline{G_n + \overline{P}_n} \oplus C_n$ where n = 0 to 3, $\overline{P} = \overline{P}_0 + \overline{P}_1 + \overline{P}_2 + \overline{P}_3$ and $\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$
Internal equation for carry lookahead:
$C_0 = C_{IN} + S_3$
$C_1 = G_0 + P_0C_{IN} + S_3$
$C_2 = G_1 + P_1G_0 + P_1P_0C_{IN} + S_3$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_{IN} + S_3$
$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_{IN} = C_{OUT}$

+6 correction for BCD operations (B + 6):
$X_0 = B_0$
$X_1 = \overline{B}_1$
$X_2 = B_1 B_2 + \overline{B}_1\overline{B}_2$
$X_3 = \overline{B}_1 \overline{B}_2 B_3 + B_2\overline{B}_3 + B_1\overline{B}_3$

+6 correction for BCD operations (B^9 + 6)
$Y_0 = B_0^9$
$Y_1 = \overline{B_1^9}$
$Y_2 = B_1^9 B_2^9 + \overline{B_1^9}\,\overline{B_2^9}$
$Y_3 = \overline{B_1^9}\,\overline{B_2^9} B_3^9 + B_2^9\overline{B_3^9} + B_1^9\overline{B_3^9}$

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	S_n, $\overline{E}$	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					300	µA
		others						190	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			130	205	300	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	2.00 2.00	6.90 6.90	2.10 2.10	6.80 6.80	2.30 2.30	7.40 7.40	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$, $\overline{G}$		1.40 1.40	4.70 4.70	1.40 1.40	4.40 4.40	1.40 1.40	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{C}_{OUT}$		2.00 2.00	6.50 6.50	2.00 2.00	6.50 6.50	2.10 2.10	6.80 6.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		1.60 1.60	5.10 5.10	1.60 1.60	5.20 5.20	1.60 1.60	5.50 5.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to $\overline{C}_{OUT}$		1.30 1.30	3.00 3.00	1.40 1.40	3.00 3.00	1.40 1.40	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to F_n		1.40 1.40	8.80 8.80	1.50 1.50	8.60 8.60	1.50 1.50	9.00 9.00	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$, $\overline{G}$		1.70 1.70	7.40 7.40	2.00 2.00	5.90 5.90	2.00 2.00	6.50 6.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{C}_{OUT}$		2.70 2.70	10.1 10.1	2.80 2.80	8.50 8.50	2.90 2.90	8.70 8.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to F_n		1.00 1.00	3.40 3.40	0.90 0.90	3.60 3.60	1.10 1.10	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{C}_{OUT}$, $\overline{P}$, $\overline{G}$		0.45 0.45	2.70 2.70	0.45 0.45	2.60 2.60	0.45 0.45	2.70 2.70	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}$	Waveform 2	6.00		6.00		6.00		ns
t_h	Hold time, $\overline{E}$ to A_n, B_n		0.10		0.10		0.10		ns
t_s	Setup time, S_n to $\overline{E}$		7.00		7.00		7.00		ns
t_h	Hold time, $\overline{E}$ to S_n		0.60		0.60		0.60		ns
t_s	Setup time, $\overline{C}_{IN}$ to $\overline{E}$		4.00		4.00		4.00		ns
t_h	Hold time, $\overline{E}$ to $\overline{C}_{IN}$		0.60		0.60		0.60		ns
$t_{w(L)}$	Pulse width Low, $\overline{E}$	Waveform 1	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	2.00 2.00	6.90 6.90	2.10 2.10	6.80 6.80	2.30 2.30	7.40 7.40	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$, $\overline{G}$		1.40 1.40	4.70 4.70	1.40 1.40	4.40 4.40	1.40 1.40	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{C}_{OUT}$		2.00 2.00	6.50 6.50	2.00 2.00	6.50 6.50	2.10 2.10	6.80 6.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		1.60 1.60	5.10 5.10	1.60 1.60	5.20 5.20	1.60 1.60	5.50 5.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to $\overline{C}_{OUT}$		1.30 1.30	3.00 3.00	1.40 1.40	3.00 3.00	1.40 1.40	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to F_n		1.40 1.40	8.80 8.80	1.50 1.50	8.60 8.60	1.50 1.50	9.00 9.00	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$, $\overline{G}$		1.70 1.70	7.40 7.40	2.00 2.00	5.90 5.90	2.00 2.00	6.50 6.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{C}_{OUT}$		2.70 2.70	10.1 10.1	2.80 2.80	8.50 8.50	2.90 2.90	8.70 8.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to F_n		1.00 1.00	3.40 3.40	0.90 0.90	3.60 3.60	1.10 1.10	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{C}_{OUT}$, $\overline{P}$, $\overline{G}$		0.45 0.45	2.70 2.70	0.45 0.45	2.60 2.60	0.45 0.45	2.70 2.70	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}$	Waveform 2	6.00		6.00		6.00		ns
t_h	Hold time, $\overline{E}$ to A_n, B_n		0.10		0.10		0.10		ns
t_s	Setup time, S_n to $\overline{E}$		7.00		7.00		7.00		ns
t_h	Hold time, $\overline{E}$ to S_n		0.60		0.60		0.60		ns
t_s	Setup time, $\overline{C}_{IN}$ to $\overline{E}$		4.00		4.00		4.00		ns
t_h	Hold time, $\overline{E}$ to $\overline{C}_{IN}$		0.60		0.60		0.60		ns
$t_{w(L)}$	Pulse width Low, $\overline{E}$	Waveform 1	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	2.00 2.00	6.70 6.70	2.10 2.10	6.60 6.60	2.30 2.30	7.20 7.20	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$, $\overline{G}$		1.40 1.40	4.50 4.50	1.40 1.40	4.20 4.20	1.40 1.40	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{C}_{OUT}$		2.00 2.00	6.30 6.30	2.00 2.00	6.30 6.30	2.10 2.10	6.60 6.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		1.60 1.60	4.90 4.90	1.60 1.60	5.00 5.00	1.60 1.60	5.30 5.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to $\overline{C}_{OUT}$		1.30 1.30	2.80 2.80	1.40 1.40	2.80 2.80	1.40 1.40	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to F_n		1.40 1.40	8.60 8.60	1.50 1.50	8.40 8.40	1.50 1.50	8.80 8.80	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$, $\overline{G}$		1.70 1.70	7.20 7.20	2.00 2.00	5.70 5.70	2.00 2.00	6.30 6.30	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{C}_{OUT}$		2.70 2.70	9.90 9.90	2.80 2.80	8.30 8.30	2.90 2.90	8.50 8.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to F_n		1.00 1.00	3.20 3.20	0.90 0.90	3.40 3.40	1.10 1.10	3.60 3.60	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{C}_{OUT}$, $\overline{P}$, $\overline{G}$		0.45 0.45	2.60 2.60	0.45 0.45	2.50 2.50	0.45 0.45	2.60 2.60	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}$	Waveform 2	6.00		6.00		6.00		ns
t_h	Hold time, $\overline{E}$ to A_n, B_n		0.00		0.00		0.00		ns
t_s	Setup time, S_n to $\overline{E}$		7.00		7.00		7.00		ns
t_h	Hold time, $\overline{E}$ to S_n		0.50		0.50		0.50		ns
t_s	Setup time, $\overline{C}_{IN}$ to $\overline{E}$		4.00		4.00		4.00		ns
t_h	Hold time, $\overline{E}$ to $\overline{C}_{IN}$		0.50		0.50		0.50		ns
$t_{w(L)}$	Pulse width Low, E	Waveform 1	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

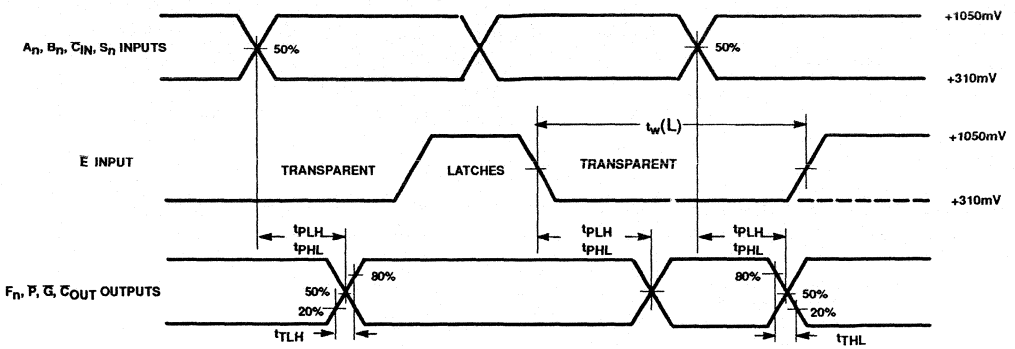
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

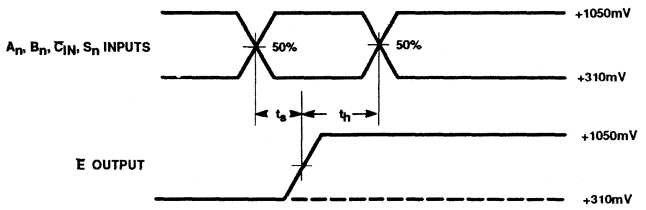
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	2.00 2.00	6.70 6.70	2.10 2.10	6.60 6.60	2.30 2.30	7.20 7.20	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$, $\overline{G}$		1.40 1.40	4.50 4.50	1.40 1.40	4.20 4.20	1.40 1.40	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{C}_{OUT}$		2.00 2.00	6.30 6.30	2.00 2.00	6.30 6.30	2.10 2.10	6.60 6.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		1.60 1.60	4.90 4.90	1.60 1.60	5.00 5.00	1.60 1.60	5.30 5.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to $\overline{C}_{OUT}$		1.30 1.30	2.80 2.80	1.40 1.40	2.80 2.80	1.40 1.40	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to F_n		1.40 1.40	8.60 8.60	1.50 1.50	8.40 8.40	1.50 1.50	8.80 8.80	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$, $\overline{G}$		1.70 1.70	7.20 7.20	2.00 2.00	5.70 5.70	2.00 2.00	6.30 6.30	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{C}_{OUT}$		2.70 2.70	9.90 9.90	2.80 2.80	8.30 8.30	2.90 2.90	8.50 8.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to F_n		1.00 1.00	3.20 3.20	0.90 0.90	3.40 3.40	1.10 1.10	3.60 3.60	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{C}_{OUT}$, $\overline{P}$, $\overline{G}$		0.45 0.45	2.60 2.60	0.45 0.45	2.50 2.50	0.45 0.45	2.60 2.60	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}$	Waveform 2	6.00		6.00		6.00		ns
t_h	Hold time, $\overline{E}$ to A_n, B_n		0.00		0.00		0.00		ns
t_s	Setup time, S_n to $\overline{E}$		7.00		7.00		7.00		ns
t_h	Hold time, $\overline{E}$ to S_n		0.50		0.50		0.50		ns
t_s	Setup time, $\overline{C}_{IN}$ to $\overline{E}$		4.00		4.00		4.00		ns
t_h	Hold time, $\overline{E}$ to $\overline{C}_{IN}$		0.50		0.50		0.50		ns
$t_{w(L)}$	Pulse width Low, $\overline{E}$	Waveform 1	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times



Waveform 2. Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

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100231

Triple D–Type Master–Slave Flip–Flop

FEATURES

- **Typical propagation delay: 1.3ns**
- **Typical supply current ($-I_{EE}$): 110mA**

DESCRIPTION

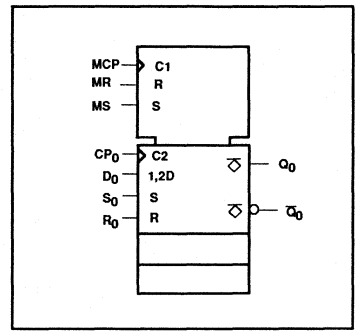
The 100231 is a high–speed version of the 100131. 100231 has three D–type master–slave flip–flops with true and complementary outputs. In addition to common clock, set and reset lines, each flip–flop also has individual clock, set and reset lines.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_2$	Data Inputs
MCP	Master Clock Input
$CP_0 - CP_2$	Individual Clock Inputs
MS	Master Set Input
$S_0 - S_2$	Individual Set Inputs
MR	Master Reset Input
$R_0 - R_2$	Individual Reset Input
$Q_0 - Q_2$	True Data Outputs
$\overline{Q}_0 - \overline{Q}_2$	Complementary Data Outputs

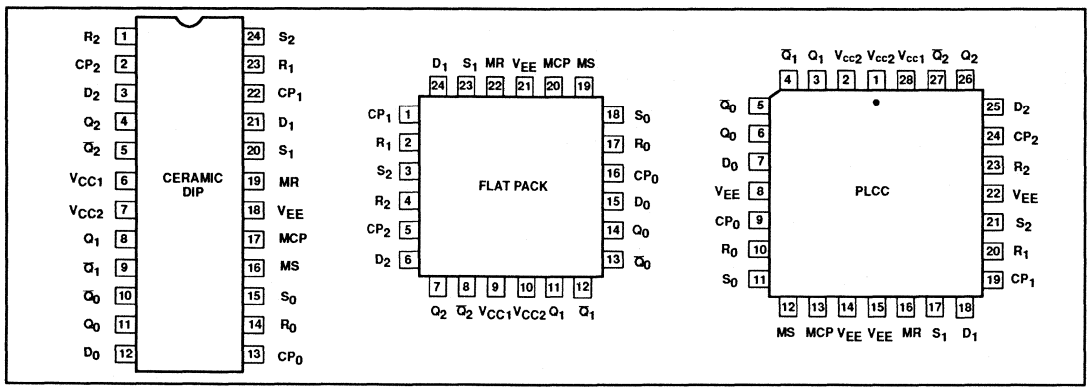
IEC/IEEE SYMBOL



ORDERING INFORMATION

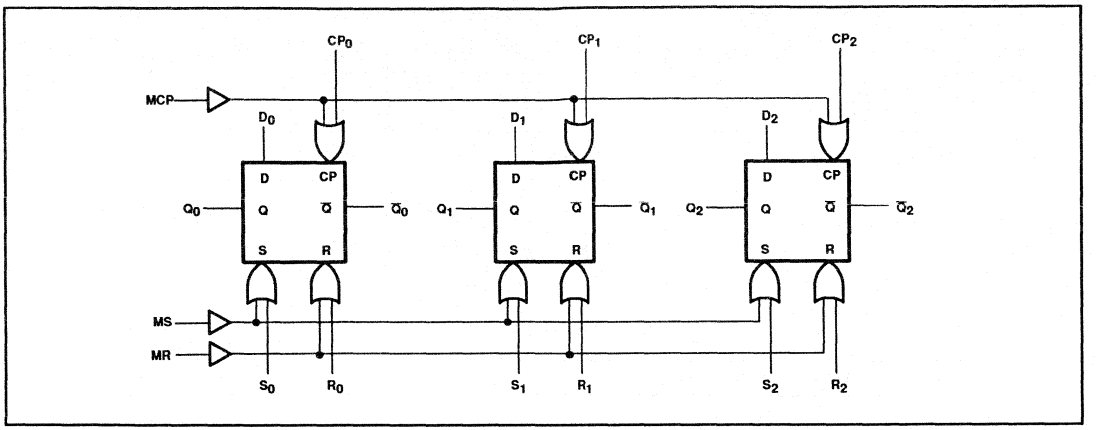
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100231F
24–Pin Ceramic Flat Pack	100231Y
28–Pin PLCC	100231A

PIN CONFIGURATIONS



Flip–Flop 100231

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS	
D	MCP	CP_n	MS	S_n	MR	R_n	Q_n	$\overline{Q}_n$
X	X	X	L	L	H	X	L	H
X	X	X	L	L	X	H	L	H
X	X	X	H	X	L	L	H	L
X	X	X	X	H	L	L	H	L
X	X	X	H	X	H	X	undefined	
X	X	X	H	X	X	H	undefined	
X	X	X	X	H	H	X	undefined	
X	X	X	X	H	X	H	undefined	
H	↑	L	L	L	L	L	H	L
L	↑	L	L	L	L	L	L	H
H	L	↑	L	L	L	L	H	L
L	L	↑	L	L	L	L	L	H
X	↕	↕	L	L	L	L	NC	NC

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low–to–High transition
↕ = No Low–to–High transition
NC = No change

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, $T_A = 0°C$ to $+85°C$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

Flip–Flop 100231

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the I0KH ECL family.		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	D_n, CP_n	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					240	µA
		MCP, MS, MR						450	µA
		R_n, S_n						530	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			74	110	149	mA

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.

NOTES (CONTINUED):

3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP V_{CC1} = V_{CC2} = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS						UNIT
				T_A = 0°C		T_A = +25°C		T_A = +85°C		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1		400		400		400		MHz
t_{PLH} t_{PHL}	Propagation delay MCP to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.75 0.75	2.00 2.00	0.75 0.75	2.00 2.00	0.70 0.70	2.05 2.05	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.70 0.70	1.80 1.80	0.70 0.70	1.80 1.80	0.70 0.70	1.80 1.80	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveforms 2,3	$CP_n = V_{ILMIN}$	1.05 1.05	2.50 2.50	1.05 1.05	2.50 2.50	1.05 1.05	2.50 2.50	ns ns
t_{PLH} t_{PHL}	MS, MR to Q_n, $\overline{Q}_n$		$CP_n = V_{IHMAX}$	1.10 1.10	2.80 2.80	1.10 1.10	2.80 2.80	1.10 1.10	2.80 2.80	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveforms 2,3	$CP_n = V_{ILMIN}$	0.65 0.65	1.70 1.70	0.70 0.70	1.70 1.70	0.70 0.70	1.90 1.90	ns ns
t_{PLH} t_{PHL}	R_n, S_n to Q_n, $\overline{Q}_n$		$CP_n = V_{IHMAX}$	0.70 0.70	2.00 2.00	0.70 0.70	1.90 1.90	0.70 0.70	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1		0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to CP_n, MCP	Waveforms 2,3		0.90		0.70		0.90		ns
t_h	Hold time CP_n, MCP to D_n			0.60		0.60		0.80		ns
t_R	Release time R_n, S_n to CP_n, MCP	Waveforms 2,3		1.50		1.30		1.50		ns
t_R	Release time MR, MS to CP_n, MCP			2.50		2.30		2.50		ns
$t_w(H)$	Pulse width High MR, MS, R_n, S_n, CP_n, MCP	Waveforms 1,2,3		2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS						UNIT
				$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1		400		400		400		MHz
t_{PLH} t_{PHL}	Propagation delay MCP to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.75 0.75	2.00 2.00	0.75 0.75	2.00 2.00	0.70 0.70	2.05 2.05	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.70 0.70	1.80 1.80	0.70 0.70	1.80 1.80	0.70 0.70	1.80 1.80	ns ns
t_{PLH} t_{PHL}	Propagation delay MS, MR to Q_n, $\overline{Q}_n$	Waveforms 2,3	$CP_n = V_{ILMIN}$	1.05 1.05	2.50 2.50	1.05 1.05	2.50 2.50	1.05 1.05	2.50 2.50	ns ns
t_{PLH} t_{PHL}			$CP_n = V_{IHMAX}$	1.10 1.10	2.80 2.80	1.10 1.10	2.80 2.80	1.10 1.10	2.80 2.80	ns ns
t_{PLH} t_{PHL}	Propagation delay R_n, S_n to Q_n, $\overline{Q}_n$	Waveforms 2,3	$CP_n = V_{ILMIN}$	0.65 0.65	1.70 1.70	0.70 0.70	1.70 1.70	0.70 0.70	1.90 1.90	ns ns
t_{PLH} t_{PHL}			$CP_n = V_{IHMAX}$	0.70 0.70	2.00 2.00	0.70 0.70	1.90 1.90	0.70 0.70	2.20 2.20	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1		0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to CP_n, MCP	Waveforms 2,3		0.90		0.70		0.90		ns
t_h	Hold time CP_n, MCP to D_n			0.60		0.60		0.80		ns
t_R	Release time R_n, S_n to CP_n, MCP	Waveforms 2,3		1.50		1.30		1.50		ns
t_R	Release time MR, MS to CP_n, MCP			2.50		2.30		2.50		ns
$t_w(H)$	Pulse width High MR, MS, R_n, S_n, CP_n, MCP	Waveforms 1,2,3		2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS						UNIT
				T_A = 0°C		T_A = +25°C		T_A = +85°C		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1		400		400		400		MHz
t_{PLH} t_{PHL}	Propagation delay MCP to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.75 0.75	1.80 1.80	0.75 0.75	1.80 1.80	0.70 0.70	1.85 1.85	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.70 0.70	1.60 1.60	0.70 0.70	1.60 1.60	0.70 0.70	1.70 1.70	ns ns
t_{PLH} t_{PHL}	Propagation delay MS, MR to Q_n, $\overline{Q}_n$	Waveforms 2,3	$CP_n = V_{ILMIN}$	1.05 1.05	2.30 2.30	1.05 1.05	2.30 2.30	1.05 1.05	2.40 2.40	ns ns
t_{PLH} t_{PHL}			$CP_n = V_{IHMAX}$	1.10 1.10	2.60 2.60	1.10 1.10	2.50 2.50	1.10 1.10	2.70 2.70	ns ns
t_{PLH} t_{PHL}	Propagation delay R_n, S_n to Q_n, $\overline{Q}_n$	Waveforms 2,3	$CP_n = V_{ILMIN}$	0.65 0.65	1.50 1.50	0.70 0.70	1.50 1.50	0.70 0.70	1.70 1.70	ns ns
t_{PLH} t_{PHL}			$CP_n = V_{IHMAX}$	0.70 0.70	1.80 1.80	0.70 0.70	1.70 1.70	0.70 0.70	2.00 2.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1		0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to CP_n, MCP	Waveforms 2,3		0.80		0.60		0.80		ns
t_h	Hold time CP_n, MCP to D_n			0.50		0.50		0.70		ns
t_R	Release time R_n, S_n to CP_n, MCP	Waveforms 2,3		1.40		1.20		1.40		ns
t_R	Release time MR, MS to CP_n, MCP			2.40		2.20		2.40		ns
$t_w(H)$	Pulse width High MR, MS, R_n, S_n, CP_n, MCP	Waveforms 1,2,3		2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

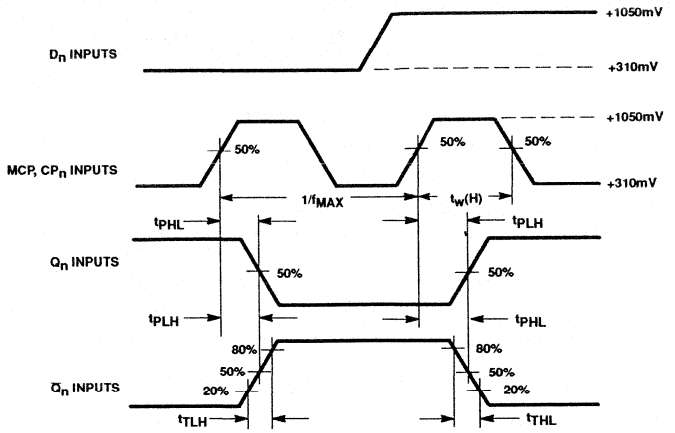
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}, V_{EE} = -5.2V \pm 5\%$

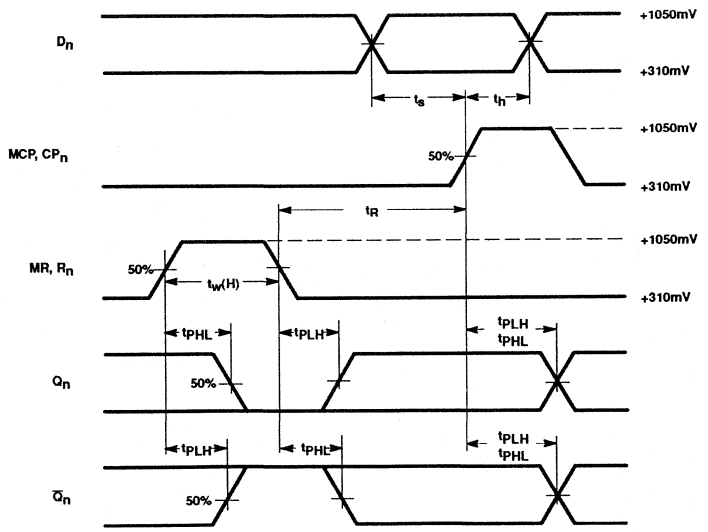
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS						UNIT
				$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum toggle frequency CP_n	Waveform 1		400		400		400		MHz
t_{PLH} t_{PHL}	Propagation delay MCP to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.75 0.75	1.80 1.80	0.75 0.75	1.80 1.80	0.70 0.70	1.85 1.85	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	Waveforms 1,2,3		0.70 0.70	1.60 1.60	0.70 0.70	1.60 1.60	0.70 0.70	1.70 1.70	ns ns
t_{PLH} t_{PHL}	Propagation delay MS, MR to Q_n, $\overline{Q}_n$	Waveforms 2,3	$CP_n = V_{ILMIN}$	1.05 1.05	2.30 2.30	1.05 1.05	2.30 2.30	1.05 1.05	2.40 2.40	ns ns
t_{PLH} t_{PHL}			$CP_n = V_{IHMAX}$	1.10 1.10	2.60 2.60	1.10 1.10	2.50 2.50	1.10 1.10	2.70 2.70	ns ns
t_{PLH} t_{PHL}	Propagation delay R_n, S_n to Q_n, $\overline{Q}_n$	Waveforms 2,3	$CP_n = V_{ILMIN}$	0.65 0.65	1.50 1.50	0.70 0.70	1.50 1.50	0.70 0.70	1.70 1.70	ns ns
t_{PLH} t_{PHL}			$CP_n = V_{IHMAX}$	0.70 0.70	1.80 1.80	0.70 0.70	1.70 1.70	0.70 0.70	2.00 2.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$	Waveform 1		0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to CP_n, MCP	Waveforms 2,3		0.80		0.60		0.80		ns
t_h	Hold time CP_n, MCP to D_n			0.50		0.50		0.70		ns
t_R	Release time R_n, S_n to CP_n, MCP	Waveforms 2,3		1.40		1.20		1.40		ns
t_R	Release time MR, MS to CP_n, MCP			2.40		2.20		2.40		ns
$t_w(H)$	Pulse width High MR, MS, R_n, S_n, CP_n, MCP	Waveforms 1,2,3		2.50		2.50		2.50		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



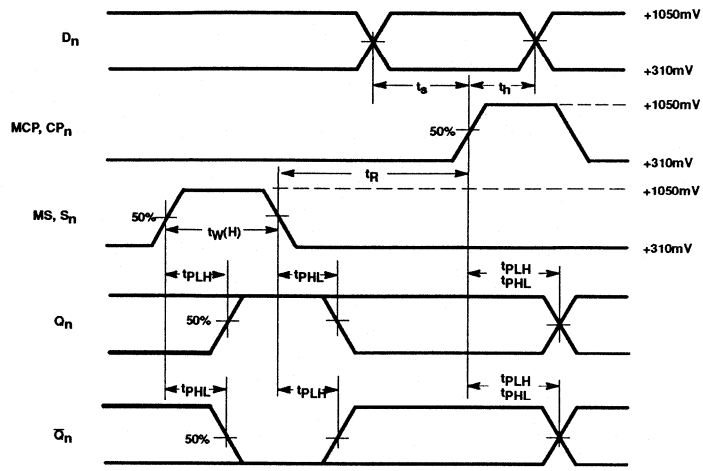
Waveform 1. Propagation Delays and Transition Times



Waveform 2. Reset, Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

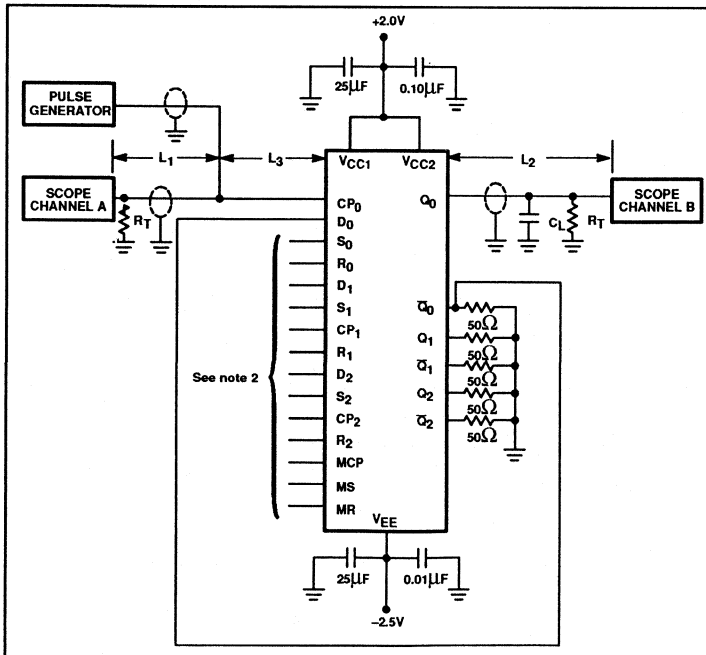
AC WAVEFORMS



Waveform 3. Set, Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

TOGGLE FREQUENCY TEST CIRCUIT



NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	
ECN No.	
Date of Issue	June 18, 1990
Status	Preliminary Specification
ECL Products	

100255

Quint ECL–TTL Translating Transceiver

FEATURES

- **Typical propagation delay from ECL input to TTL output: 3.2ns**
- **Typical propagation delay from TTL input to ECL output: 1.6ns**
- **Typical ECL supply current ($-I_{EE}$): 105mA**
- **Typical TTL supply current (I_{TTL}): 76mA**
- **ECL output has three–state capability**
- **ECL output drives 25 Ohm loads**

DESCRIPTION

The 100255 is a five–bit, inverting, translating transceiver. It allows the exchange of data between a 100K ECL bus and a TTL bus. The A data lines are bidirectional with 100K ECL compatibility and three–state capability. The B data lines are bidirectional with TTL compatibility and three–state capability. The control lines require 100K ECL input levels.

The Direction Control, DIR, selects the data flow path (A_n to B_n or B_n to A_n). A Low on the Chip Enable, CE, puts both the A_n and the B_n lines into a high impedance state. Each A_n output can drive a load as low as 25 Ohms (i.e. a 50 Ohm bus terminated at each end with 50 Ohms to –2.0V).

The GND_1 line is associated with all the TTL circuitry, the ECL internal logic, and the ECL reference generator. GND_2 services the ECL outputs.

Power may be applied to the V_{EE} and V_{TTL} pins in any order.

All unused inputs can be left open due to integrated pull–down resistors.

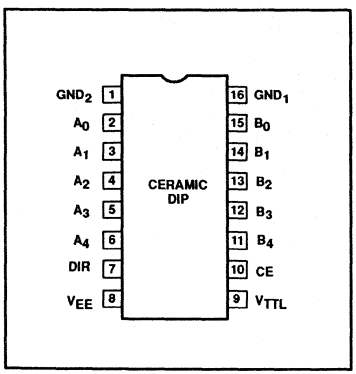
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Ceramic DIP (300 mils wide)	100255F

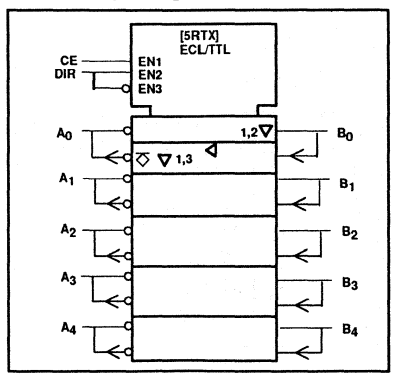
PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_4$	Bidirectional data lines (100K ECL compatible)
$B_0 - B_4$	Bidirectional data lines (TTL compatible)
DIR	Direction control input (100K ECL compatible)
CE	Chip enable input (100K ECL compatible)

PIN CONFIGURATION

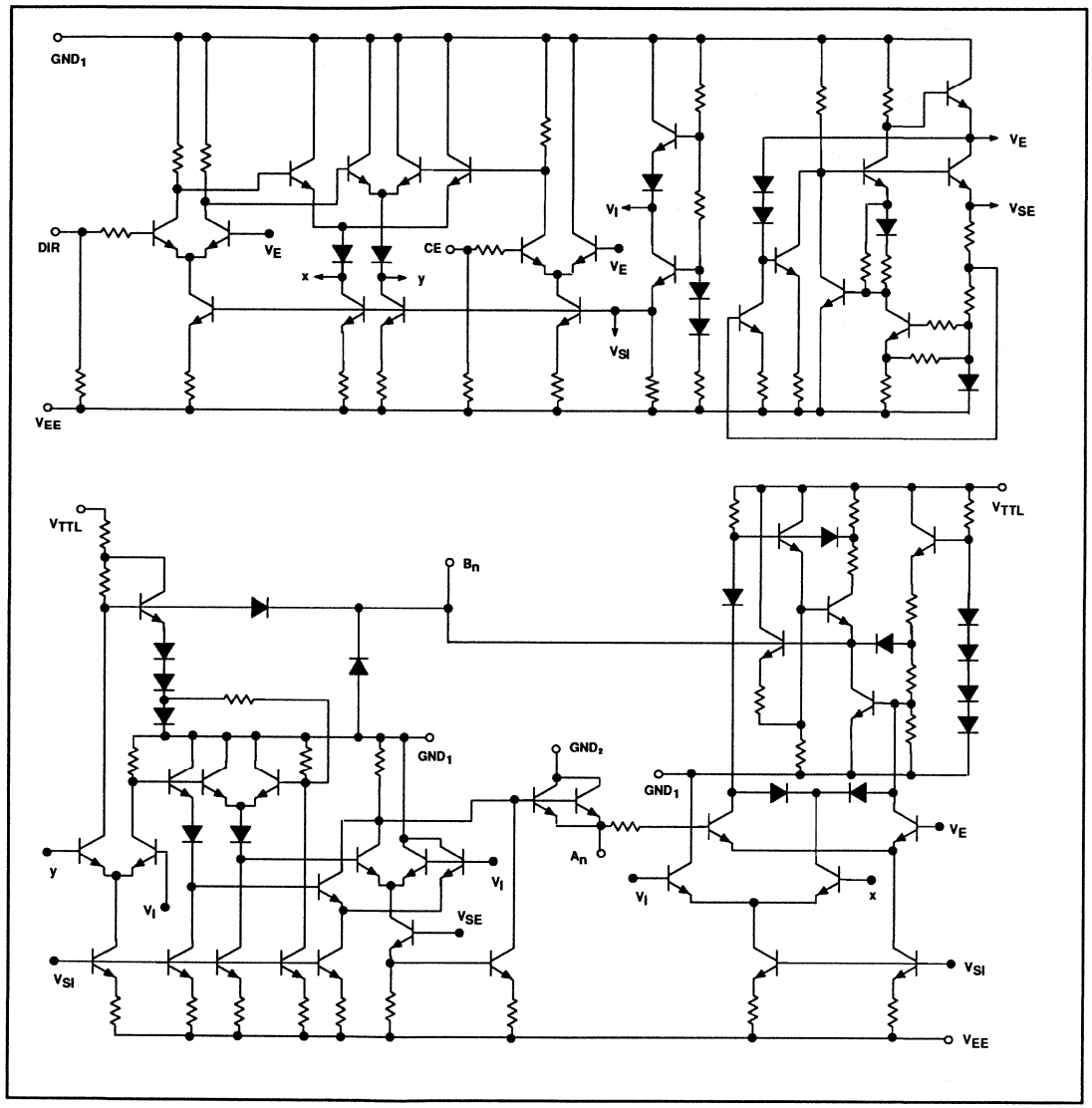


IEC/IEEE SYMBOL



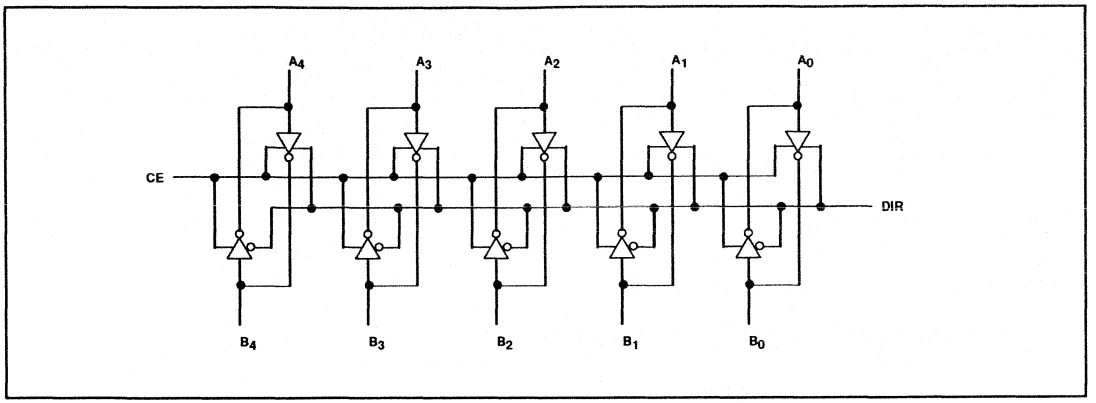
Translating Transceiver 100255

SIMPLIFIED SCHEMATIC



Translating Transceiver 100255

LOGIC DIAGRAM



NOTE:
Pins B_0 through B_4 are compatible with TTL. Pins CE, DIR, and A_0 through A_4 are compatible with 100K ECL.

FUNCTION TABLE

CONTROL		DATA		OPERATING MODE
CE	DIR	A_n	B_n	
L	X	Z	Z	A_n and B_n in high impedance state
H H	H H	L H	H L	Data flows from A_n to B_n (ECL–to–TTL translation)
H H	L L	L H	H L	Data flows from B_n to A_n (TTL–to–ECL translation)

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance state

ABSOLUTE MAXIMUM RATINGS FOR ECL–COMPATIBLE LINES

$GND_1 = GND_2$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	ECL supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–100	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

ABSOLUTE MAXIMUM RATINGS FOR TTL–COMPATIBLE LINES

$GND_1 = GND_2$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{TTL}	TTL supply voltage range	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to V_{TTL}	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to B_n in High state	–0.5 to V_{TTL}	V
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS FOR ECL–COMPATIBLE LINES

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
GND_1, GND_2	Circuit ground		0	0	0	V
V_{EE}	ECL supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	ECL supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V			–1475	mV
		V_{EE} = –4.5V	–1810		–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC OPERATING CONDITIONS FOR TTL–COMPATIBLE LINES

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{TTL}	TTL supply voltage	+4.5	+5.0	+5.5	V
V_{IH}	High level input voltage	+2.0			V
V_{IL}	Low level input voltage			+0.8	V
$-I_{OH}$	High level output current			2	mA
I_{OL}	Low level output current			20	mA
T_A	Operating ambient temperature range	0	+25	+85	°C

Translating Transceiver 100255

DC ELECTRICAL CHARACTERISTICS FOR ECL–COMPATIBLE LINES

$GND_1 = GND_2$ = ground, V_{EE} = –4.8V to –4.2V, V_{TTL} = 4.5V to 5.5V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		DIR at V_{ILMIN}. CE at V_{IHMAX}. A_n loaded with 25Ω to –2.0V ± 0.010V.	B_n at 0.4V.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			B_n at 0.8V.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			B_n at 2.0V.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			B_n at 2.4V.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current[5]	DIR, CE	One control input under test at V_{IHMAX}, other control input at V_{ILMIN}. A_n and B_n are open.					350	µA
		A_n	One A_n under test at V_{IHMAX}, all other A_n at V_{ILMIN}. CE and DIR at V_{IHMAX}.					350	µA
I_{IL}	Low level input current for DIR and CE		One control input under test at V_{ILMIN}, other control input at V_{IHMAX}. A_n and B_n are open.			+0.5			µA
I_{OZ}	Off–state output current[6]		One A_n under test at –2.1V, all other A_n open. B_n, CE and DIR at V_{ILMIN}.			–50		50	µA
$-I_{EE}$	ECL supply current		CE at V_{IHMAX}.			60	105	150	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for extended V_{EE} range. For more information, see Chapter 10, sexction 4.
5. For bidirectional lines, this parameter includes output leakage current.
6. This parameter includes input reverse leakage current.

DC ELECTRICAL CHARACTERISTICS FOR TTL–COMPATIBLE LINES

$GND_1 = GND_2$ = ground, V_{EE} = –4.8V to –4.2V, V_{TTL} = 4.5V to 5.5V, T_A = 0°C to +85°C unless otherwise specified[1,3]

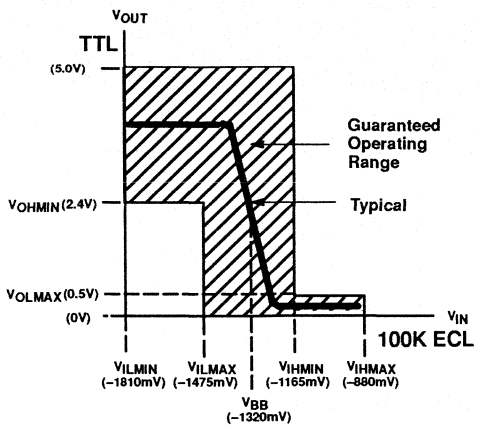
SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS			UNIT
			MIN.	TYP.	MAX.	
V_{OH}	High level output voltage	A_n at V_{ILMAX}, DIR and CE at V_{IHMAX}, I_{OH} = –2.0mA.	2.4			V
V_{OL}	Low level output voltage	A_n at V_{IHMIN}, DIR and CE at V_{IHMAX}, I_{OL} = +20mA.		0.35	0.50	V
V_{IK}	Input clamp voltage	Apply –18mA to B_n under test with other B_n open. CE at V_{ILMIN}.	–1.2	–0.73		V
I_I	Input current at maximum input voltage[4]	B_n under test at +5.5V, other B_n at ground. CE at V_{ILMIN}. V_{TTL} at +5.5V.			1.0	mV
I_{IH}	High level input current[4]	B_n under test at +2.4V, other B_n at ground. CE at V_{IHMAX}. DIR at V_{ILMIN}.			40	µA
$-I_{IL}$	Low level input current[4]	B_n under test at +0.4V, other B_n at +2.4V. CE at V_{IHMAX}. DIR at V_{ILMIN}.			1.6	mA
I_{OZH}	Off–state output current, High level voltage applied[5]	B_n at +2.4V. A_n at V_{ILMAX}. CE at V_{ILMIN}. DIR at V_{IHMAX}.			40	µA
$-I_{OZL}$	Off–state output current, Low level voltage applied[5]	B_n at +0.4V. A_n at V_{IHMIN}. CE at V_{ILMIN}. DIR at V_{IHMAX}.			40	µA
$-I_{OS}$	Short circuit output current[6]	A_n at V_{ILMIN}. One B_n under test at ground. V_{TTL} at +5.5V. DIR and CE at V_{IHMAX}.	40		130	mA
I_{TTLH}	TTL supply current with outputs High	All A_n at V_{ILMIN}. V_{TTL} at +5.5V. All B_n open. DIR and CE at V_{IHMAX}.	25	35	44	mA
I_{TTLL}	TTL supply current with outputs Low	All A_n at V_{IHMAX}. V_{TTL} at +5.5V. All B_n open. CE and DIR at V_{IHMAX}.	19	35	44	mA
I_{TTLZ}	TTL supply current with outputs in the high impedance state	V_{TTL} at +5.5V. All B_n open. CE at V_{ILMIN}.	25	44	48	mA

NOTES:

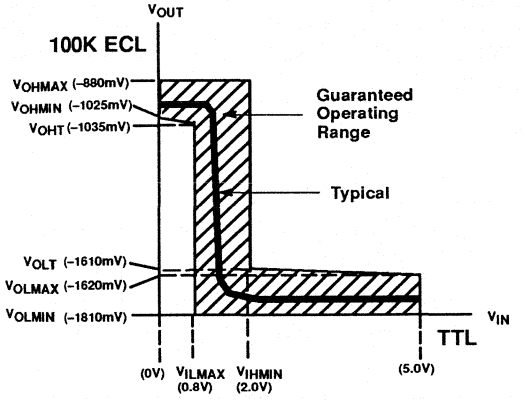
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply volage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. This parameter includes output leakage current.
5. This parameter includes input reverse leakage current.
6. Not more than one output should be shorted at a time. The other outputs should not be loaded. For testing I_{OS}, the use of a high–speed test apparatus and/or sample–and–hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Translating Transceiver 100255

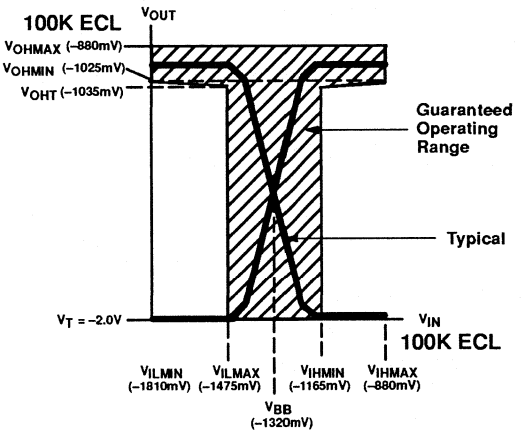
TRANSFER CHARACTERISTICS



ECL–to–TTL Translation[1]



TTL–to–ECL Translation[2]



Enabling and Disabling the ECL–Compatible Data Lines[3]

NOTES:
1. V_{IN} is applied to A_n and V_{OUT} is measured at B_n.
2. V_{IN} is applied to B_n and V_{OUT} is measured at A_n.
3. V_{IN} is applied to DIR or CE and V_{OUT} is measured at A_n.

AC ELECTRICAL CHARACTERISTICS FOR TTL–TO–ECL DATA FLOW

Ceramic DIP $GND_1 = GND_2$ = ground, V_{EE} = –5.7V to –4.2V, V_{TTL} = 4.5V to 5.5V.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	1.00 1.00	4.00 4.00	1.00 1.00	4.00 4.00	1.00 1.00	4.00 4.00	ns ns
t_{PZH}	Output enable time CE, DIR to A_n	Waveform 2	4.00	8.00	4.00	8.00	4.00	8.00	ns ns
t_{PHZ}	Output disable time CE, DIR to A_n	Waveform 2	1.50	4.00	1.50	4.00	1.50	4.00	ns ns
t_{TLH} t_{THL}	Transition time for A_n	Waveform 1	1.00 1.00	2.50 2.50	1.00 1.00	2.50 2.50	1.00 1.00	2.50 2.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

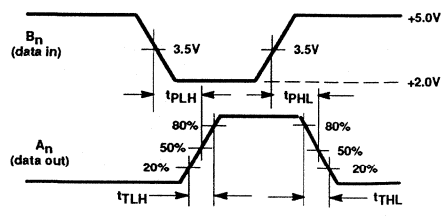
AC ELECTRICAL CHARACTERISTICS FOR ECL–TO–TTL DATA FLOW

Ceramic DIP $GND_1 = GND_2$ = ground, V_{EE} = –5.7V to –4.2V, V_{TTL} = 4.5V to 5.5V.

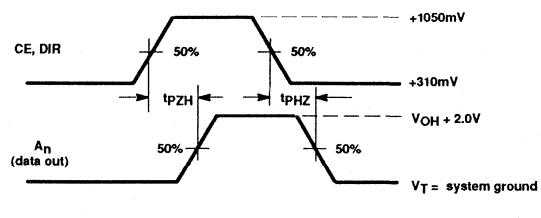
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 3		4.50 4.50		4.50 4.50		4.50 4.50	ns ns
t_{PZH} t_{PZL}	Output enable time CE, DIR to B_n	Waveform 4		7.00 7.00		7.00 7.00		7.00 7.00	ns ns
t_{PHZ} t_{PLZ}	Output disable time CE, DIR to B_n	Waveform 4		3.00 3.00		3.00 3.00		3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time for B_n	Waveform 3	1.00 1.00	3.50 3.50	1.00 1.00	3.50 3.50	1.00 1.00	3.50 3.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS FOR TTL–TO–ECL DATA FLOW



Waveform 1. Propagation Delays and Transition Times

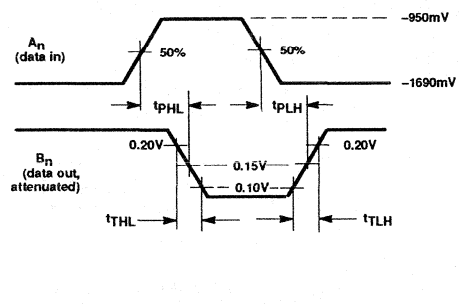


Waveform 2. Output Enable and Disable Times

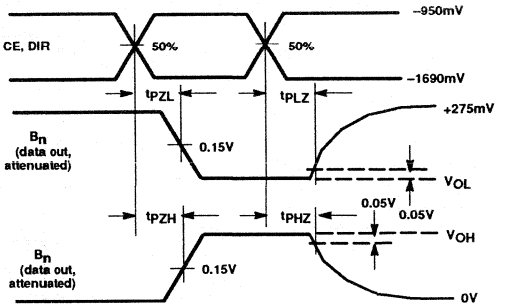
NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Translating Transceiver 100255

AC WAVEFORMS FOR ECL–TO–TTL DATA FLOW

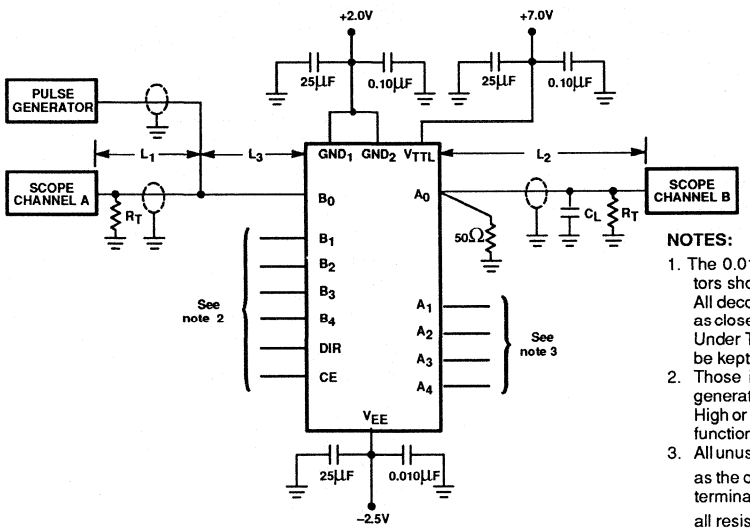


Waveform 3. Propagation Delays and Transition Times



Waveform 4. Output Enable and Disable Times

AC TEST CIRCUIT FOR TTL–TO–ECL DATA FLOW

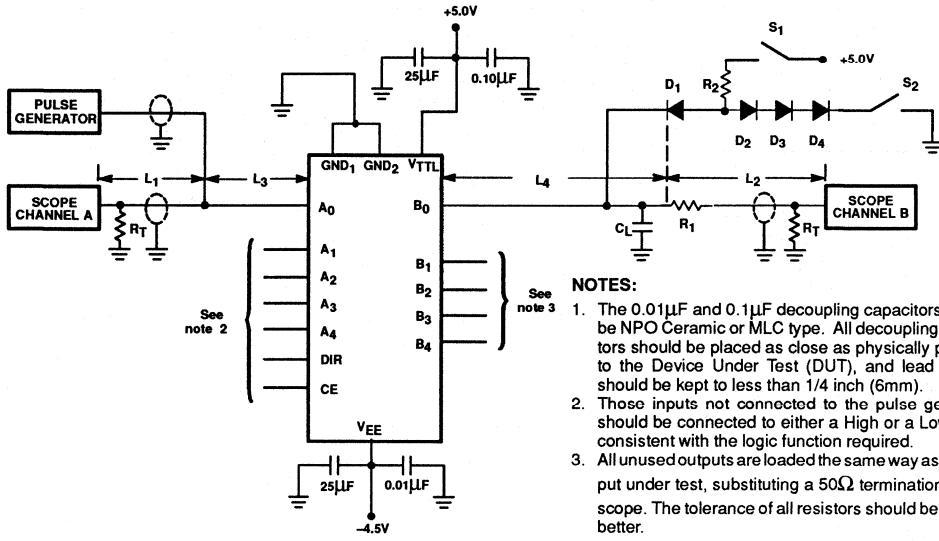


NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

Translating Transceiver 100255

AC TEST CIRCUIT FOR ECL–TO–TTL DATA FLOW



SWITCH POSITION

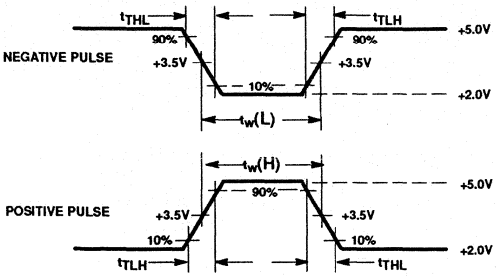
TEST	SWITCH S_1	SWITCH S_2
t_{PLH}, t_{PHL}	closed	closed
t_{PLZ}, t_{PZL}	closed	open
t_{PHZ}, t_{PZH}	open	open

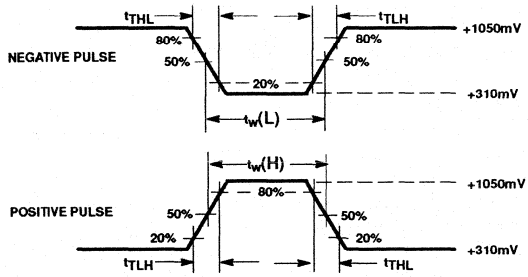
NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm). L_4, the lead length from the DUT output pin to R_1 and D_1, should not exceed 1/4 inch.
5. R_T = 50Ω termination internal to scope. R_1 =450Ω. R_2 =280Ω.
6. Fixture and stray capacitance (not including scope cable capacitance) = C_L = 25pF.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. When the output under test is in the high impedance state, the voltage at scope channel B will be at ground potential with S_1 and S_2 open and at 0.275V with S_1 closed and S_2 open.
9. D_1 through D_4 are high frequency (low capacitance) switching diodes.

Translating Transceiver 100255

INPUT PULSE DEFINITION FOR TTL–TO–ECL DATA FLOW



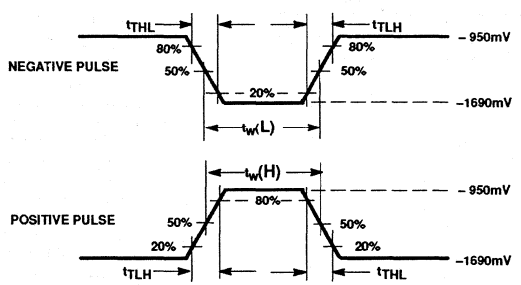


INPUT PULSE REQUIREMENTS for B_n $GND_1 = GND_2 = +2.0V \pm 0.010V$, $V_{EE} = -2.8V$ to $-2.2V$, $V_{TTL} = +6.5V$ to $+7.5V$, $V_T = 0V$ (system ground)				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
TTL	$3.0V_{p-p}$	1MHz	500ns	2.5 ± 0.2ns

INPUT PULSE REQUIREMENTS for CE and DIR $GND_1 = GND_2 = +2.0V \pm 0.010V$, $V_{EE} = -2.8V$ to $-2.2V$, $V_{TTL} = +6.5V$ to $+7.5V$, $V_T = 0V$ (system ground)				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
100K ECL	$740mV_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION FOR ECL–TO–TTL DATA FLOW



INPUT PULSE REQUIREMENTS for A_n, CE, and DIR $GND_1 = GND_2 = 0V$ (system ground), $V_{EE} = -4.8V$ to $-4.2V$, $V_{TTL} = +4.5V$ to $+5.5V$				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
100K ECL	$3.0V_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

Document No.	
ECN No.	
Date of Issue	May 25, 1990
Status	Preliminary Specification
ECL Products	

100790

9–Bit Transceiver

FEATURES

- **Typical propagation delay from input to output: 1.3ns**
- **Typical supply current ($-I_{EE}$): 240mA**
- **3–state outputs eliminate bus impedance discontinuities and wire–OR problems**
- **9–bit data width provides optimum handling of parity bit**
- **Drives 25Ω loads**
- **4,000 Volt ESD protection for all pins**
- **Controlled edge rates for quieter bus operation**

DESCRIPTION

The 100790 is a nine–bit, noninverting transceiver. All data lines (A_n and B_n) are bidirectional with three–state capability. The Direction Control, DIR, selects the data flow path (A_n to B_n or B_n to A_n). The Output Enable, $\overline{OE}$, determines whether the data lines are active or in a high impedance state. A High on $\overline{OE}$ will turn off the output emitter follower of every data line. As a result, each data line approaches the termination voltage (–2.0V) and takes on a high impedance state.

Each data line can drive a load as low as 25 Ohms (i.e. a 50 Ohm bus terminated at each end with 50 Ohms to –2.0V). Integrated pull–down resistors are provided for all data lines.

All unused inputs can be left open due to integrated pull–down resistors.

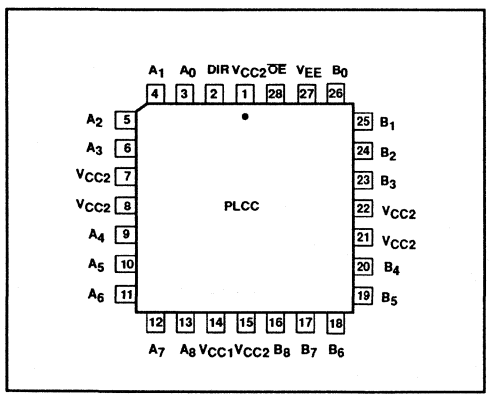
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28–Pin PLCC	100790A

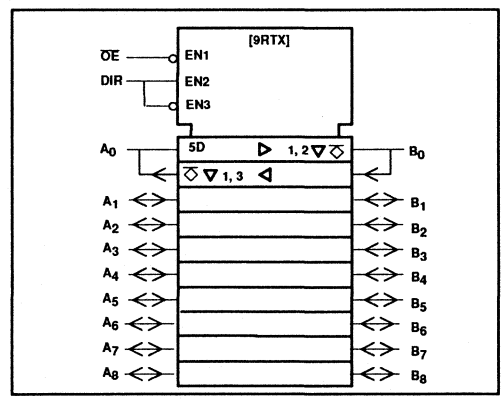
PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_8$	A bidirectional data lines
$B_0 - B_8$	B bidirectional data lines
$\overline{OE}$	Output enable input
DIR	Direction control input

PIN CONFIGURATION



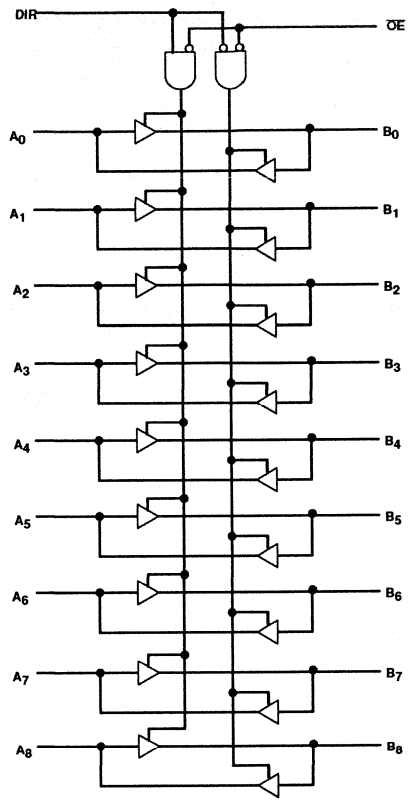
IEC/IEEE SYMBOL



Transceiver

100790

LOGIC DIAGRAM



FUNCTION TABLE

CONTROL		DATA		OPERATING MODE
$\overline{OE}$	DIR	A_n	B_n	
L	L	L	L	Data flows from B_n to A_n
L	L	H	H	
L	H	L	L	Data flows from A_n to B_n
L	H	H	H	
H	X	Z	Z	All A_n and B_n in high impedance state

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance state

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, $T_A = 0°C$ to $+70°$ C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–100	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+70	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

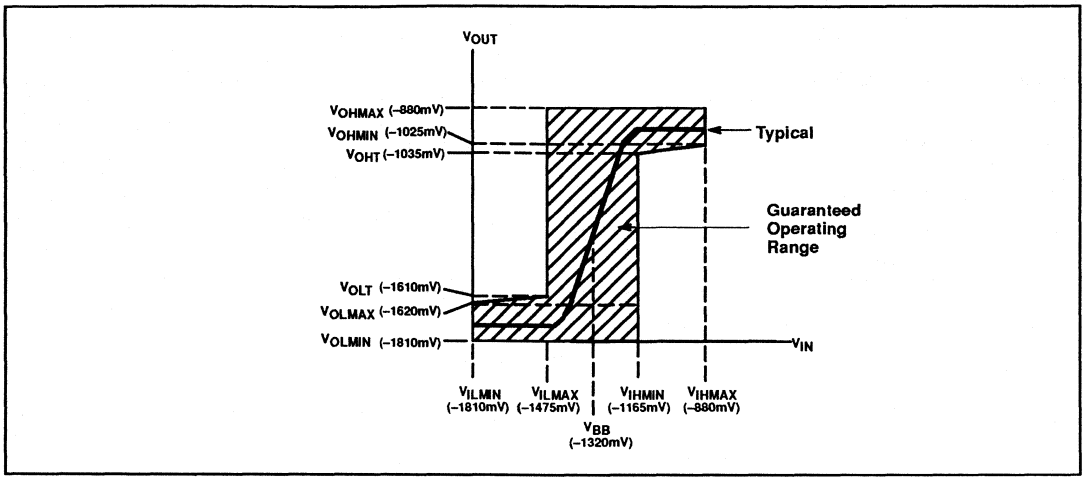
$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +70°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 25Ω to –2.0V ± 0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{OZ}	Off–state output current[5]		$\overline{OE}$ at V_{IHMAX}. Apply –2.1V to output under test. Apply V_{IHMAX} to the corresponding input.					120	µA
I_{IH}	High level input current[5]	A_n, B_n	One input under test at V_{IHMAX}, other inputs at V_{ILMIN}. $\overline{OE}$ at V_{IHMAX}.					100	µA
		$\overline{OE}$, DIR	One control line under test at V_{IHMAX}, other control line at V_{ILMIN}. All A_n and B_n open.					100	µA
I_{IL}	Low level input current[5]	A_n, B_n	One input under test at V_{ILMIN}, other inputs at V_{IHMAX}. $\overline{OE}$ at V_{IHMAX}.			10			µA
		$\overline{OE}$, DIR	One control line under test at V_{ILMIN}, other control line at V_{IHMAX}. All A_n and B_n open.			10			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}.			100	240	280	mA

NOTES:

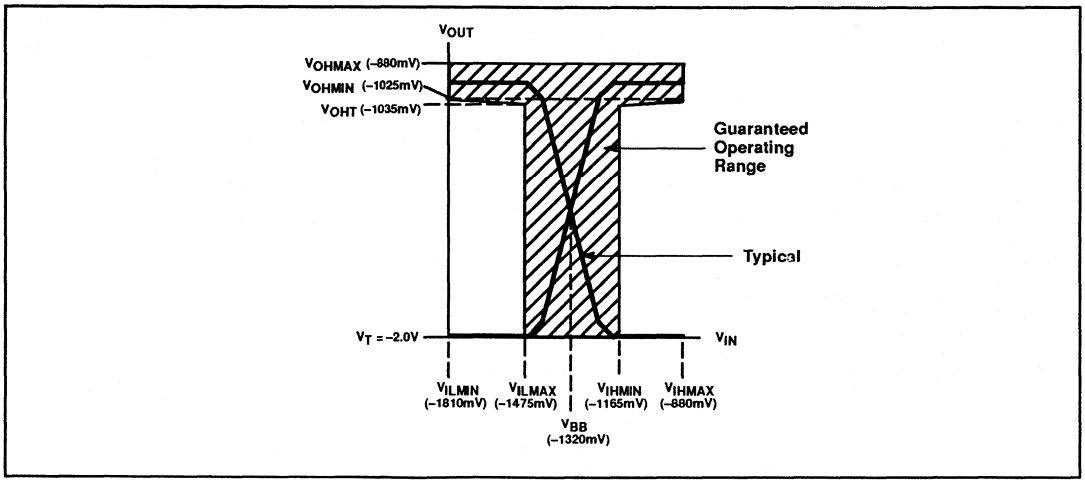
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapter 10, Section 4.
5. For bidirectional lines, this parameter includes currents due to output leakage and input pull–down resistors.

TRANSFER CHARACTERISTIC FOR DATA FLOW



NOTES:
1. If V_{IN} is applied to A_n, then V_{OUT} is measured at B_n.
2. If V_{IN} is applied to B_n, then V_{OUT} is measured at A_n.

TRANSFER CHARACTERISTIC FOR ENABLING AND DISABLING THE OUTPUTS



NOTE:
V_{IN} is applied to DIR or $\overline{OE}$; V_{OUT} is measured at A_n or B_n.

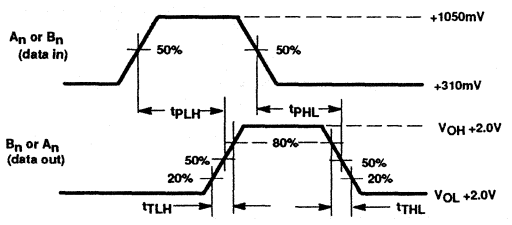
AC ELECTRICAL CHARACTERISTICS

PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.7V to –4.2V

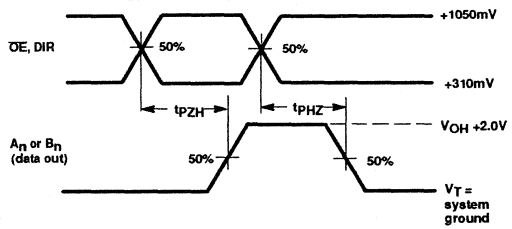
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +70°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 1	0.5	2.0	0.5	2.0	0.5	2.0	ns
t_{PZH}	Output enable time DIR, $\overline{OE}$ to A_n, B_n	Waveform 2	2.0	4.0	2.0	4.0	2.0	4.0	ns
t_{PHZ}	Output disable time DIR, $\overline{OE}$ to A_n, B_n	Waveform 2	0.7	2.2	0.7	2.2	0.7	2.2	ns
t_{TLH} t_{THL}	Transition time for A_n, B_n	Waveform 1	0.4	1.85	0.4	1.85	0.4	1.85	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delays and Transition Times

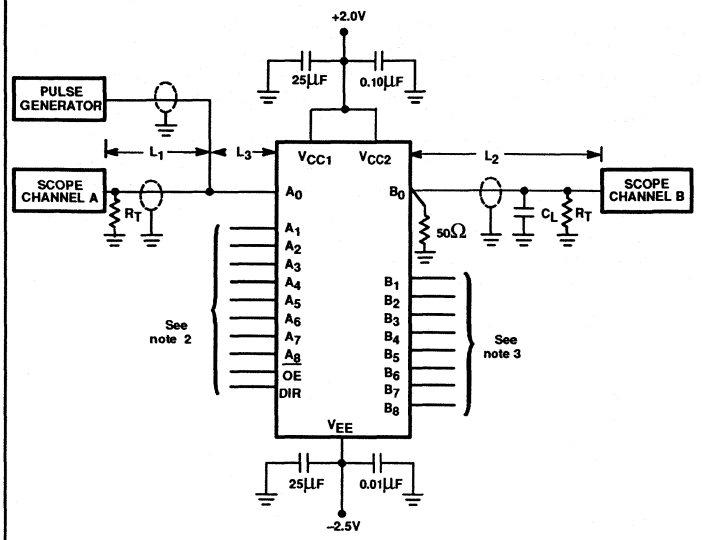


Waveform 2. Output Enable and Disable Time

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Transceiver 100790

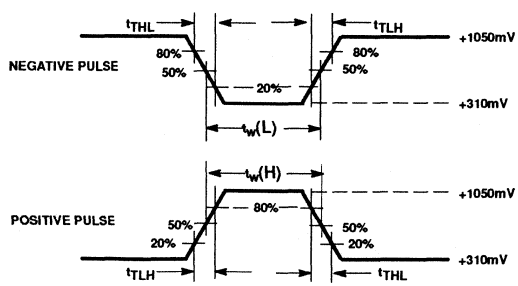
AC TEST CIRCUIT



NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.8V$ to $-2.2V$, $V_T = 0V$ (system ground)				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
100K ECL	740mV$_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Document No.	853–1438
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100982

Hex ECL–TTL Translating Transceiver with Registers

FEATURES

- **Typical propagation delay from clock to output: 3.5ns**
- **Typical ECL supply current (–IECL): 110mA**
- **Typical TTL supply current (ITTL): 25mA**
- **Low logic level of ECL output doubles as a high impedance state**
- **ECL output drives 25 Ohm loads**
- **4,000 Volt ESD protection for all pins**
- **Controlled edge rates for quieter bus operation**

DESCRIPTION

The 100982 is a six–bit, translating transceiver with registers. It allows the exchange of data between a 100K ECL bus and a TTL bus. The A data lines are 100K ECL–compatible and bidirectional. The B data lines are TTL–compatible and bidirectional. The control lines are 100K ECL–compatible.

There are three basic modes of operation for the device: When data flows from A to B, an ECL–to–TTL translation occurs. When data flows from B to A, a TTL–to–ECL translation occurs. Finally, A can be disconnected from B, preventing any data exchange between the ECL and TTL buses.

The 100982 has two storage registers, one for each direction of data flow (A to B, B to A). Data is stored on the rising edge of the clock pulse (CPAB, CPBA), provided that the clock enable ($\overline{CEAB}$, $\overline{CEBA}$) is Low.

Each 100K ECL output (A side) can drive a load as low as 25 Ohms (i.e. a 50 Ohm bus terminated at each end with 50 Ohms to –2.0V). When an ECL output goes Low, its emitter–follower turns off. As a result, the Low logic level approaches the termination voltage (–2.0V) and represents a high impedance state. A High on the ECL output enable ($\overline{OEBA}$) will also cut off the emitter–follower, producing the same high impedance state.

The TTL outputs (B side) have three–state capability. A High on the TTL output enable ($\overline{OEAB}$) will put the TTL outputs into a high impedance state.

Power may be applied to the VECL and VTTL pins in any order.

All unused inputs can be left open due to integrated pull–down resistors.

ORDERING INFORMATION

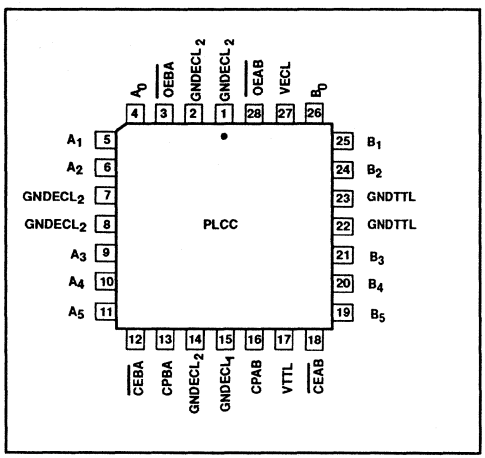
DESCRIPTION	ORDER CODE
28–Pin PLCC	100982A

Translating Transceiver 100982

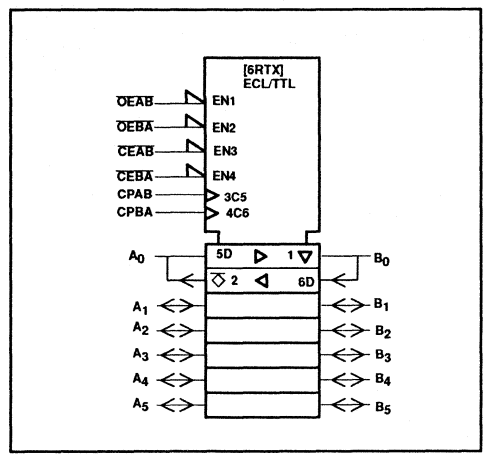
PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_5$	Bidirectional data lines (100K ECL compatible)
$B_0 - B_5$	Bidirectional data lines (TTL compatible)
$\overline{OEAB}$	B output enable (100K ECL compatible)
$\overline{OEBA}$	A output enable (100K ECL compatible)
CPAB	Clock pulse input for A–to–B data flow (100K ECL compatible)
CPBA	Clock pulse input for B–to–A data flow (100K ECL compatible)
$\overline{CEAB}$	Clock enable input for A–to–B data flow (100K ECL compatible)
$\overline{CEBA}$	Clock enable input for B–to–A data flow (100K ECL compatible)
VECL	ECL supply voltage
VTTL	TTL supply voltage
$GNDECL_1$	Ground for ECL internal logic and reference generator
$GNDECL_2$	Ground for ECL outputs
GNDTTL	TTL ground

PIN CONFIGURATION

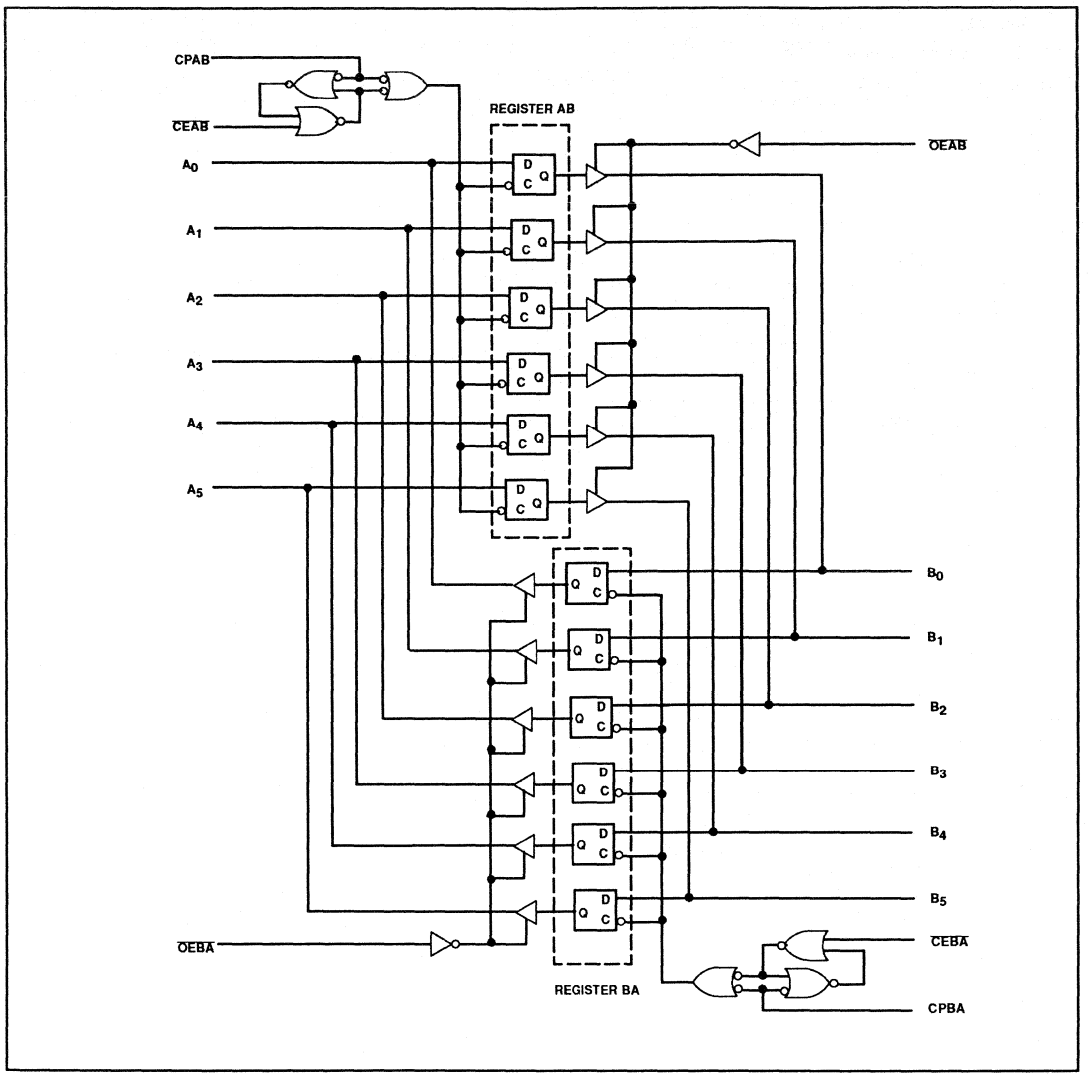


IEC/IEEE SYMBOL



Translating Transceiver 100982

LOGIC DIAGRAM



NOTE:
Pins B_0 through B_5 are TTL–compatible. Pins CPAB, CPBA, $\overline{CEAB}$, $\overline{CEBA}$, $\overline{OEAB}$, $\overline{OEBA}$, and A_0 through A_5 are ECL–compatible.

Translating Transceiver | 100982

FUNCTION TABLE

ENABLES		CLOCK	INPUT	REGISTER	OUTPUT	OPERATING MODE
$\overline{OEAB}$	$\overline{CEAB}$	CPAB	A_n	AB	B_n	A–TO–B DATA PATH (ECL–TO–TTL TRANSLATION)
$\overline{OEBA}$	$\overline{CEBA}$	CPBA	B_n	BA	A_n	B–TO–A DATA PATH (TTL–TO–ECL TRANSLATION)
L	L	↑	L	L	L	Load data into register and present at outputs
L	L	↑	H	H	H	
L	L	↥	X	L	L	Hold data in register and present at outputs
L	L	↥	X	H	H	
L	H	X	X	L	L	
L	H	X	X	H	H	
H	L	↑	L	L	Z	Load data into register with outputs in high impedance state
H	L	↑	H	H	Z	
H	L	↥	X	NC	Z	Hold data in register with outputs in high impedance state
H	H	X	X	NC	Z	

NOTES:

H = High voltage level
L = Low voltage level
X = Don't care
NC = No change
Z = High impedance state
↑ = Low–to–High transition
↥ = No Low–to–High transition

Any combination of A–to–B and B–to–A operations may be carried out concurrently, provided that no signal is driven into an active (enabled) output.

ABSOLUTE MAXIMUM RATINGS FOR ECL– COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground

T_A=0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
VECL	ECL supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than VECL)	VECL to +0.5	V
I_O	Output source current (continuous)	–100	mA

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

ABSOLUTE MAXIMUM RATINGS FOR TTL–COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground,

T_A =0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
VTTL	TTL supply voltage range	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to VTTL	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High state	–0.5 to VTTL	V
I_{OUT}	Current applied to output in Low state	+96	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS FOR ECL–COMPATIBLE LINES

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	NOM.	MAX.	
$GNDECL_1$	Ground for ECL internal logic and reference generator		0	0	0	V
$GNDECL_2$	Ground for ECL outputs		0	0	0	V
VECL	ECL supply voltage		–4.8	–4.5	–4.2	V
VECL	ECL supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	VECL = –4.2V	–1150		–880	mV
		VECL = –4.5V	–1165			
		VECL = –4.8V	–1165			
V_{IL}	Low level input voltage	VECL = –4.2V	–1810		–1475	mV
		VECL = –4.5V			–1475	mV
		VECL = –4.8V			–1490	mV

NOTE:
When operating at other than the specified VECL voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC OPERATING CONDITIONS FOR TTL–COMPATIBLE LINES

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	NOM.	MAX.	
GNDTTL	TTL ground	0	0	0	V
VTTL	TTL supply voltage	+4.5	+5.0	+5.5	V
V_{IH}	High level input voltage	+2.0			V
V_{IL}	Low level input voltage			+0.8	V
$-I_{OH}$	High level output current			15	mA
I_{OL}	Low level output current			48	mA
T_A	Operating ambient temperature range	0	+25	+85	°C

DC ELECTRICAL CHARACTERISTICS FOR ECL–COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –4.8V to –4.2V, VTTL = +4.5V to +5.5V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Store High state in register BA. A_n is tested with a 25Ω load terminated to V_T = –2.0V ± 0.010V. $\overline{OEBA}$ at V_{ILMIN}.	VECL = –4.2V	–1020		–870	mV
				VECL = –4.5V	–1025	–955	–880	mV
				VECL = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Store High state in register BA. A_n is tested with a 25Ω load terminated to V_T = –2.0V ± 0.010V. $\overline{OEBA}$ at V_{ILMAX}.	VECL = –4.2V	–1030			mV
				VECL = –4.5V	–1035			mV
				VECL = –4.8V	–1045			mV
I_{OZ}	Off–state output current[5]		Store High state in register BA. $\overline{OEBA}$ and $\overline{OEAB}$ at V_{IHMAX}. Apply –2.1V to A_n under test.				90	µA
I_{IH}	High level input current[5]	A_n	A_n under test at V_{IHMAX}, other A_n at V_{ILMIN}. $\overline{OEBA}$ at V_{IHMAX}.				120	µA
		$\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$, CPAB, CPBA	One control line under test at V_{IHMAX}, all other control lines at V_{ILMIN}. All A_n and B_n open.				140	µA
I_{IL}	Low level input current[5]	A_n	One A_n under test at V_{ILMIN}, other A_n at V_{IHMAX}. $\overline{OEBA}$ at V_{IHMAX}.		10			µA
		$\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$, CPAB, CPBA	One control line under test at V_{ILMIN}, all other control lines at V_{IHMAX}. All A_n and B_n open.		10			µA
–IECL	ECL supply current		All A_n at V_{IHMAX}. $\overline{OEBA}$ at V_{IHMAX}.		64	110	150	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to VECL = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended VECL range. For more information, see Chapter 10, Section 4.
5. For bidirectional lines, this parameter includes currents due to output leakage and input pull–down resistors.

DC ELECTRICAL CHARACTERISTICS FOR TTL–COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –4.8V to –4.2V, VTTL = 4.5V to 5.5V, $T_A = 0°C$ to +85°C unlles otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Store High state in register AB.	I_{OH} = –3mA	2.4			V
		$\overline{OEAB}$ at V_{ILMIN}.	I_{OH} = –15mA	2.0			V
V_{OL}	Low level output voltage	Store Low state in register AB.	I_{OL} = +24mA		0.35	0.50	V
		$\overline{OEAB}$ at V_{ILMIN}.	I_{OL} = +48mA		0.40	0.55	V
V_{IK}	Input clamp voltage	Apply –18mA to B_n under test with other B_n open. $\overline{OEAB}$ at V_{IHMAX}.		–1.2	–0.73		V
I_I	Input current at maximum input voltage[4]	B_n under test at +5.5V, other B_n at ground. $\overline{OEAB}$ at V_{IHMAX}. VTTL = +5.5V.				500	µA
I_{OZH}	Off–state output current, High level voltage applied[5]	Store Low state in register AB. $\overline{OEAB}$ and $\overline{OEBA}$ at V_{IHMAX}. Apply 2.7V to B_n under test.				80	µA
I_{OZL}	Off–state output current, Low level voltage applied[6]	Store High state in register AB. $\overline{OEAB}$ and $\overline{OEBA}$ at V_{IHMAX}. Apply 0.5V to B_n under test.				40	µA
$-I_{OS}$	Short circuit output current[7]	Store High state in register AB. One B_n under test at ground. $\overline{OEAB}$ at V_{ILMIN}.		60	95	225	mA
ITTLH	TTL supply current with outputs High	Store High state in register AB. $\overline{OEAB}$ at V_{ILMIN}.			20	30	mA
ITTLL	TTL supply current with outputs Low	Store Low state in register AB. $\overline{OEAB}$ at V_{ILMIN}.			25	35	mA
ITTLZ	TTL supply current with outputs in the high impedance state	$\overline{OEAB}$ at V_{IHMAX}.			30	40	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. This parameter includes output leakage current.
5. This parameter includes input reverse leakage current.
6. This parameter includes forward input current.
7. Not more than one output should be shorted at a time. The other outputs should not be loaded. For testing I_{OS}, the use of a high–speed test apparatus and/or sample–and–hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR TTL–TO–ECL DATA FLOW

PLCC $GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –5.7V to –4.2V, VTTL = 4.5V to 5.5V.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency CPBA	Waveform 1	400		400		400		MHz
t_{PZH} t_{PHZ}	Propagation delay CPBA to A_n	Waveform 1	2.0 0.5	4.5 3.0	2.0 0.5	4.5 3.0	2.0 0.5	4.5 3.0	ns ns
t_{PZH}	Output enable time $\overline{OEBA}$ to A_n	Waveform 3	2.0	4.5	2.0	4.5	2.0	4.5	ns
t_{PHZ}	Output disable time $\overline{OEBA}$ to A_n	Waveform 3	0.5	2.5	0.5	2.5	0.5	2.5	ns
t_{TZH} t_{THZ}	Transition time for A_n	Waveform 1	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time B_n to CPBA	Waveform 1	3.5 4.0		3.5 4.0		3.5 4.0		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time CPBA to B_n	Waveform 1	0 0		0 0		0 0		ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time $\overline{CEBA}$ to CPBA	Waveform 2	1.0 1.5		1.0 1.5		1.0 1.5		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time CPBA to $\overline{CEBA}$	Waveform 2	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{w(H)}$ $t_{w(L)}$	Pulse width CPBA	Waveform 1	1.0 1.0		1.0 1.0		1.0 1.0		ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

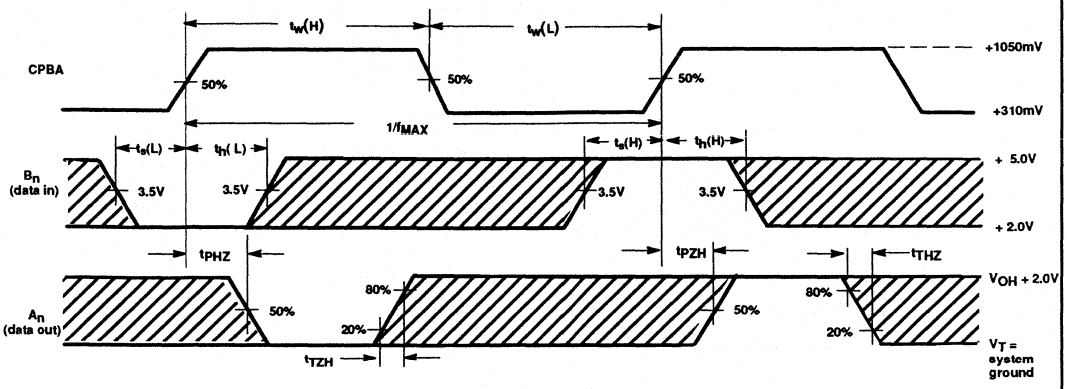
AC ELECTRICAL CHARACTERISTICS FOR ECL–TO–TTL DATA FLOW

PLCC $GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –5.7V to –4.2V, VTTL = 4.5V to 5.5V.

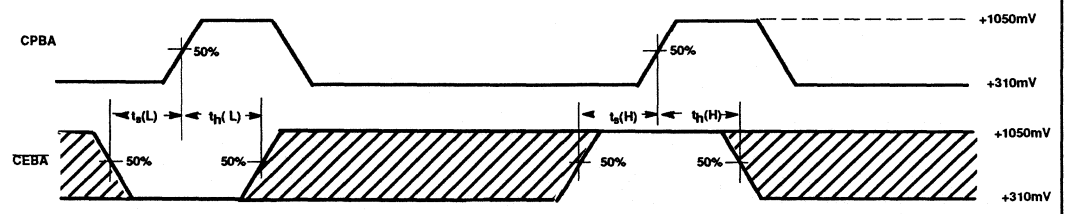
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency CPAB	Waveform 4	300		300		300		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to B_n	Waveform 4	1.5 2.0	4.0 4.5	1.5 2.0	4.0 4.5	1.5 2.0	4.0 4.5	ns ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEAB}$ to B_n	Waveform 6	1.5 2.0	4.0 5.0	1.5 2.0	4.0 5.0	1.5 2.0	4.0 5.0	ns ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEAB}$ to B_n	Waveform 6	2.0 4.0	5.0 7.0	2.0 4.0	5.0 7.0	2.0 4.0	5.0 7.0	ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time A_n to CPAB	Waveform 4	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time CPAB to A_n	Waveform 4	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time $\overline{CEAB}$ to CPAB	Waveform 5	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time CPAB to $\overline{CEAB}$	Waveform 5	1.0 1.5		1.0 1.5		1.0 1.5		ns ns
$t_{w(H)}$ $t_{w(L)}$	Pulse width CPAB	Waveform 4	1.0 1.0		1.0 1.0		1.0 1.0		ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

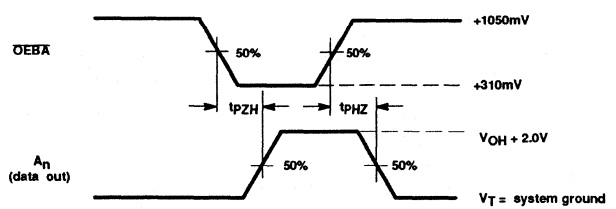
AC WAVEFORMS FOR TTL–TO–ECL DATA FLOW



Waveform 1. Data Timing



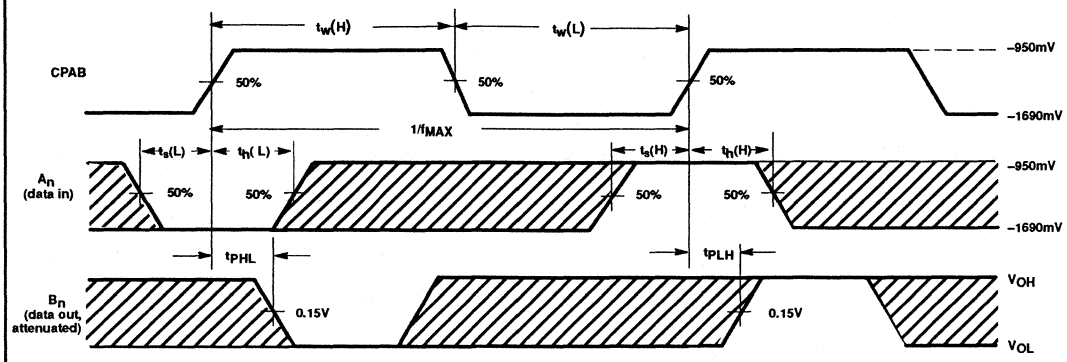
Waveform 2. Clock Enable Timing



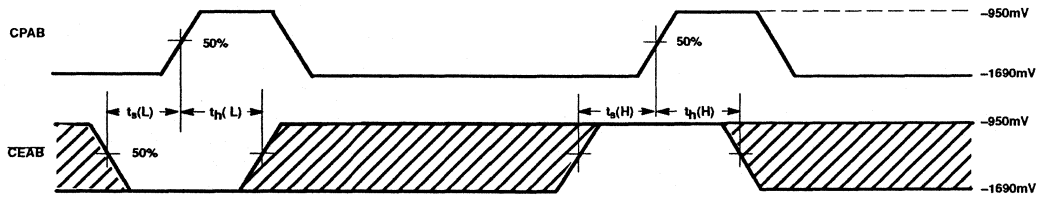
Waveform 3. Output Enable Timing

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

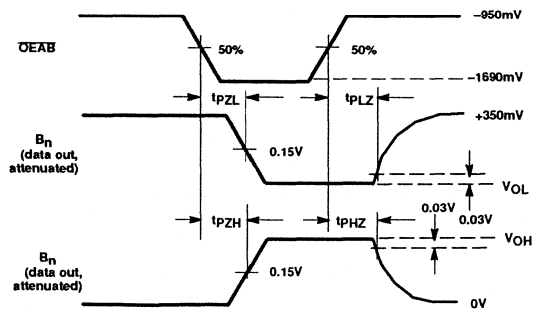
AC WAVEFORMS FOR ECL–TO–TTL DATA FLOW



Waveform 4. Data Timing



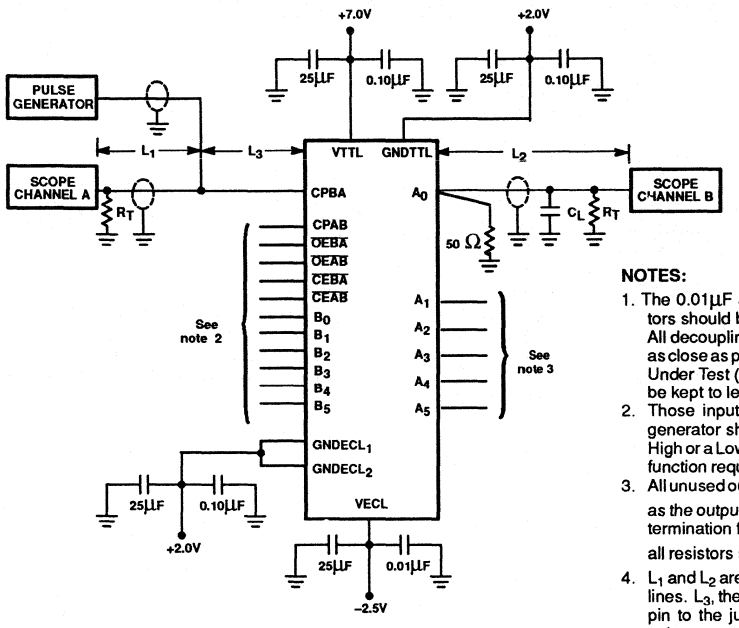
Waveform 5. Clock Enable Timing



Waveform 6. Output Enable Timing

Translating Transceiver 100982

AC TEST CIRCUIT FOR TTL–TO–ECL DATA FLOW

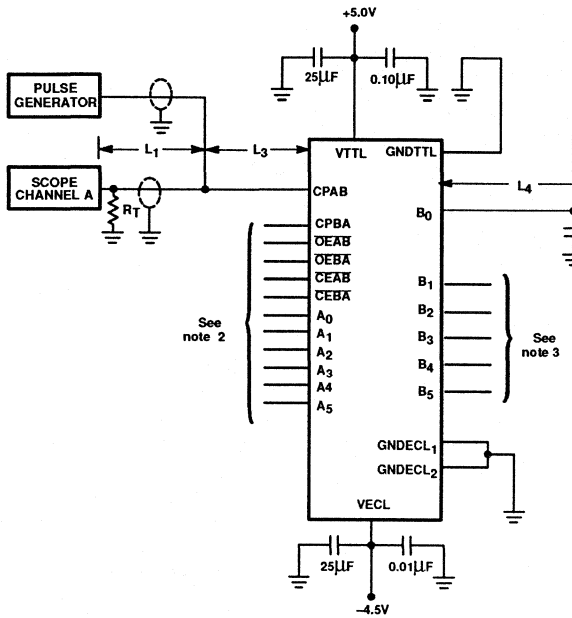


NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

Translating Transceiver | 100982

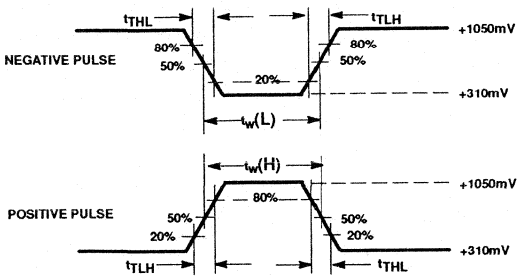
AC TEST CIRCUIT FOR ECL–TO–TTL DATA FLOW



NOTES:

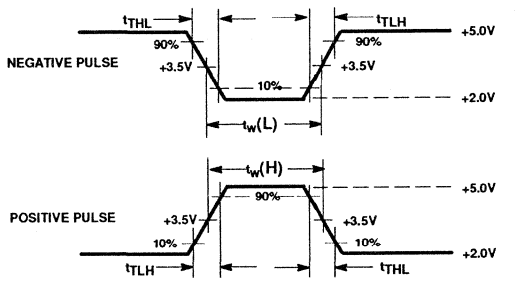
1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead length should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm). L_4, the lead length from the DUT output pin to R_1 and R_L, should not exceed 1/4 inch.
5. R_T = 50Ω termination internal to scope. R_1 = 450Ω. R_L = 500Ω.
6. Fixture and stray capacitance (not including scope cable capacitance) = C_L = 50pF.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. Measure t_{PLZ} and t_{PZL} with the switch closed. Other AC parameters are tested with the switch open.

INPUT PULSE DEFINITION FOR TTL–TO–ECL DATA FLOW



INPUT PULSE REQUIREMENTS FOR CPAB, CPBA, $\overline{CEAB}$, $\overline{CEBA}$, $\overline{OEAB}$, $\overline{OEBA}$
$GNDECL_1 = GNDECL_2 = GNDTTL = +2.0V \pm 0.010V$, VECL = –2.8V to –2.2V, VTTL = +6.5V to +7.5V, V_T = 0V (system ground)

Family	Amplitude	Rep Rate	$t_w(L)$, $t_w(H)$	t_{TLH}, t_{THL}
100K ECL	$740mV_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

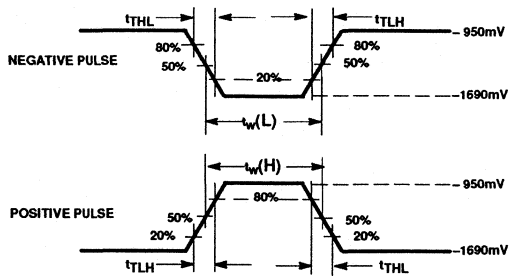


INPUT PULSE REQUIREMENTS FOR B_n
$GNDECL_1 = GNDECL_2 = GNDTTL = +2.0V \pm 0.010V$, VECL = –2.8V to –2.2V, VTTL = +6.5V to +7.5V, V_T = 0V (system ground)

Family	Amplitude	Rep Rate	$t_w(L)$, $t_w(H)$	t_{TLH}, t_{THL}
TTL	$3.0V_{p-p}$	1MHz	500ns	2.5 ± 0.2ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION FOR ECL–TO–TTL DATA FLOW



INPUT PULSE REQUIREMENTS FOR
A_n, CPAB, CPBA, $\overline{CEAB}$, $\overline{CEBA}$, $\overline{OEAB}$, $\overline{OEBA}$
$GNDECL_1$ = $GNDECL_2$ = GNDTTL = 0V (system ground),
VECL = –4.8V to –4.2V, VTTL = +4.5V to +5.5V

Family	Amplitude	Rep Rate	$t_w(L)$, $t_w(H)$	t_{TLH}, t_{THL}
100K ECL	740mV_{p-p}	1MHz	500ns	0.7 ± 0.1ns

Document No.	853–1439
ECN No.	99800
Date of Issue	June 14, 1990
Status	Product Specification
ECL Products	

100984

Quad ECL–TTL Translating Transceiver with Registers

FEATURES

- **Typical propagation delay from clock to output: 3.5ns**
- **Typical ECL supply current (–IECL): 110mA**
- **Typical TTL supply current (ITTL): 25mA**
- **Low logic level of ECL output doubles as a high impedance state**
- **ECL output drives 25 Ohm loads**
- **4,000 Volt ESD protection for all pins**
- **Controlled edge rates for quieter bus operation**

DESCRIPTION

The 100984 is a four–bit, translating transceiver with registers. It allows the exchange of data between a 100K ECL bus and a TTL bus. The A data lines are 100K ECL–compatible and bidirectional. The B data lines are TTL–compatible and unidirectional (BI for input, BO for output). The control lines are 100K ECL–compatible.

There are three basic modes of operation for the device: When data flows from A to BO, an ECL–to–TTL translation occurs. When data flows from BI to A, a TTL–to–ECL translation occurs. Finally, A can be disconnected from B, preventing any data exchange between the ECL and TTL buses.

The 100984 has two storage registers, one for each direction of data flow (A to BO, BI to A). Data is stored on the rising edge of the clock pulse (CPAB, CPBA), provided that the clock enable ($\overline{CEAB}$, $\overline{CEBA}$) is Low.

Each 100K ECL output (A side) can drive a load as low as 25 Ohms (i.e. a 50 Ohm bus terminated at each end with 50 Ohms to –2.0V). When an ECL output goes Low, its emitter–follower turns off. As a result, the Low logic level approaches the termination voltage (–2.0V) and represents a high impedance state. A High on the ECL output enable ($\overline{OEBA}$) will also cut off the emitter–follower, producing the same high impedance state.

The TTL outputs (BO) have three–state capability. A High on the TTL output enable ($\overline{OEAB}$) will put the TTL outputs into a high impedance state.

Power may be applied to the VECL and VTTL pins in any order.

All unused inputs can be left open due to integrated pull–down resistors.

ORDERING INFORMATION

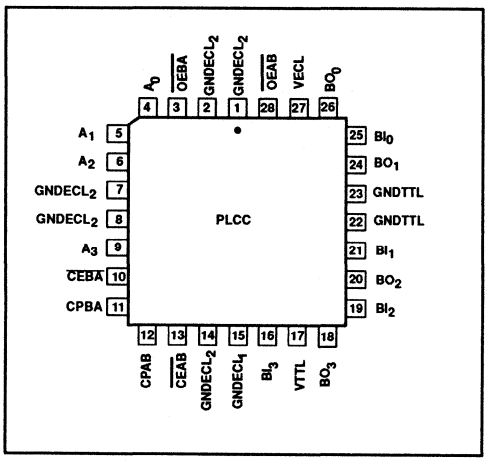
DESCRIPTION	ORDER CODE
28–Pin PLCC	100984A

Translating Transceiver 100984

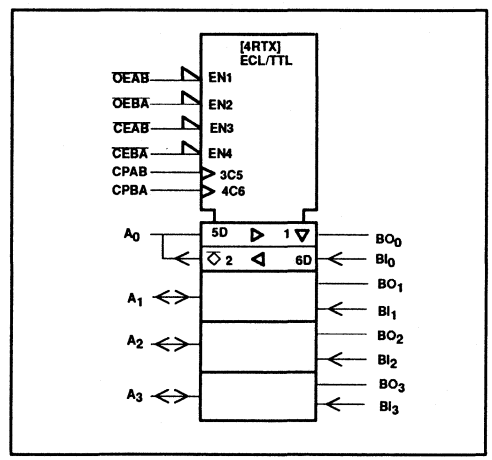
PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_3$	Bidirectional data lines (100K ECL compatible)
$BI_0 - BI_3$	Data inputs (TTL compatible)
$BO_0 - BO_3$	Data outputs (TTL compatible)
$\overline{OEAB}$	BO output enable (100K ECL compatible)
$\overline{OEBA}$	A output enable (100K ECL compatible)
CPAB	Clock pulse input for A–to–BO data flow (100K ECL compatible)
CPBA	Clock pulse input for BI–to–A data flow (100K ECL compatible)
$\overline{CEAB}$	Clock enable input for A–to–BO data flow (100K ECL compatible)
$\overline{CEBA}$	Clock enable input for BI–to–A data flow (100K ECL compatible)
VECL	ECL supply voltage
VTTL	TTL supply voltage
$GNDECL_1$	Ground for ECL internal logic and reference generator
$GNDECL_2$	Ground for ECL outputs
GNDTTL	TTL ground

PIN CONFIGURATION

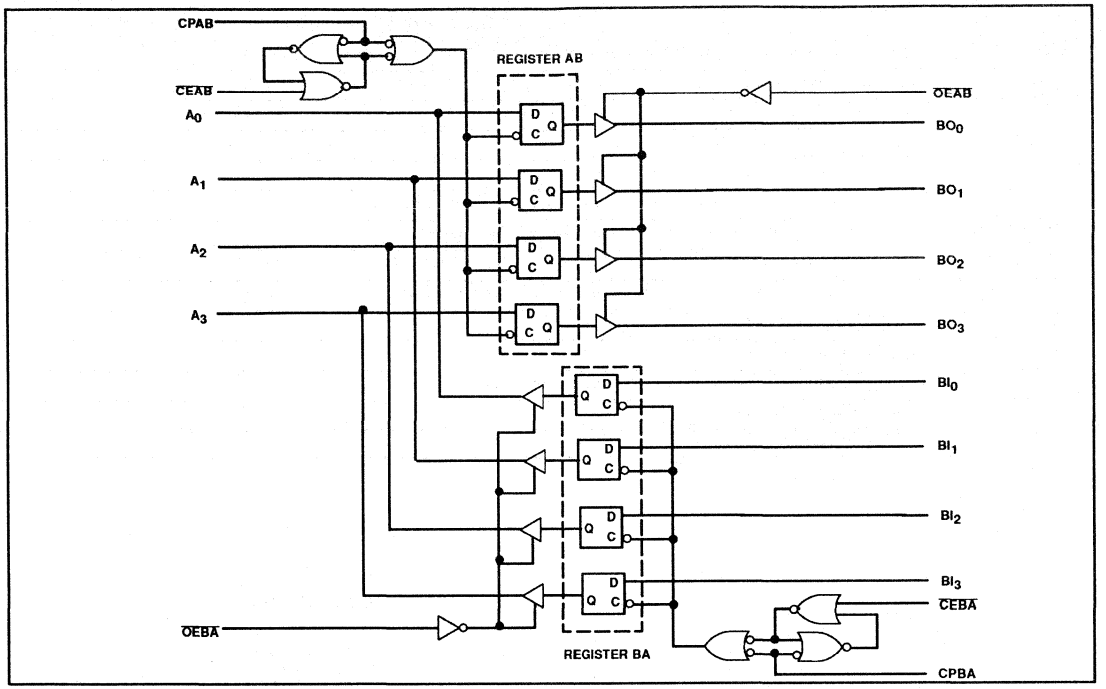


IEC/IEEE SYMBOL



Translating Transceiver | 100984

LOGIC DIAGRAM



NOTE:
Pins BI_0 through BI_3 and BO_0 through BO_3 are TTL–compatible. Pins CPAB, CPBA, $\overline{CEAB}$, $\overline{CEBA}$, $\overline{OEAB}$, $\overline{OEBA}$, and A_0 through A_3 are ECL–compatible.

FUNCTION TABLE

ENABLES		CLOCK	INPUT	REGISTER	OUTPUT	OPERATING MODE
$\overline{OEAB}$	$\overline{CEAB}$	CPAB	A_n	AB	BO_n	A–TO–BO DATA PATH (ECL–TO–TTL TRANSLATION)
$\overline{OEBA}$	$\overline{CEBA}$	CPBA	BI_n	BA	A_n	BI–TO–A DATA PATH (TTL–TO–ECL TRANSLATION)
L	L	↑	L	L	L	Load data into register and present at outputs
L	L	↑	H	H	H	
L	L	↕	X	L	L	Hold data in register and present at outputs
L	L	↕	X	H	H	
L	H	X	X	L	L	
L	H	X	X	H	H	
H	L	↑	L	L	Z	Load data in register with outputs in high impedance state
H	L	↑	H	H	Z	
H	L	↕	X	NC	Z	Hold data in register with outputs in high impedance state
H	H	X	X	NC	Z	

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
NC = No change
Z = High impedance state
↑ = Low–to–High transition
↕ = No Low–to–High transition

Any combination of A–to–B and B–to–A operations may be carried out concurrently, provided that no signal is driven into an active (enabled) output.

ABSOLUTE MAXIMUM RATINGS FOR ECL–COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground

$T_A = 0°C$ to $+85°C$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
VECL	ECL supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than VECL)	VECL to +0.5	V
I_O	Output source current (continuous)	–100	mA

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

ABSOLUTE MAXIMUM RATINGS FOR TTL–COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground,

$T_A = 0°C$ to $+85°C$ unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
VTTL	TTL supply voltage range	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to VTTL	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High state	–0.5 to VTTL	V
I_{OUT}	Current applied to output in Low state	+96	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS FOR ECL–COMPATIBLE LINES

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
$GNDECL_1$	Ground for ECL internal logic and reference generator		0	0	0	V
$GNDECL_2$	Ground for ECL outputs		0	0	0	V
VECL	ECL supply voltage		–4.8	–4.5	–4.2	V
VECL	ECL supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	VECL = –4.2V	–1150		–880	mV
		VECL = –4.5V	–1165			
		VECL = –4.8V	–1165			
V_{IL}	Low level input voltage	VECL = –4.2V	–1810		–1475	mV
		VECL = –4.5V			–1475	mV
		VECL = –4.8V			–1490	mV

NOTE:
When operating at other than the specified VECL voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

Translating Transceiver 100984

DC OPERATING CONDITIONS FOR TTL–COMPATIBLE LINES

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	NOM.	MAX.	
GNDTTL	TTL ground	0	0	0	V
VTTL	TTL supply voltage	+4.5	+5.0	+5.5	V
V_{IH}	High level input voltage	+2.0			V
V_{IL}	Low level input voltage			+0.8	V
$-I_{OH}$	High level output current			15	mA
I_{OL}	Low level output current			48	mA
T_A	Operating ambient temperature range	0	+25	+85	°C

DC ELECTRICAL CHARACTERISTICS FOR ECL–COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –4.8V to –4.2V, VTTL = +4.5V to +5.5V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Store High state in register BA. A_n is tested with a 25Ω load terminated to V_T = –2.0V ± 0.010V. $\overline{OEBA}$ at V_{ILMIN}.	VECL = –4.2V	–1020		–870	mV
				VECL = –4.5V	–1025	–955	–880	mV
				VECL = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Store High state in register BA. A_n is tested with a 25Ω load terminated to V_T = –2.0V ± 0.010V. $\overline{OEBA}$ at V_{ILMAX}.	VECL = –4.2V	–1030			mV
				VECL = –4.5V	–1035			mV
				VECL = –4.8V	–1045			mV
I_{OZ}	Off–state output current[5]		Store High state in register BA. $\overline{OEBA}$ and $\overline{OEAB}$ at V_{IHMAX}. Apply –2.1V to A_n under test.				90	µA
I_{IH}	High level input current[5]	A_n	A_n under test at V_{IHMAX}, other A_n at V_{ILMIN}. $\overline{OEBA}$ at V_{IHMAX}.				120	µA
		$\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$, CPAB, CPBA	One control line under test at V_{IHMAX}, all other control lines at V_{ILMIN}. All BI_n at V_{ILMIN}. All A_n and BO_n open.				140	µA
I_{IL}	Low level input current[5]	A_n	A_n under test at V_{ILMIN}, other A_n at V_{IHMAX}. $\overline{OEBA}$ at V_{IHMAX}.		10			µA
		$\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$, CPAB, CPBA	One control line under test at V_{ILMIN}, all other control lines at V_{IHMAX}. All BI_n at V_{IHMAX}. All A_n and BO_n open.		10			µA
–IECL	ECL supply current		All A_n at V_{IHMAX}. $\overline{OEBA}$ at V_{IHMAX}.		64	110	150	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to VECL = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended VECL range. For more information, see Chapter 10, Section 4.
5. For bidirectional lines, this parameter includes currents due to output leakage and input pull–down resistors.

DC ELECTRICAL CHARACTERISTICS FOR TTL–COMPATIBLE LINES

$GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –4.8V to –4.2V, VTTL = 4.5V to 5.5V, T_A = 0°C to +85°C unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Store High state in register AB.	I_{OH} = –3mA	2.4			V
		$\overline{OEAB}$ at V_{ILMIN}.	I_{OH} = –15mA	2.0			V
V_{OL}	Low level output voltage	Store Low state in register AB.	I_{OL} = +24mA		0.35	0.50	V
		$\overline{OEAB}$ at V_{ILMIN}.	I_{OL} = +48mA		0.40	0.55	V
V_{IK}	Input clamp voltage	Apply –18mA to BI_n under test with other BI_n open.		–1.2	–0.73		V
I_I	Input current at maximum input voltage	BI_n under test at +5.5V, other BI_n at ground. VTTL at +5.5V.				500	µA
I_{IH}	High level input current	BI_n under test at +2.4V, other BI_n at ground.				70	µA
$-I_{IL}$	Low level input current	BI_n under test at +0.4V, other BI_n at +2.4V.				70	µA
I_{OZH}	Off–state output current, High level voltage applied	Store Low state in register AB. $\overline{OEAB}$ and $\overline{OEBA}$ at V_{IHMAX}. Apply 2.4V to BO_n under test.				80	µA
I_{OZL}	Off–state output current, Low level voltage applied	Store High state in register AB. $\overline{OEAB}$ and $\overline{OEBA}$ at V_{IHMAX}. Apply 0.5V to BO_n under test.				40	µA
$-I_{OS}$	Short circuit output current[4]	Store High state in register AB. One BO_n under test at ground. $\overline{OEAB}$ at V_{ILMIN}.		60	95	225	mA
ITTLH	TTL supply current with outputs High	Store High state in register AB. $\overline{OEAB}$ at V_{ILMIN}. All BO_n open. VTTL at +5.5V.			20	30	mA
ITTLL	TTL supply current with outputs Low	Store Low state in register AB. $\overline{OEAB}$ at V_{ILMIN}. All BO_n open. VTTL at +5.5V.			25	35	mA
ITTLZ	TTL supply current with outputs in the high impedance state	$\overline{OEAB}$ at V_{IHMAX}. All BO_n open. VTTL at +5.5V.			30	40	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. Not more than one output should be shorted at a time. The other outputs should not be loaded. For testing I_{OS}, the use of a high–speed test apparatus and/or sample–and–hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR TTL–TO–ECL DATA FLOW

PLCC $GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –5.7V to –4.2V, VTTL = 4.5V to 5.5V.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency CPBA	Waveform 1	350		350		350		MHz
t_{PZH} t_{PHZ}	Propagation delay CPBA to A_n	Waveform 1	2.0 0.5	4.5 3.0	2.0 0.5	4.5 3.0	2.0 0.5	4.5 3.0	ns ns
t_{PZH}	Output enable time $\overline{OEBA}$ to A_n	Waveform 3	2.0	4.5	2.0	4.5	2.0	4.5	ns
t_{PHZ}	Output disable time $\overline{OEBA}$ to A_n	Waveform 3	0.5	2.5	0.5	2.5	0.5	2.5	ns
t_{TZH} t_{THZ}	Transition time for A_n	Waveform 1	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time BI_n to CPBA	Waveform 1	3.5 4.0		3.5 4.0		3.5 4.0		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time BI_n to CPBA	Waveform 1	0 0		0 0		0 0		ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time $\overline{CEBA}$ to CPBA	Waveform 2	1.0 1.5		1.0 1.5		1.0 1.5		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time $\overline{CEBA}$ to CPBA	Waveform 2	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{w(H)}$ $t_{w(L)}$	Pulse width CPBA	Waveform 1	1.0 1.0		1.0 1.0		1.0 1.0		ns ns

NOTE: For AC test setup information, see AC Testing, Chapter 2, Section 3.

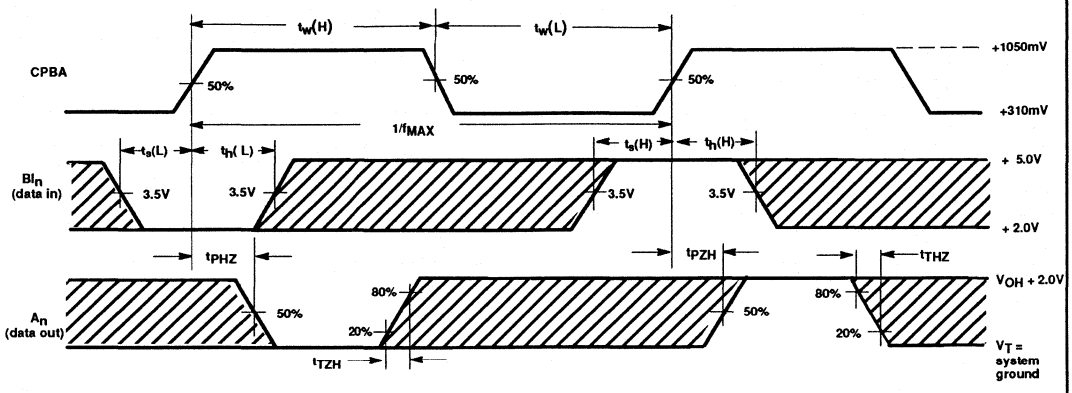
AC ELECTRICAL CHARACTERISTICS FOR ECL–TO–TTL DATA FLOW

PLCC $GNDECL_1 = GNDECL_2 = GNDTTL$ = ground, VECL = –5.7V to –4.2V, VTTL = 4.5V to 5.5V.

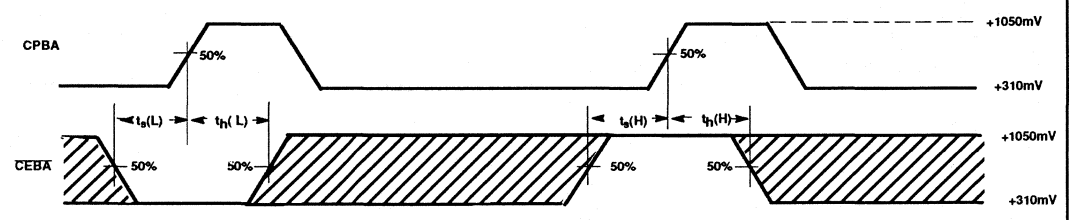
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{MAX}	Maximum clock frequency CPAB	Waveform 4	300		300		300		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to BO_n	Waveform 4	1.5 2.0	4.0 4.5	1.5 2.0	4.0 4.5	1.5 2.0	4.0 4.5	ns ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEAB}$ to BO_n	Waveform 6	1.5 2.0	4.0 5.0	1.5 2.0	4.0 5.0	1.5 2.0	4.0 5.0	ns ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEAB}$ to BO_n	Waveform 6	2.0 4.0	5.0 7.0	2.0 4.0	5.0 7.0	2.0 4.0	5.0 7.0	ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time A_n to CPAB	Waveform 4	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time A_n to CPAB	Waveform 4	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{s(H)}$ $t_{s(L)}$	Setup time $\overline{CEAB}$ to CPAB	Waveform 5	1.0 1.0		1.0 1.0		1.0 1.0		ns ns
$t_{h(H)}$ $t_{h(L)}$	Hold time $\overline{CEAB}$ to CPAB	Waveform 5	1.0 1.5		1.0 1.5		1.0 1.5		ns ns
$t_{w(H)}$ $t_{w(L)}$	Pulse width CPAB	Waveform 4	1.0 1.0		1.0 1.0		1.0 1.0		ns ns

NOTE: For AC test setup information, see AC Testing, Chapter 2, Section 3.

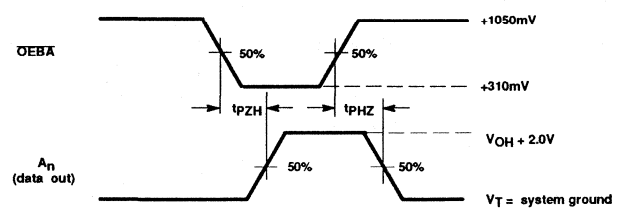
AC WAVEFORMS FOR TTL–TO–ECL DATA FLOW



Waveform 1. Data Timing



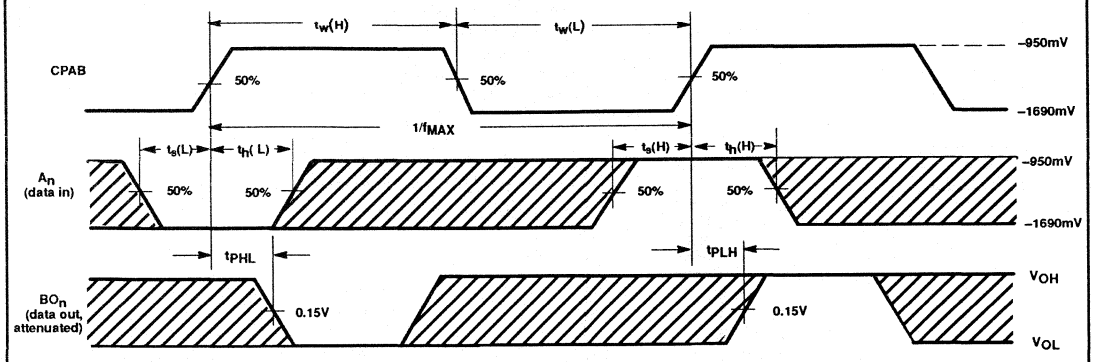
Waveform 2. Clock Enable Timing



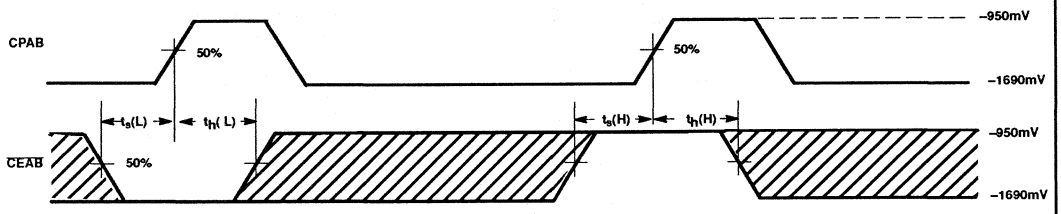
Waveform 3. Output Enable Timing

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

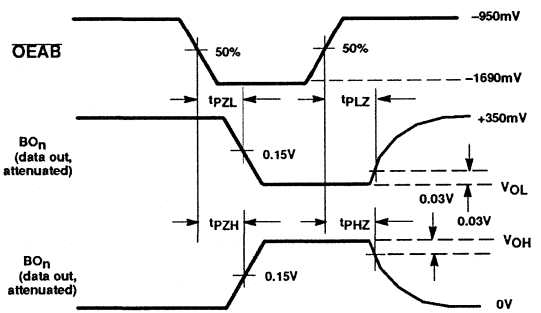
AC WAVEFORMS FOR ECL–TO–TTL DATA FLOW



Waveform 4. Data Timing

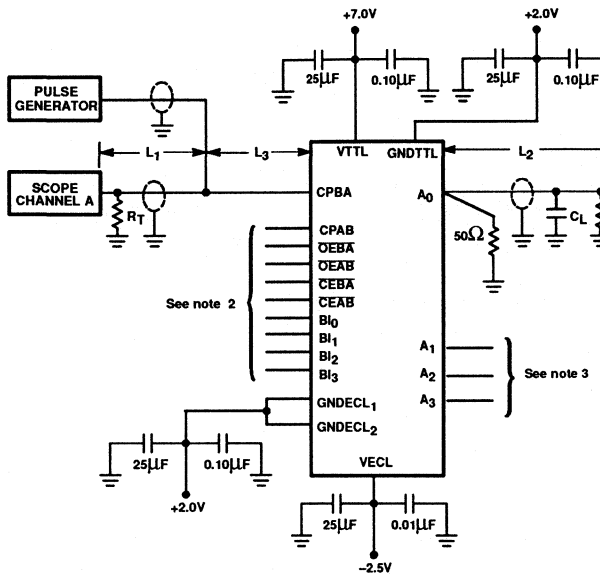


Waveform 5. Clock Enable Timing



Waveform 6. Output Enable and Disable Timing

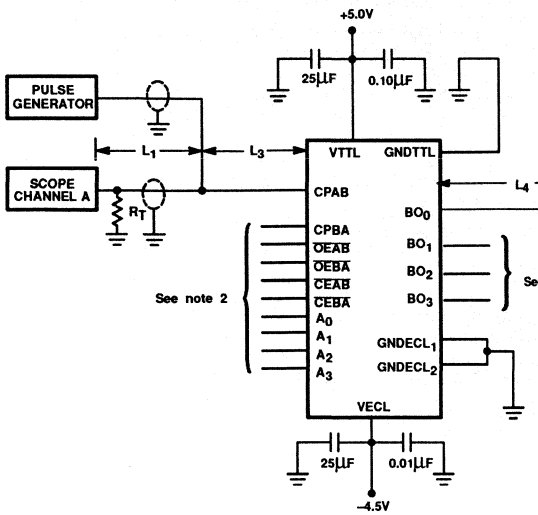
AC TEST CIRCUIT FOR TTL–TO ECL DATA FLOW



NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

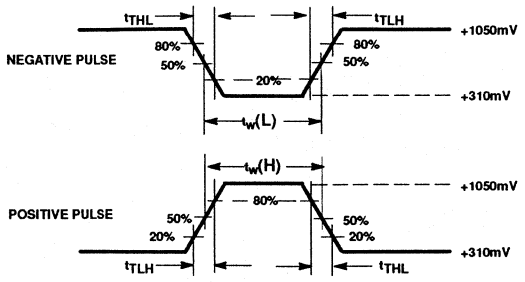
AC TEST CIRCUIT FOR ECL–TO TTL DATA FLOW



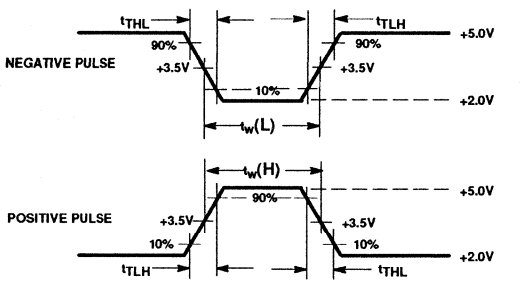
NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm). L_4, the lead length from the DUT output pin to R_1 and R_L, should not exceed 1/4 inch.
5. R_T = 50Ω termination internal to scope. R_1 = 450Ω. R_L = 500Ω.
6. Fixture and stray capacitance (not including scope cable capacitance) = C_L = 50pF.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. Measure t_{PLZ} and t_{PZL} with the switch closed. Other AC parameters are tested with the switch open.

INPUT PULSE DEFINITION FOR TTL–TO–ECL DATA FLOW



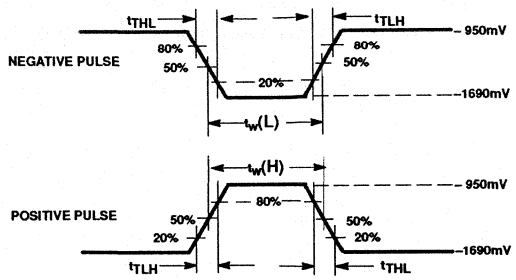
INPUT PULSE REQUIREMENTS FOR CPAB, CPBA, $\overline{CEAB}$, $\overline{CEBA}$, $\overline{OEAB}$, $\overline{OEBA}$ $GNDECL_1 = GNDECL_2 = GNDTTL = +2.0V \pm 0.010V$, $VECL = -2.8V$ to $-2.2V$, $VTTL = +6.5V$ to $+7.5V$, $V_T = 0V$ (system ground)				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
100K ECL	$740mV_{p-p}$	1MHz	500ns	0.7 ± 0.1ns



INPUT PULSE REQUIREMENTS FOR BI_n $GNDECL_1 = GNDECL_2 = GNDTTL = +2.0V \pm 0.010V$, $VECL = -2.8V$ to $-2.2V$, $VTTL = +6.5V$ to $+7.5V$, $V_T = 0V$ (system ground)				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
TTL	$3.0V_{p-p}$	1MHz	500ns	2.5 ± 0.2ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION FOR ECL–TO–TTL DATA FLOW



INPUT PULSE REQUIREMENTS FOR
A_n, CPAB, CPBA, $\overline{CEAB}$, $\overline{CEBA}$, $\overline{OEAB}$, $\overline{OEBA}$
$GNDECL_1 = GNDECL_2 = GNDTTL = 0V$ (system ground),
VECL = –4.8V to –4.2V, VTTL = +4.5V to +5.5V

Family	Amplitude	Rep Rate	$t_w(L)$, $t_w(H)$	t_{TLH}, t_{THL}
100K ECL	$740mV_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

Document No.	
ECN No.	
Date of Issue	March 14, 1990
Status	Preliminary Specification
ECL Products	

100990

9–Bit Transceiver

FEATURES

- **Typical propagation delay from input to output: 1.3ns**
- **Typical supply current ($-I_{EE}$): 240mA**
- **3–state outputs eliminate bus impedance discontinuities and wire–OR problems**
- **9–bit data width provides optimum handling of parity bit**
- **Drives 25Ω loads**
- **4,000 Volt ESD protection for all pins**
- **Controlled edge rates for quieter bus operation**

DESCRIPTION

The 100990 is a nine–bit, noninverting transceiver. All data lines (A_n and B_n) are bidirectional with three–state capability. Two control lines preside over the data flow direction: a Priority Enable, E_p, and a Subordinate Enable, $\overline{E}_s$. A High logic level on E_p selects an A–to–B data flow path regardless of the level applied to $\overline{E}_s$. Bringing both E_p and $\overline{E}_s$ Low selects a B–to–A data flow path. If E_p is Low and $\overline{E}_s$ is High, all data lines will be in a high impedance state.

Each data line can drive a load as low as 25 Ohms (i.e. a 50 Ohm bus terminated at each end with 50 Ohms to –2.0V). Integrated pull–down resistors are provided for all data lines.

All unused inputs can be left open due to integrated pull–down resistors.

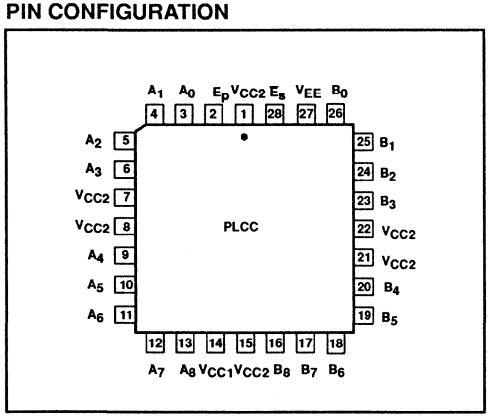
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28–Pin PLCC	100990A

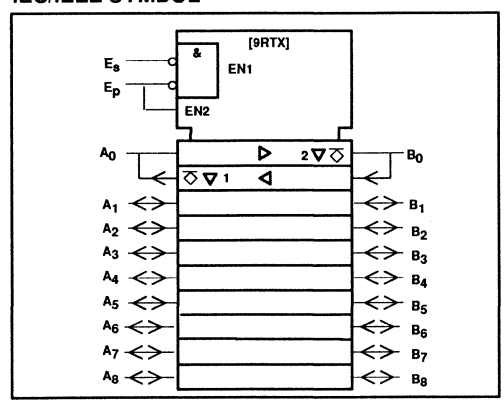
PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_8$	A bidirectional data lines
$B_0 - B_8$	B bidirectional data lines
$\overline{E}_s$	Subordinate enable input
E_p	Priority enable input

PIN CONFIGURATION

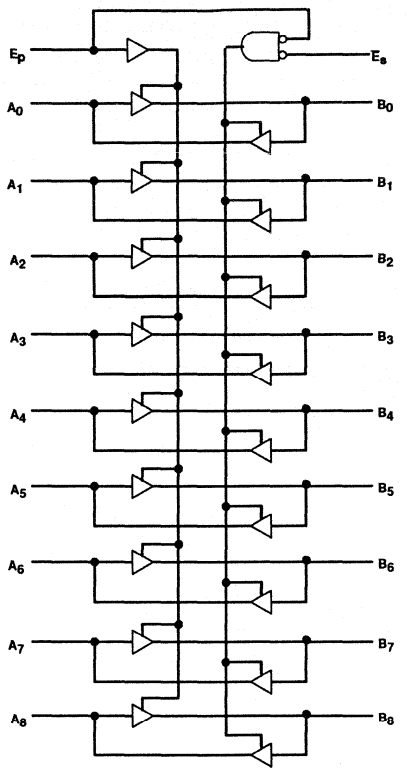


IEC/IEEE SYMBOL



Transceiver 100990

LOGIC DIAGRAM



FUNCTION TABLE

CONTROL		DATA		OPERATING MODE
E_p	E_s	A_n	B_n	
L	L	L	L	Data flows from B_n to A_n
L	L	H	H	
L	H	Z	Z	All A_n and B_n in high impedance state
H	X	L	L	Data flows from A_n to B_n
H	X	H	H	

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance state

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +70° C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–100	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+70	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

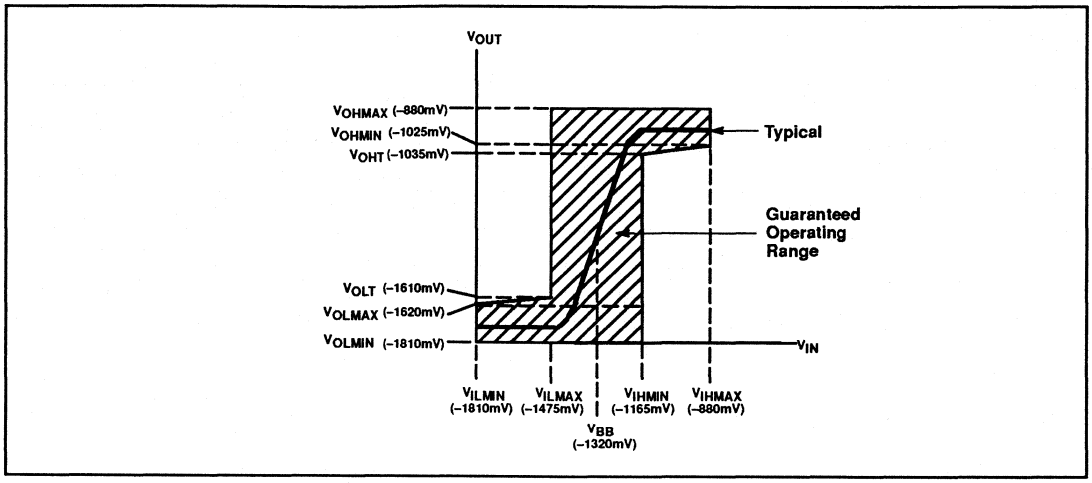
$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +70°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs Loaded with 25Ω to –2.0V ± 0.010V	Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time, other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{OZ}	Off-state output current[5]		E_p at V_{ILMIN}. $\overline{E}_s$ at V_{IHMAX}. Apply –2.1V to output under test. Apply V_{IHMAX} to the corresponding input.					120	µA
I_{IH}	High level input current[5]	A_n, B_n	One input under test at V_{IHMAX}, other inputs at V_{ILMIN}. E_p at V_{ILMIN}. $\overline{E}_s$ at V_{IHMAX}.					100	µA
		E_p, $\overline{E}_s$	One control line under test at V_{IHMAX}, other control line at V_{ILMIN}. All A_n and B_n open.					100	µA
I_{IL}	Low level input current[5]	A_n, B_n	One input under test at V_{ILMIN}, other inputs at V_{IHMAX}. E_p at V_{ILMIN}. $\overline{E}_s$ at V_{IHMAX}.			10			µA
		E_p, $\overline{E}_s$	One control line under test at V_{ILMIN}, other control line at V_{IHMAX}. All A_n and B_n open.			10			µA
$-I_{EE}$	V_{EE} supply current		E_p at V_{ILMIN}, all other inputs at V_{IHMAX}.			100	240	280	mA

NOTES:

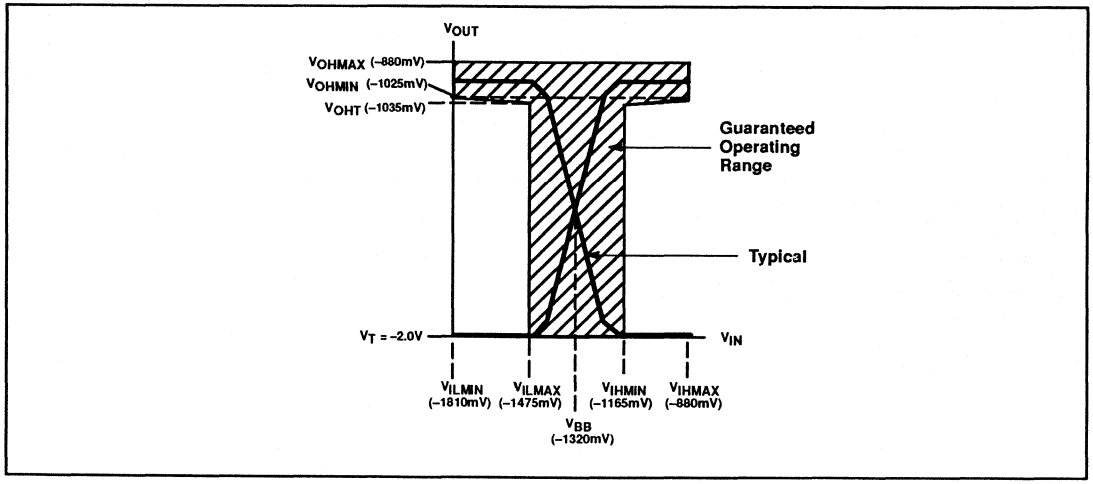
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapter 10, Section 4.
5. For bidirectional lines, this parameter includes currents due to output leakage and input pull–down resistors.

TRANSFER CHARACTERISTIC FOR DATA FLOW



NOTES:
1. If V_{IN} is applied to A_n, then V_{OUT} is measured at B_n.
2. If V_{IN} is applied to B_n, then V_{OUT} is measured at A_n.

TRANSFER CHARACTERISTIC FOR ENABLING AND DISABLING THE OUTPUTS



NOTE:
V_{IN} is applied to E_p or $\overline{E}_s$; V_{OUT} is measured at A_n or B_n.

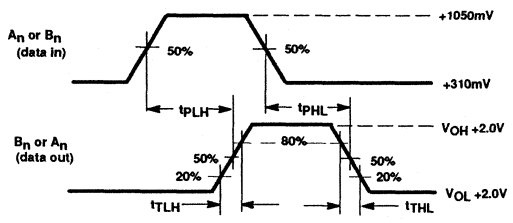
AC ELECTRICAL CHARACTERISTICS

PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.7V$ to $-4.2V$

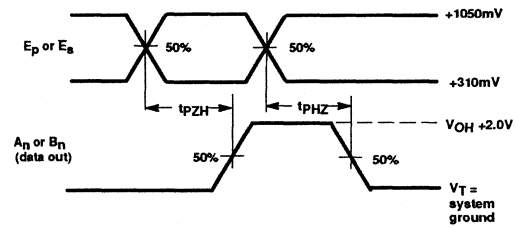
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +70°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 1	0.5	2.0	0.5	2.0	0.5	2.0	ns
t_{PZH}	Output enable time E_p to A_n, B_n or $\overline{E}_s$ to A_n	Waveform 2	2.0	4.0	2.0	4.0	2.0	4.0	ns
t_{PHZ}	Output disable time E_p to A_n, B_n or $\overline{E}_s$ to A_n	Waveform 2	0.7	2.2	0.7	2.2	0.7	2.2	ns
t_{TLH} t_{THL}	Transition time for A_n, B_n	Waveform 1	0.4	1.85	0.4	1.85	0.4	1.85	ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



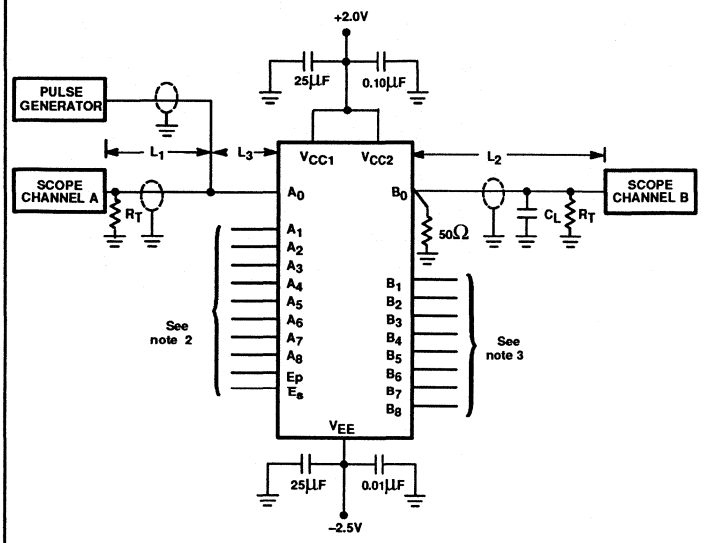
Waveform 1. Propagation Delays and Transition Times



Waveform 2. Output Enable and Disable Time

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

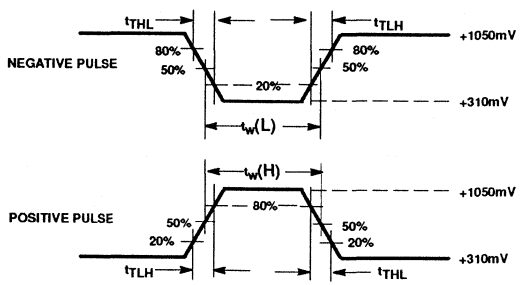
AC TEST CIRCUIT



NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS

$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$,
$V_{EE} = -2.8V$ to $-2.2V$, $V_T = 0V$ (system ground)

Family	Amplitude	Rep Rate	$t_w(L)$, $t_w(H)$	t_{TLH}, t_{THL}
100K ECL	$740mV_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

Section 8
ECL Memory Data Sheets

INDEX

10149	1K-Bit ECL Bipolar PROM (256 × 4)	615
10149A	1K-Bit ECL Bipolar PROM (256 × 4)	619
10149B	1K-Bit ECL Bipolar PROM (256 × 4)	623
100149	1K-Bit ECL Bipolar PROM (256 × 4)	627
100149A	1K-Bit ECL Bipolar PROM (256 × 4)	631
100149B	1K-Bit ECL Bipolar PROM (256 × 4)	635
10H20EV8	ECL Programmable Array Logic	639
10020EV8	ECL Programmable Array Logic	639

Philips Components

Document No.	853–0133
ECN No.	86487
Date of Issue	November 11, 1986
Status	Product Specification
ECL Products	

10149
1K-Bit ECL Bipolar PROM

DESCRIPTION

The 10149 is field programmable, meaning that custom patterns are immediately available by following the ECL fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 10149 is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

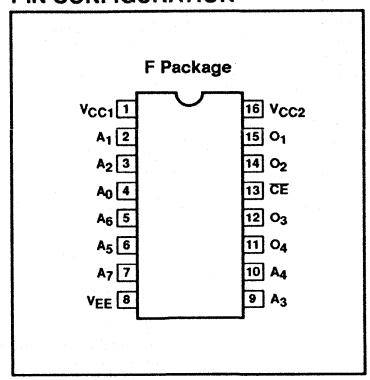
FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High-impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

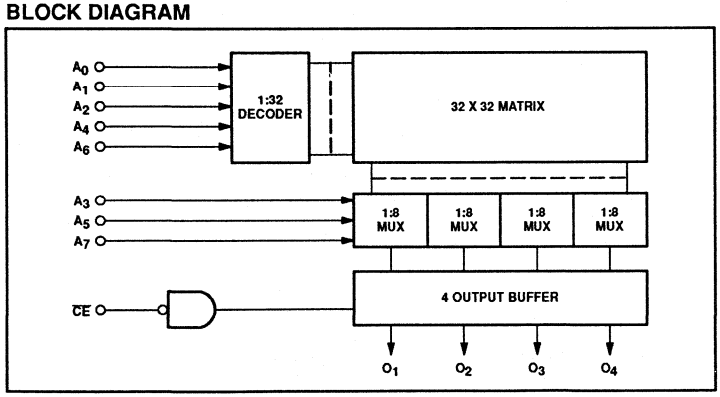
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



1K–Bit ECL Bipolar PROM (256 × 4) 10149

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–pin Ceramic DIP (300mil–wide)	10149 F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	–30 to +85	°C
T_{STG}	Storage temperature range	–55 to +165	°C

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

DC ELECTRICAL CHARACTERISTICS $-30°C \leq T_A < +85°C$, $-4.94V \leq V_{EE} \leq -5.46V$

			–30°C		+25°C			+85°C		
SYMBOL	PARAMETER[1]	TEST CONDITIONS	Min	Max	Min	Typ[3]	Max	Min	Max	UNIT
Input voltage[2,3]										
V_{IL}	Low		–1.890		–1.850			–1.825		V
V_{IH}	High			–0.890			–0.810		–0.700	V
V_{ILA}	Low threshold			–1.500			–1.475		–1.440	V
V_{IHA}	High threshold		–1.205		–1.105			–1.035		V
Output voltage										
V_{OL}	Low	V_{IH} = Max	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	V
V_{OH}	High	V_{IL} = Min	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	V
V_{OLA}	Low threshold	V_{IHA} = Min, V_{ILA} = Max		–1.655			–1.630		–1.595	V
V_{OHA}	High threshold	V_{IHA} = Min, V_{ILA} = Max	–1.080		–0.980			–0.910		V
Input current										
I_{IL}	Low	V_{IH} = Max			0.5					µA
I_{IH}	High	V_{IL} = Min		250			250		250	µA
Supply drain current										
I_{EE}		V_{EE} = –5.2V		160		150	160		160	mA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 10K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. Typical values are at V_{EE} = –5.2V, T_A = +25°C.

1K–Bit ECL Bipolar PROM (256 × 4) 10149

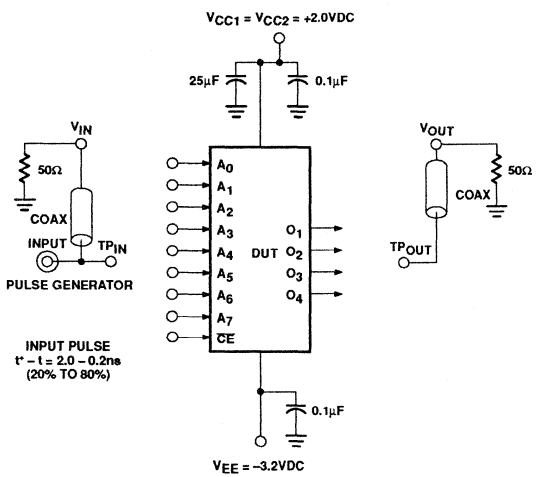
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $C_L = 30pF$, $-30°C \leq T_A \leq +85°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address		14	20	ns
t_{CE}		Output	Chip Enable		4	8	ns
Disable time							
t_{CD}		Output	Chip Disable		4	8	ns
Rise and fall time							
t_+	Rise time (20–80%)				4.0		ns
t_-	Fall time (80–20%)				4.0		ns

NOTE:

1. Typical values are at $V_{EE} = -5.2V$, $T_A = +25°C$.

TEST LOAD CIRCUITS

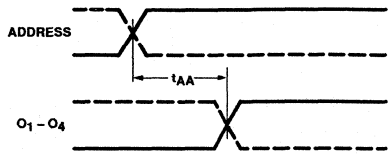


NOTES:

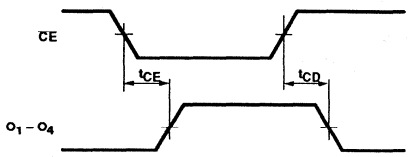
1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as posstble. A 10µF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

1K–Bit ECL Bipolar PROM (256 × 4) 10149

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

Philips Components

Document No.	853–1282
ECN No.	91142
Date of Issue	October 27, 1987
Status	Product Specification
ECL Products	

10149A
1K-Bit ECL Bipolar PROM

DESCRIPTION

The 10149A is field programmable, meaning that custom patterns are immediately available by following the Signetics Generic IV Programming procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 10149A is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

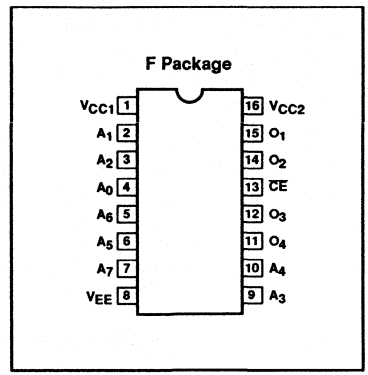
FEATURES

- **Address access time: 10ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High-impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

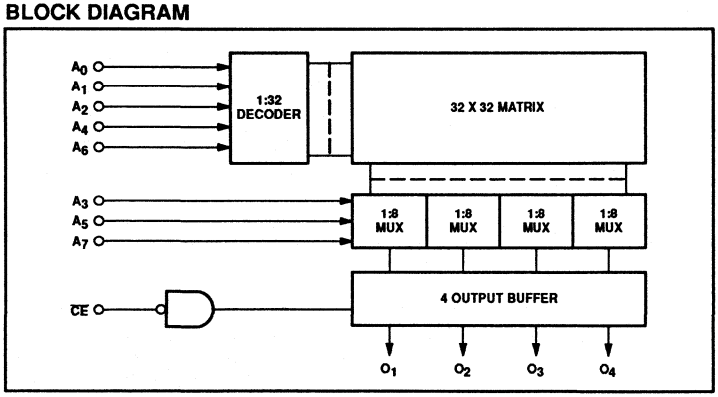
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



1K–Bit ECL Bipolar PROM (256 × 4) — 10149A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–pin Ceramic DIP (300mil–wide)	10149A F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to –3	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	–0 to +75	°C
T_{STG}	Storage temperature range	–55 to +165	°C

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

DC ELECTRICAL CHARACTERISTICS $-30°C \leq T_A \leq +75°C, -4.94V \leq V_{EE} \leq -5.46V$

			0°C		+25°C			+75°C		
SYMBOL	PARAMETER[1]	TEST CONDITIONS	Min	Max	Min	Typ[3]	Max	Min	Max	UNIT
Input voltage[2,3]										
V_{IL}	Low		–1.870		–1.850			–1.830		V
V_{IH}	High			–0.840			–0.810		–0.720	V
V_{ILA}	Low threshold			–1.480			–1.475		–1.445	V
V_{IHA}	High threshold		–1.150		–1.105			–1.040		V
Output voltage										
V_{OL}	Low	V_{IH} = Max	–1.870	–1.665	–1.850		–1.650	–1.830	–1.625	V
V_{OH}	High	V_{IL} = Min	–1.000	–0.840	–0.960		–0.810	–0.900	–0.720	V
V_{OLA}	Low threshold	V_{IHA} = Min, V_{ILA} = Max		–1.640			–1.630		–1.600	V
V_{OHA}	High threshold	V_{IHA} = Min, V_{ILA} = Max	–1.020		–0.980			–0.920		V
Input current										
I_{IL}	Low	V_{IH} = Max			0.5					µA
I_{IH}	High	V_{IL} = Min		250			250		250	µA
Supply drain current										
I_{EE}		V_{EE} = –5.2V		160		150	160		160	mA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 10K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. Typical values are at V_{EE} = –5.2V, T_A = +25°C.

1K–Bit ECL Bipolar PROM (256 × 4) — 10149A

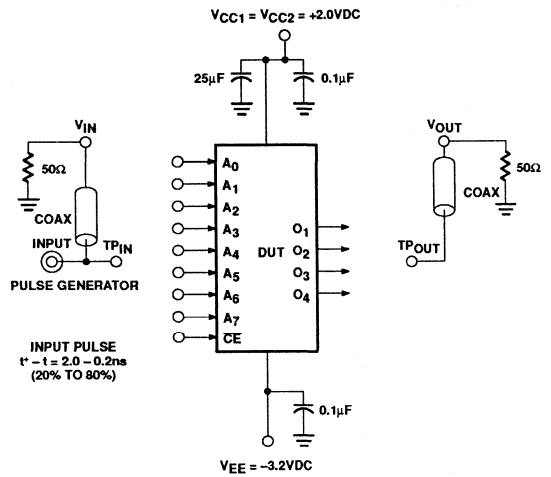
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address			10	ns
t_{CE}		Output	Chip Enable		4	6	ns
Disable time							
t_{CD}		Output	Chip Disable		4	6	ns
Rise and fall time							
t_+	Rise time (20–80%)				4.0		ns
t_-	Fall time (80–20%)				4.0		ns

NOTE:

1. Typical values are at $V_{EE} = -5.2V$, $T_A = +25°C$.

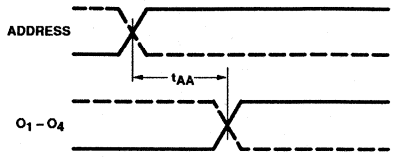
TEST LOAD CIRCUITS



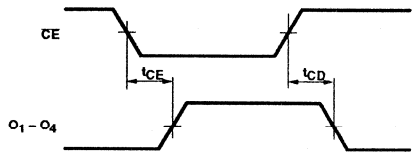
NOTES:

4. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
5. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
6. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as posstble. A 10µF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

Document No.	
ECN No.	
Date of Issue	December 1988
Status	Preliminary Specification
ECL Products	

10149B
1K-Bit ECL Bipolar PROM

DESCRIPTION

The 10149B is field programmable, meaning that custom patterns are immediately available by following the Signetics Generic IV Programming procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the TiW link matrix.

The 10149B is suitable for use in high–performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

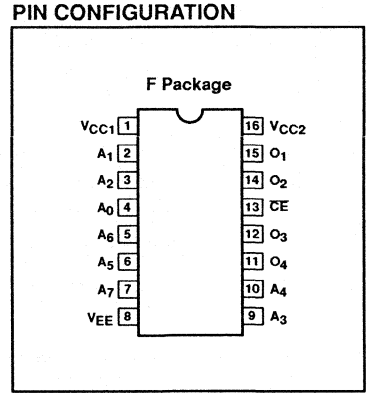
FEATURES

- **Address access time: 5ns max**
- **Power dissipation: 0.76mW/bit typ**
- **High–impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

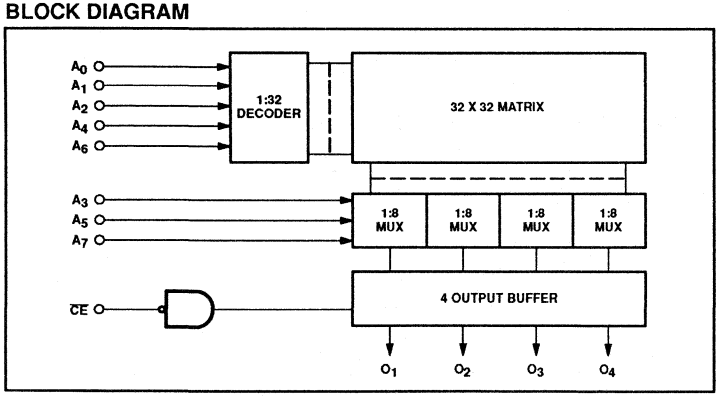
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



1K–Bit ECL Bipolar PROM (256 × 4) 10149B

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–pin Ceramic DIP (300mil–wide)	10149B F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to –3	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	–0 to +75	°C
T_{STG}	Storage temperature range	–55 to +165	°C

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER[1]	TEST CONDITIONS	0°C		+25°C			+75°C		UNIT
			Min	Max	Min	Typ[3]	Max	Min	Max	
Input voltage[2,3]										
V_{IL}	Low		–1.870		–1.850			–1.830		V
V_{IH}	High			–0.840			–0.810		–0.720	V
V_{ILA}	Low threshold			–1.480			–1.475		–1.445	V
V_{IHA}	High threshold		–1.150		–1.105			–1.040		V
Output voltage										
V_{OL}	Low	V_{IH} = Max	–1.870	–1.665	–1.850		–1.650	–1.830	–1.625	V
V_{OH}	High	V_{IL} = Min	–1.000	–0.840	–0.960		–0.810	–0.900	–0.720	V
V_{OLA}	Low threshold	V_{IHA} = Min, V_{ILA} = Max		–1.640			–1.630		–1.600	V
V_{OHA}	High threshold	V_{IHA} = Min, V_{ILA} = Max	–1.020		–0.980			–0.920		V
Input current[4]										
I_{IL}	Low	V_{IH} = Max			0.5					µA
I_{IH}	High	V_{IL} = Min		250			250		250	µA
Supply drain current										
I_{EE}		V_{EE} = –5.2V		160		150	160		160	mA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 10K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. Typical values are at V_{EE} = –5.2V, T_A = +25°C.
4. Unused input pins must have 10KΩ min to V_{EE} or be connected to $-2V_{DC}$.

1K–Bit ECL Bipolar PROM (256 × 4) — 10149B

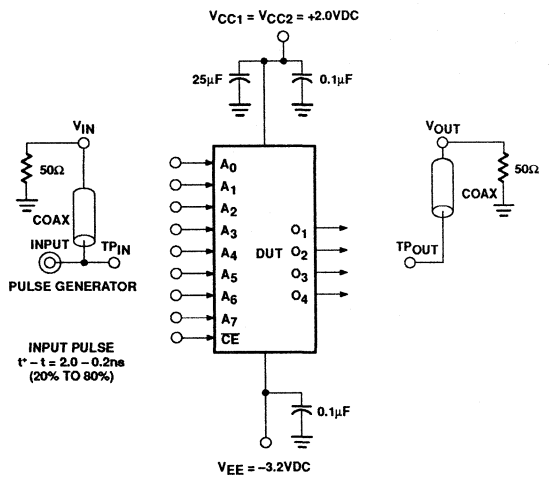
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $0°C \leq T_A \leq +75°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address			5	ns
t_{CE}		Output	Chip Enable		2	3	ns
Disable time							
t_{CD}		Output	Chip Disable		2	3	ns
Rise and fall time							
t_+	Rise time (20–80%)				2.0		ns
t_-	Fall time (80–20%)				2.0		ns

NOTE:

1. Typical values are at $V_{EE} = -5.2V$, $T_A = +25°C$.

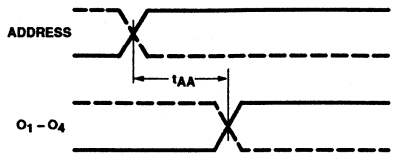
TEST LOAD CIRCUITS



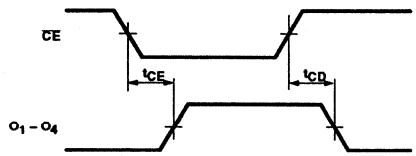
NOTES:

7. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
8. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
9. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as posstble. A 10µF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

Philips Components

Document No.	853–0134
ECN No.	86487
Date of Issue	November 11, 1986
Status	Product Specification
ECL Products	

100149
1K-Bit ECL Bipolar PROM

DESCRIPTION

The 100149 is field programmable, meaning that custom patterns are immediately available by following the ECL fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 100149 is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

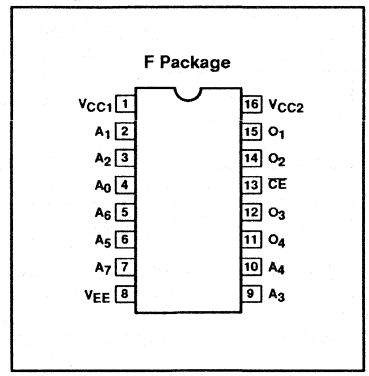
FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High-impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 100K series**

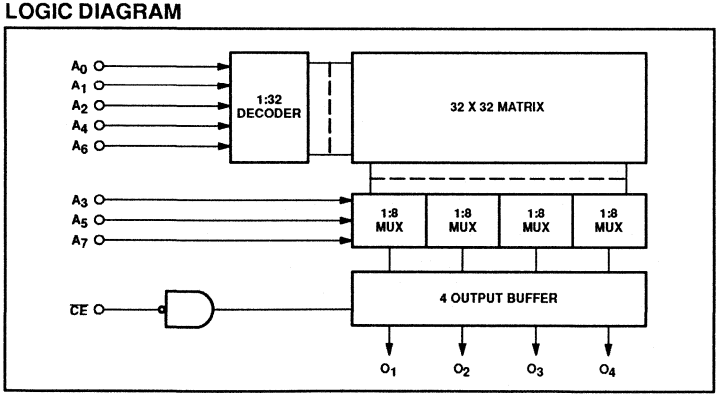
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



LOGIC DIAGRAM



1K–Bit ECL Bipolar PROM (256 × 4) 100149

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–pin Ceramic DIP (300mil–wide)	100149 F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	–0 to +75	°C
T_{STG}	Storage temperature range	–55 to +165	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C, -4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[4]	Max	
Input voltage						
V_{IL}	Low		–1.810			V
V_{IH}	High				–0.880	V
V_{ILA}	Threshold Low				–1.475	V
V_{IHA}	Threshold High		–1.165			V
Output voltage						
V_{OL}	Low	V_{IL} = Min	–1.810		–1.620	V
V_{OH}	High	V_{IH} = Max	–1.025		–0.880	V
V_{OLA}	Threshold Low	V_{IL} = Max			–1.610	V
V_{OHA}	Threshold High	V_{IH} = Min	–1.035			V
Input current						
I_{IL}	Low	V_{IL} = Min	0.5			µA
I_{IH}	High	V_{IH} = Max			220	µA
Supply current						
I_{EE}		V_{EE} = –4.5V		150	180	mA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. For current measurements, maximum is defined as the maximum absolute value.
4. Typical values are at V_{EE} = –4.5V, T_A = +25°C.

1K–Bit ECL Bipolar PROM (256 × 4) 100149

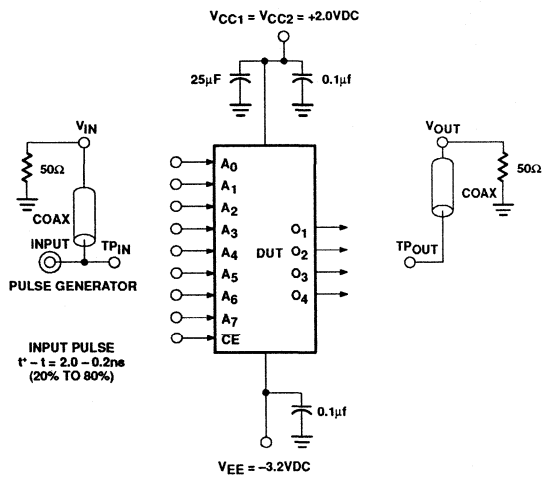
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $-4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address		15	20	ns
t_{CE}		Output	Chip Enable		5	8	ns
Disable time							
t_{CD}		Output	Chip Disable		5	8	ns
Rise and fall time							
t^+	Rise time (20–80%)				4.0		ns
t^-	Fall time (80–20%)				4.0		ns

NOTES:

1. Typical values are at $V_{EE} = -4.5V$, $T_A = +25°C$.

TEST LOAD CIRCUIT

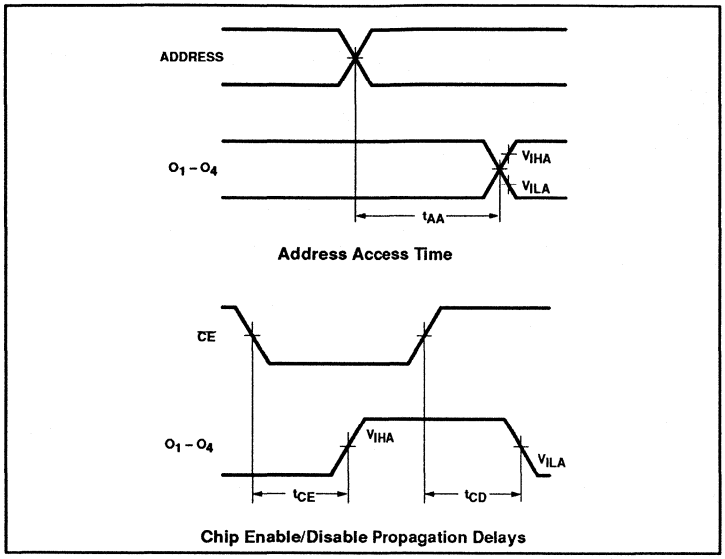


NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as posstble. A 10µF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

1K–Bit ECL Bipolar PROM (256 × 4) 100149

VOLTAGE WAVEFORMS



Document No.	853–1283
ECN No.	91142
Date of Issue	October 27, 1987
Status	Product Specification
ECL Products	

100149A
1K-Bit ECL Bipolar PROM

DESCRIPTION

The 100149A is field programmable, meaning that custom patterns are immediately available by following the ECL fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 100149A is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

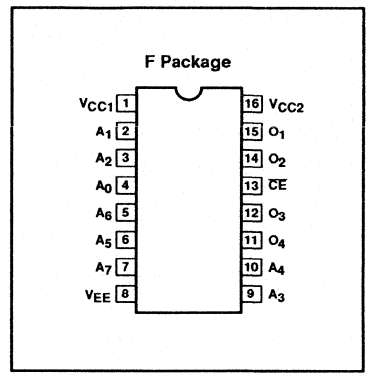
FEATURES

- **Address access time: 10ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High-impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 100K series**

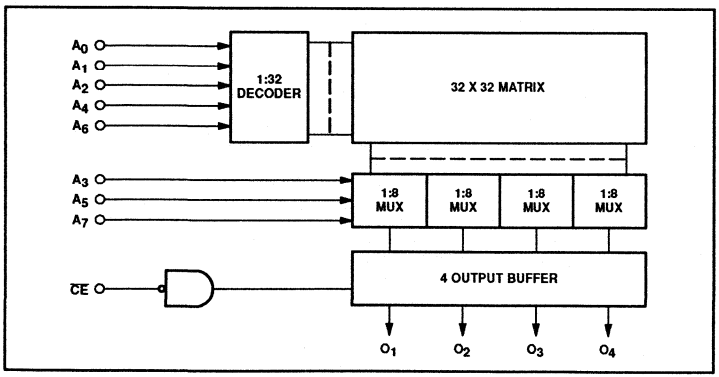
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



LOGIC DIAGRAM



1K–Bit ECL Bipolar PROM (256 × 4) — 100149A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–pin Ceramic DIP (300mil–wide)	100149A F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	–0 to +75	°C
T_{STG}	Storage temperature range	–55 to +165	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, –4.275V ≤ V_{EE} ≤ –4.725V

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[4]	Max	
Input voltage						
V_{IL}	Low		–1.810			V
V_{IH}	High				–0.880	V
V_{ILA}	Threshold Low				–1.475	V
V_{IHA}	Threshold High		–1.165			V
Output voltage						
V_{OL}	Low	V_{IL} = Min	–1.810		–1.620	V
V_{OH}	High	V_{IH} = Max	–1.025		–0.880	V
V_{OLA}	Threshold Low	V_{IL} = Max			–1.610	V
V_{OHA}	Threshold High	V_{IH} = Min	–1.035			V
Input current						
I_{IL}	Low	V_{IL} = Min	0.5			µA
I_{IH}	High	V_{IH} = Max			220	µA
Supply current						
I_{EE}		V_{EE} = –4.5V		150	160	mA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. For current measurements, maximum is defined as the maximum absolute value.
4. Typical values are at V_{EE} = –4.5V, T_A = +25°C.

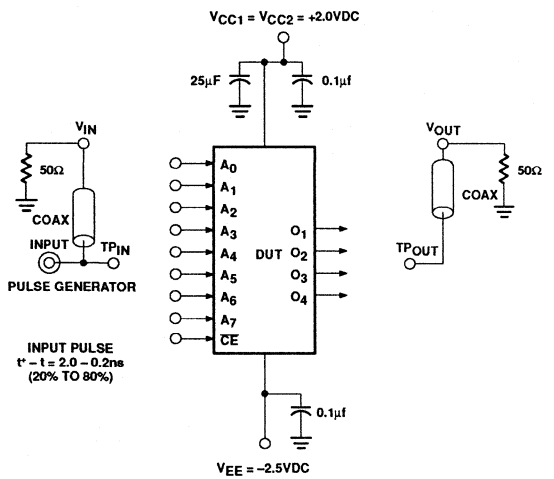
1K–Bit ECL Bipolar PROM (256 × 4) — 100149A

AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $-4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address			10	ns
t_{CE}		Output	Chip Enable		5	6	ns
Disable time							
t_{CD}		Output	Chip Disable		5	6	ns
Rise and fall time							
t^+	Rise time (20–80%)				4.0		ns
t^-	Fall time (80–20%)				4.0		ns

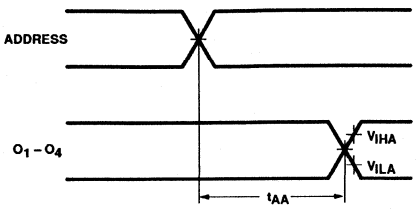
NOTES:
1. Typical values are at $V_{EE} = -4.5V$, $T_A = +25°C$.

TEST LOAD CIRCUIT

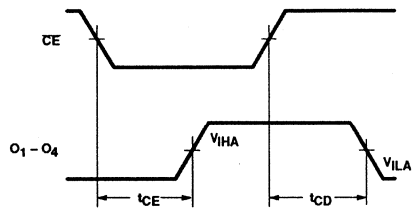


NOTES:
1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as posstble. A 10µF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

Philips Components

Document No.	
ECN No.	
Date of Issue	January 1989
Status	Preliminary Specification
ECL Products	

100149B
1K-Bit ECL Bipolar PROM

DESCRIPTION

The 100149B is field programmable, meaning that custom patterns are immediately available by following the Signetics Generic IV Programming procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the TiW link matrix.

The 100149B is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

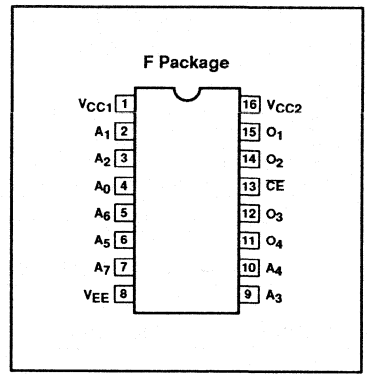
FEATURES

- **Address access time: 5ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High-impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 100K series**

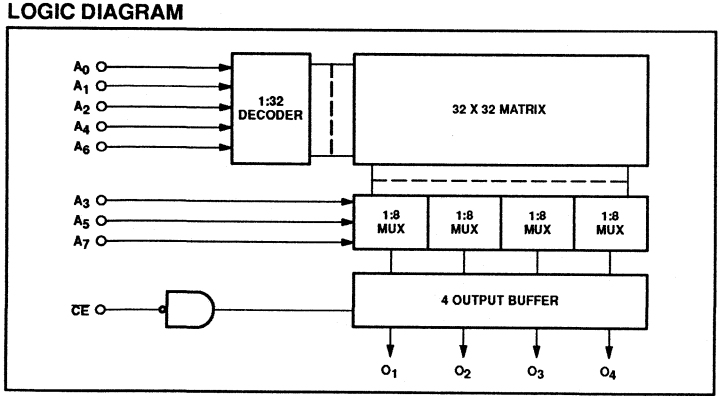
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



LOGIC DIAGRAM



1K–Bit ECL Bipolar PROM (256 × 4) 100149B

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–pin Ceramic DIP (300mil–wide)	100149B F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to –3	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	–0 to +75	°C
T_{STG}	Storage temperature range	–55 to +165	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C, -4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[4]	Max	
Input voltage						
V_{IL}	Low		–1.810			V
V_{IH}	High				–0.880	V
V_{ILA}	Threshold Low				–1.475	V
V_{IHA}	Threshold High		–1.165			V
Output voltage						
V_{OL}	Low	V_{IL} = Min	–1.810		–1.620	V
V_{OH}	High	V_{IH} = Max	–1.025		–0.880	V
V_{OLA}	Threshold Low	V_{IL} = Max			–1.610	V
V_{OHA}	Threshold High	V_{IH} = Min	–1.035			V
Input current[5]						
I_{IL}	Low	V_{IL} = Min	0.5			µA
I_{IH}	High	V_{IH} = Max			220	µA
Supply current						
I_{EE}		V_{EE} = –4.5V		150	160	mA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. For current measurements, maximum is defined as the maximum absolute value.
4. Typical values are at V_{EE} = –4.5V, T_A = +25°C.
5. Unused inputs must have 10KΩ minimum to V_{EE} or be connected to $-2V_{DC}$.

1K–Bit ECL Bipolar PROM (256 × 4) — 100149B

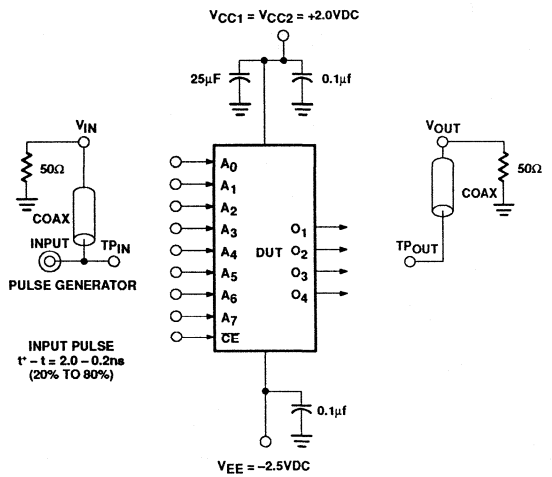
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $0°C \leq T_A \leq +75°C$, $-4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address			5	ns
t_{CE}		Output	Chip Enable		2	3	ns
Disable time							
t_{CD}		Output	Chip Disable		2	3	ns
Rise and fall time							
t^+	Rise time (20–80%)				2.0		ns
t^-	Fall time (80–20%)				2.0		ns

NOTES:

1. Typical values are at $V_{EE} = -4.5V$, $T_A = +25°C$.

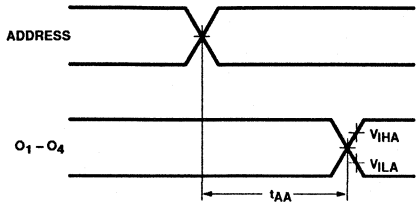
TEST LOAD CIRCUIT



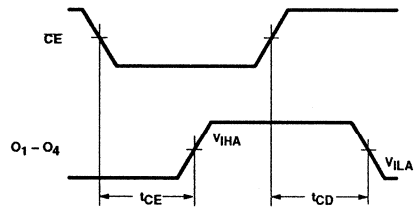
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as posstble. A 10µF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

Document No.	853–1423
ECN No.	99373
Date of Issue	April 17, 1990
Status	Product Specification
ECL Products	

10H20EV8/10020EV8
ECL Programmable Array Logic

DESCRIPTION

The 10H20EV8/10020EV8 is an ultra high-speed universal ECL PAL®-type device. Combining versatile output macrocells with a standard AND/OR single programmable array, this device is ideal in implementing a user's custom logic. The use of Signetics state-of-the-art bipolar oxide isolation process enables the 10H20EV8/10020EV8 to achieve optimum speed in any design. The AMAZE design software package from Signetics simplifies design entry based upon Boolean or state equations.

The 10H20EV8/10020EV8 is a two-level logic element comprised of 11 fixed inputs, an input pin that can either be used as a clock or 12th input, 90 AND gates, and 8 Output Logic Macrocells. Each Output Macrocell can be individually configured as a dedicated input, dedicated output with polarity control, a bidirectional I/O, or as a registered output that has both output polarity control and feedback to the AND array. This gives the part the capability of having up to 20 inputs and eight outputs.

The 10H20EV8/10020EV8 has a variable number of product terms that can be OR'd per output. Four of the outputs have 12 AND terms available and the other four have 8 terms per output. This allows the designer the extra flexibility to implement those functions that he couldn't in a standard PAL device. Asynchronous Preset and Reset product terms are also included for system design ease. Each output has a separate output enable product term. Another feature added for the system designer is a power-up Reset on all registered outputs.

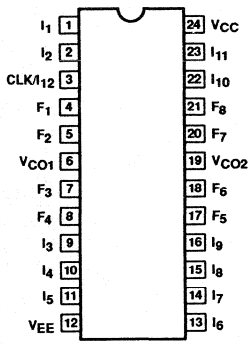
The 10H20EV8/10020EV8 also features the ability to Preload the registers to any desired state during testing. The Preload is not affected by the pattern within the device, so can be performed at any step in the testing sequence. This permits full logical verification even after the device has been patterned.

FEATURES

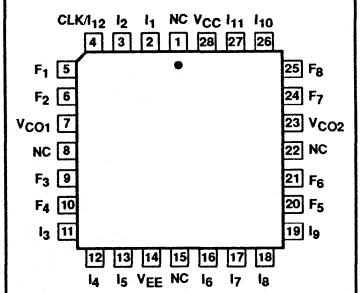
- **Ultra high speed ECL device**
  - **t_{PD} = 4.5ns (max)**
  - **t_{IS} = 2.7ns (max)**
  - **t_{CKO} = 2.2ns (max)**
  - **f_{MAX} = 208MHz**
- **Universal ECL Programmable Array Logic**
  - **8 user programmable output macrocells**
  - **Up to 20 inputs and 8 outputs**
  - **Individual user programmable output polarity**
- **Variable product term distribution allows increased design capability**
- **Asynchronous Preset and Reset capability**
- **10KH and 100K options**
- **Power-up Reset and Preload function to enhance state machine design and testing**
- **Design support provided via AMAZE and other CAD tools**
- **Security fuse for preventing design duplication**
- **Available in 24-Pin 300mil-wide DIP and 28-Pin PLCC.**

PIN CONFIGURATIONS

F Package



A Package



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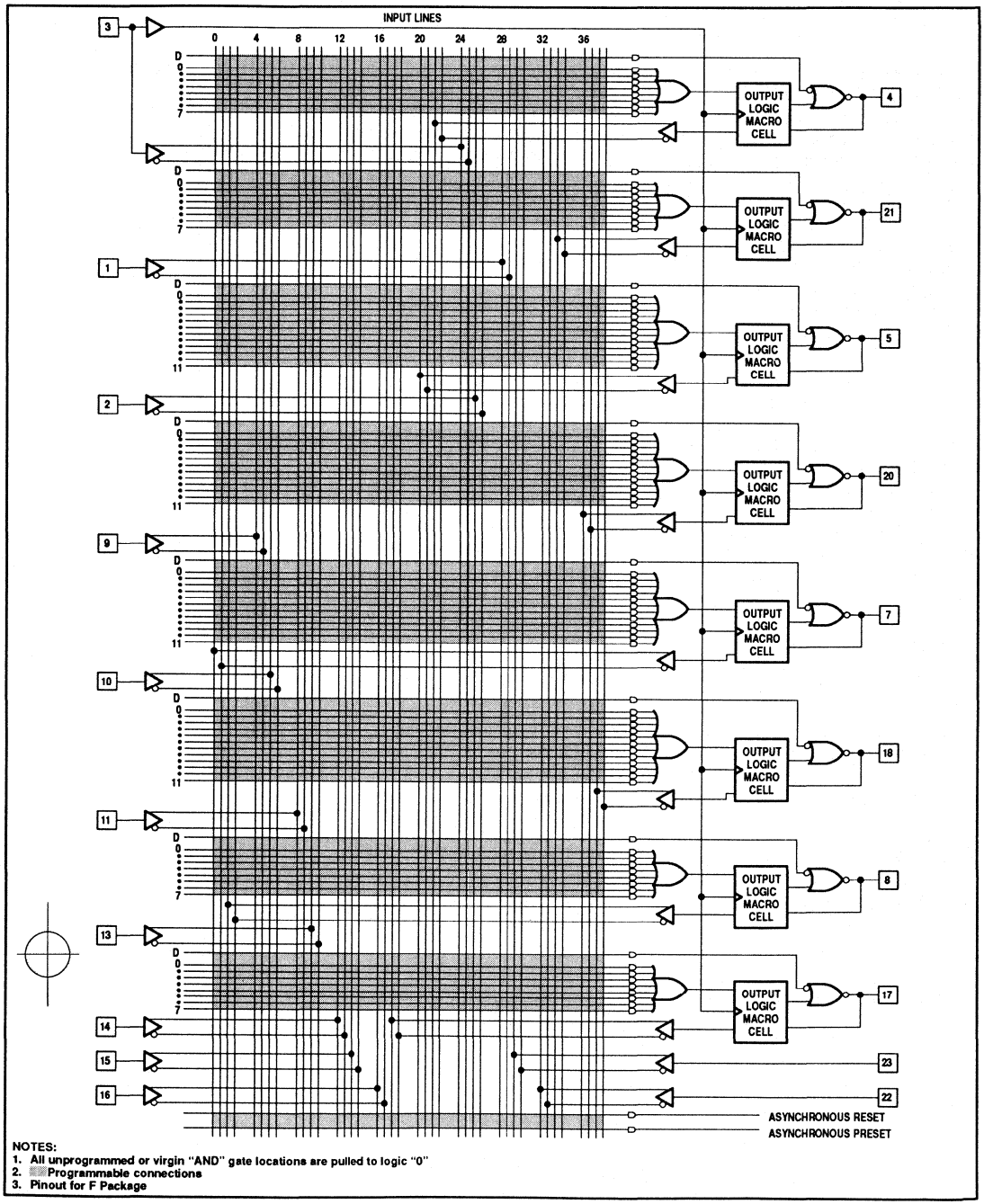
ECL Programmable Array Logic 10H20EV8/10020EV8

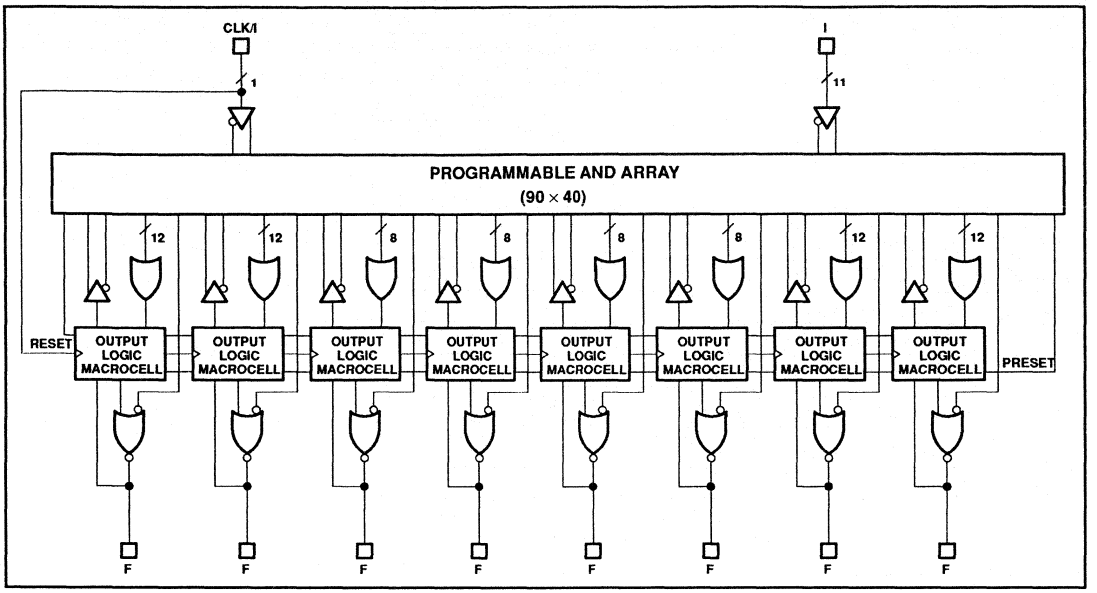
LOGIC DIAGRAM



NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0"
2. ▒ Programmable connections
3. Pinout for F Package

ECL Programmable Array Logic 10H20EV8/10020EV8

FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

The 10H20EV8/10020EV8 is an ultra high-speed universal ECL PAL-type device. Combining versatile Output Macrocells with a standard AND/OR single programmable array, this device is ideal in implementing a user's custom logic.

As can be seen in the Logic Diagram, the device is a two-level logic element with a programmable AND array. The 20EV8 can have up to 20 inputs and 8 outputs. Each output has a versatile Macrocell whereby the output can either be configured as a dedicated input, a dedicated combinatorial output with polarity control, a bidirectional I/O, or as a registered output that has both output polarity control and feedback into the AND array.

The device also features 90 product terms. Two of the product terms can be used for a global asynchronous preset and/or reset. Eight of the product terms can be used for individual output enable control of each Macrocell. The other 80 product terms are distributed among the outputs. Four of the outputs have eight product terms, while the other four have 12. This arrangement allows the utmost in flexibility when implementing user patterns.

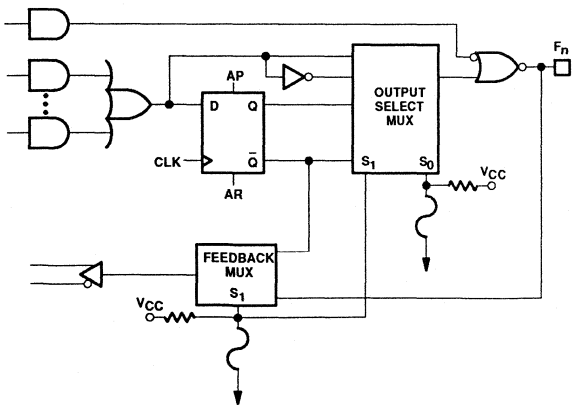


Figure 1. Output Logic Macrocell

Output Logic Macrocell

The 10H20EV8/10020EV8 incorporates an extremely versatile Output Logic Macrocell that allows the user complete flexibility when configuring outputs.

As seen in Figure 1, the 10H20EV8/10020EV8 Output Logic Macrocell consists of an edge-triggered D-type flip-flop, an output select MUX, and a feedback select MUX. Fuses S_0 and S_1 allow the user to select between the various cells. S_1 controls whether the output will be either registered with internal feedback or combinatorial I/O. S_0 controls the polarity of the output (Active-HIGH or Active-LOW). This allows the user to achieve the following configurations: Registered Active-HIGH output, Registered Active-LOW output, Combinatorial Active-HIGH output, and Combinatorial Active-LOW output. With the output enable product term, this list can be extended by adding the configurations of a Combinatorial I/O with Polarity or another input.

ECL Programmable Array Logic — 10H20EV8/10020EV8

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic Dual In-Line (300mil-wide)	10H20EV8–6F 10H20EV8–4F 10020EV8–6F 10020EV8–4F
28-Pin Plastic Leaded Chip Carrier	10H20EV8–6A 10H20EV8–4A 10020EV8–6A 10020EV8–4A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating Temperature range	0 to +75 (10KH) 0 to +85 (100K)	°C
T_{STG}	Storage Temperature range	–55 to +150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

OPERATING RANGES

DEVICE	SYMBOL	PARAMETER	RATINGS		UNIT
			Min	Max	
10H20EV8	V_{EE}	Supply voltage	–5.46	–4.94	V_{DC}
	T_A	Operating free-air temperature	0	+75	°C
10020EV8	V_{EE}	Supply voltage	–4.8	–4.2	V_{DC}
	T_A	Operating free-air temperature	0	+85	°C

ECL Programmable Array Logic 10H20EV8/10020EV8

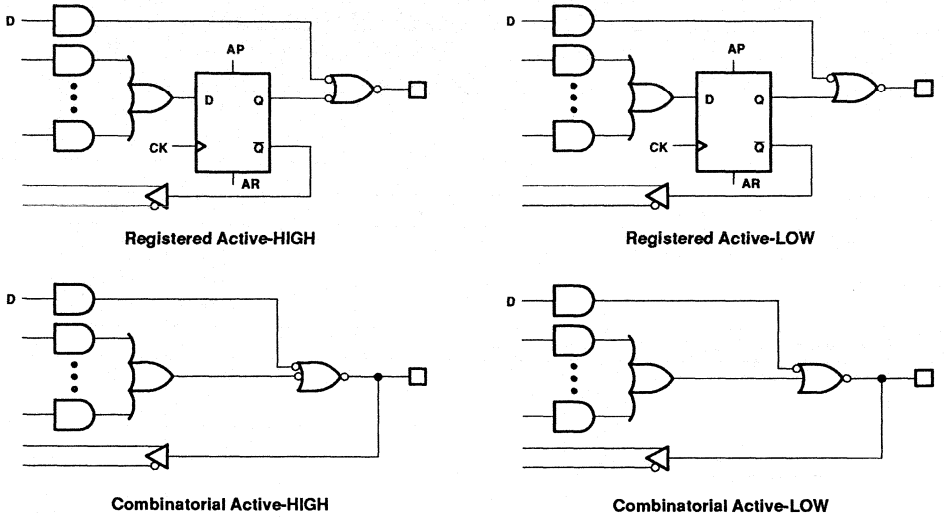


Figure 2. Output Macro Cell Configurations

OUTPUT MACRO CELL CONFIGURATION

Shown in Figure 2 are the four possible configurations of the output macrocell using fuses S_0 and S_1. As seen, the output can either be registered Active-HIGH/LOW with feedback or combinatorial Active-HIGH/LOW with feedback. If the registered mode is chosen, the feedback is from the $\overline{Q}$ output to the AND array enables one to make state machines or shift registers without having to tie the output to one of the inputs. If a combinatorial output is chosen, the feedback gate is enabled from the pin and allows one to create permanent outputs, permanent inputs, or I/O pins through the use of the output enable (D) product term.

OUTPUT ENABLE

Each output on the 10H20EV8/10020EV8 has its own individual product term for output enable. The use of the D product term (direction control) allows the user three possible configurations of the outputs. They are always enabled, always disabled, and controlled by a programmed pattern. A HIGH on the D term enables the output, while a LOW performs the disable function. Output enable control can be achieved by programming a pattern on the D term.

The output enable control can also be used to expand a designer's possibilities once a combinatorial output has been chosen. If the D term is always HIGH, the pin becomes a permanent Active-HIGH/LOW output. If the D term is always LOW (all fuses left intact), the pin now becomes an extra input.

PRESET AND RESET

The 10H20EV8/10020EV8 also includes a separate product term for asynchronous Preset and asynchronous Reset. These lines are common for all registers and are asserted when the specific product term goes HIGH. Being asynchronous, they are independent of the clock. It should be noted that the actual state of the output is dependent on how the polarity of the particular output has been chosen. If the outputs are a mix of Active-HIGH and Active-LOW, a Preset signal will force the Active-HIGH outputs HIGH while the Active-LOW outputs would go LOW, even though the Q output of all flip-flops would go HIGH. A Reset signal would force the opposite conditions.

PRELOAD

To simplify testing, the 10H20EV8/10020EV8 has also included PRELOAD circuitry. This allows a user to load any particular data desired into the registers regardless of the programmed pattern. This means that the PRELOAD can be done on a blank part and after that same part has been programmed to facilitate any post-fuse testing desired.

It can also be used by a designer to help debug his/her circuit. This could be important if a state machine was implemented in the 10H20EV8/10020EV8. The PRELOAD would allow a designer to enter any state in the sequence desired and start clocking from that particular point. Any or all transitions could be verified.

AMAZE

The AMAZE PLD Design Software development system also supports the 10H20EV8/10020EV8. AMAZE provides the following capabilities for the 10H20EV8/10020EV8:

- State equation entry
- Boolean equation entry
- Logic and timing simulation
- Automatic test vector generation

AMAZE operates on an IBM PC/XT, PC/AT, PS/2, or any compatible system with DOS 2.0 or higher. The minimum system configuration for AMAZE is 640K bytes of RAM and a hard disk.

AMAZE compiles the design after completion for syntax and completeness. Programming data is generated in JEDEC format.

DESIGN SECURITY

The 10H20EV8/10020EV8 has a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

DC ELECTRICAL CHARACTERISTICS

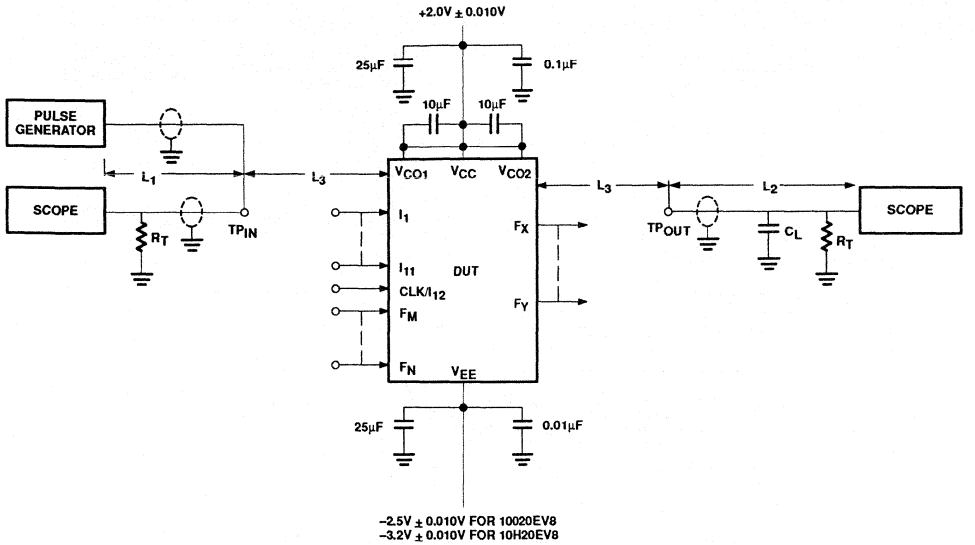
10H20EV8: $0°C \leq T_A \leq +75°C$, $V_{EE} = -5.2V \pm 5\%$, $V_{CC} = V_{CO1} = V_{CO2} = GND$
10020EV8: $0°C \leq T_A \leq +85°C$, $-4.8V \leq V_{EE} \leq -4.2V$, $V_{CC} = V_{CO1} = V_{CO2} = GND$

SYMBOL	PARAMETER[1]	TEST CONDITIONS[2]		T_A	LIMITS Min	LIMITS Max	UNITS
V_{OH}	High level output voltage	$V_{IN} = V_{IH}$ Max. or V_{IL} Min.	10KH	0°C +25°C +75°C	−1020 −980 −920	−840 −810 −735	mV
			100K	0°C to 85°C	−1025	−880	mV
V_{OHT}	High level output threshold voltage	$V_{IN} = V_{IH}$ Max. or V_{IL} Min.	100K	0°C to 85°C	−1035		mV
V_{OL}	Low level output voltage	$V_{IN} = V_{IH}$ Max. or V_{IL} Min.	10KH	0°C +25°C +75°C	−1950 −1950 −1950	−1630 −1630 −1600	mV
			100K	0°C to 85°C	−1810	−1620	mV
V_{OLT}	Low level output threshold voltage	$V_{IN} = V_{IH}$ Max. or V_{IL} Min.	100K	0°C to 85°C		−1610	mV
V_{IH}	High level input voltage	Guaranteed input voltage high for all inputs	10KH	0°C +25°C +75°C	−1170 −1130 −1070	−840 −810 −735	mV
			100K	0°C to 85°C	−1165	−880	mV
V_{IL}	Low level input voltage	Guaranteed input voltage low for all inputs	10KH	0°C +25°C +75°C	−1950 −1950 −1980	−1480 −1480 −1450	mV
			100K	0°C to 85°C	−1810	−1475	mV
I_{IH}	High level input current	$V_{IN} = V_{IH}$ Max.	10KH	0°C +75°C		220	µA
			100K	0°C to 85°C			
I_{IL}	Low level input current	$V_{IN} = V_{IL}$ Min. Except I/O Pins	10KH	0°C +75°C	0.3		µA
			100K	0°C to 85°C	0.5		
I_{EE}	Supply current	V_{EE} = Max. All inputs and outputs open	10KH	0°C to 75°C	−230		mA
			100K	0°C to 85°C			

NOTES:
1. All voltage measurements are referenced to the ground terminal.
2. Each ECL 10KH/100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 (150 meters) linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to −2V.
3. Terminals not specifically referenced can be left electrically open. Open inputs assume a logic LOW state. Any unused pins can be terminated to −2V. If tied to V_{EE}, it must be through a resistor > 10K.

ECL Programmable Array Logic 10H20EV8/10020EV8

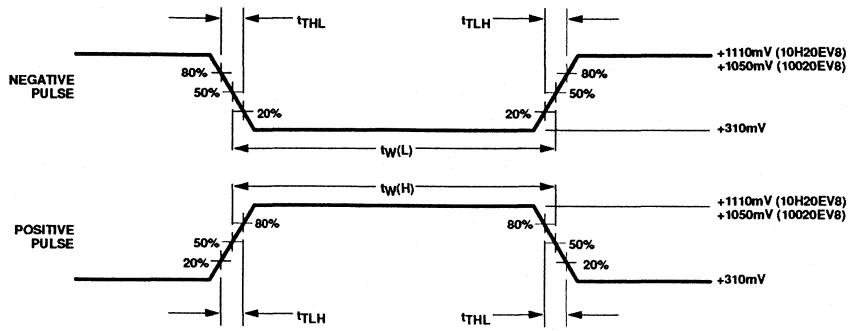
AC TEST CIRCUIT



NOTES:

1. Use decoupling capacitors of 0.1μF and 25μF from GND to V_{CC}, and 0.01μF and 25μF from GND to V_{EE} (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than $^1/_4$ inch (6mm).
2. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
3. All unused outputs are loaded with 50Ω to GND.
4. L_1 and L_2 are equal length 50Ω impedance lines. L_3, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed $^1/_4$ inch (6mm).
5. R_T = 50Ω terminator internal to Scope.
6. The unmatched wire stub between coaxial cable and pins under test must be less than $^1/_4$ inch (6mm) long for proper test.
7. C_L = Fixture and stray capacitance ≤ 3pF.
8. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed $^1/_4$ inch (6mm) in length (refer to section on AC setup procedure).
9. All 50Ω resistors should have tolerance of ± 1% or better.
10. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
11. Two 10μF capacitors between V_{CC} and V_{CO1} and V_{CO2} respectively located as close to the device as possible is recommended to reduce ringing.
12. Normal practice in test fixtures layout should be followed. Lead lengths, particular to the power supply, should be as short as possible.

VOLTAGE WAVEFORMS



INPUT PULSE REQUIREMENTS $V_{CC} = V_{CO1} = V_{CO2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, V_T = GND (0V)					
FAMILY	AMPLITUDE	REP RATE	PULSE WIDTH	t_{TLH}	t_{THL}
10KH ECL	800mV$_{p-p}$	1MHz	500ns	1.3 ± 0.2ns	1.3 ± 0.2ns
INPUT PULSE REQUIREMENTS $V_{CC} = V_{CO1} = V_{CO2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, V_T = GND (0V)					
FAMILY	AMPLITUDE	REP RATE	PULSE WIDTH	t_{TLH}	t_{THL}
100K ECL	740mV$_{p-p}$	1MHz	500ns	0.7 ± 0.1ns	0.7 ± 0.1ns

Input Pulse Definition

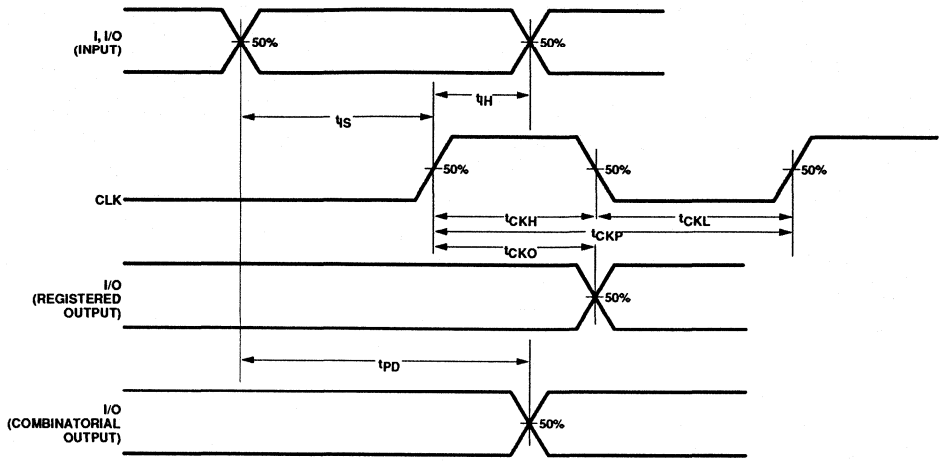
AC ELECTRICAL CHARACTERISTICS

10H20EV8: $0°C \leq T_A \leq +75°C$, $V_{EE} = -5.2V \pm 5\%$, $V_{CC} = V_{CO1} = V_{CO2} = GND$
10020EV8: $0°C \leq T_A \leq +85°C$, $-4.8V \leq V_{EE} \leq -4.2V$, $V_{CC} = V_{CO1} = V_{CO2} = GND$

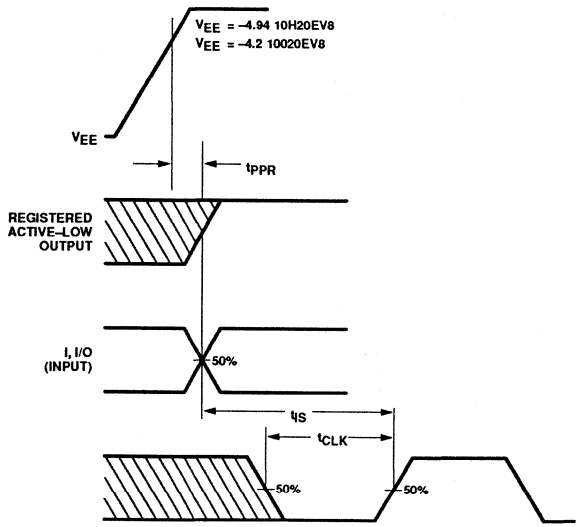
SYMBOL	PARAMETER	FROM	TO	TEST CONDITIONS[1]	LIMITS				UNIT
					–4		–6		
					Min	Max	Min	Max	
Pulse Width									
t_{CKH}	Clock High	CLK +	CLK –		2		3		ns
t_{CKL}	Clock Low	CLK –	CLK +		2		3		ns
t_{CKP}	Clock Period	CLK +	CLK +		4		6		ns
t_{PRH}	Preset/Reset Pulse	(I, I/O) ±	(I, I/O) ±		4.5		6		ns
Setup and Hold Time									
t_{IS}	Input	(I, I/O) ±	CLK +		2.7		4		ns
t_{IH}	Input	CLK +	(I, I/O) ±		0		0		ns
t_{PRS}	Clock Resume after Preset/Reset	(I, I/O) ±	CLK +		4.5		6		ns
Propagation Delay									
t_{PD}	Input	(I, I/O) ±	I/O ±			4.5		6	ns
t_{CKO}	Clock	CLK +	I/O ±			2.2		3	ns
t_{OE}	Output Enable	(I, I/O) ±	I/O			4		6	ns
t_{OD}	Output Disable	(I, I/O) ±	I/O			4		6	ns
t_{PRO}	Preset/Reset	(I, I/O) ±	I/O ±			4.5		6	ns
t_{PPR}	Power–on Reset	V_{EE}	I/O			10			ns

NOTES:
1. Refer to AC Test Circuit and Voltage Wafeforms diagrams.

TIMING DIAGRAMS



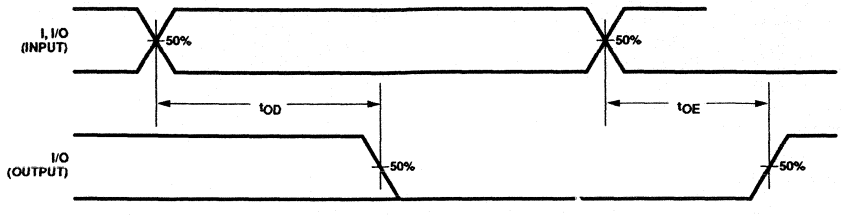
Flip–Flop and Gate Outputs



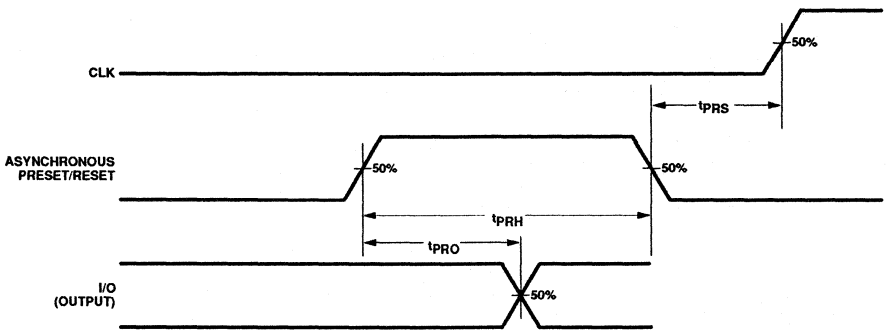
Power–On Reset

ECL Programmable Array Logic 10H20EV8/10020EV8

TIMING DIAGRAMS (Continued)



Output Enable/Disable

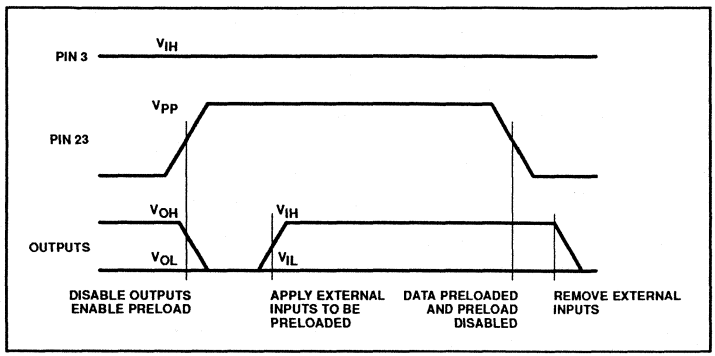


Asynchronous Preset/Reset

REGISTER PRELOAD

The 10H20EV8/10020EV8 has included circuitry that allows a user to load data into the output registers. Register PRELOAD can be done at any time and is not dependent on any particular pattern programmed into the device. This simplifies the ability to fully verify logic states and sequences even after the device has been patterned.

The pin levels and sequence necessary to perform the register PRELOAD are shown below.



SYMBOL	PARAMETER	LIMITS			UNIT
		Min.	Typ.	Max	
V_{IH}	Input HIGH level during PRELOAD and Verify	–1.1	–0.9	–0.7	V
V_{IL}	Input LOW level during PRELOAD and Verify	–1.85	–1.65	–1.45	V
V_{PP}	PRELOAD enable voltage applied to I_{11}	1.45	1.6	1.75	V

NOTE:

1. Unused inputs should be handled as follows:
   - Set at V_{IH} or V_{IL}
   - Terminated to –2V
   - Tied to V_{EE} through a resistor > 10K
   - Open

ECL Programmable Array Logic 10H20EV8/10020EV8

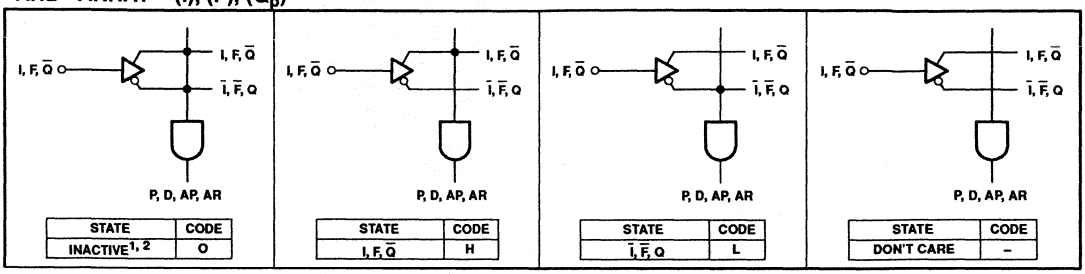
LOGIC PROGRAMMING

10H20EV8/10020EV8 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

10H20EV8/10020EV8 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, F, Q, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

"AND" ARRAY – (I), (F), ($\overline{Q}_p$)



NOTES:
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (P, D, AP, AR) will be unconditionally inhibited if any one of the I, F or Q link pairs is left intact.

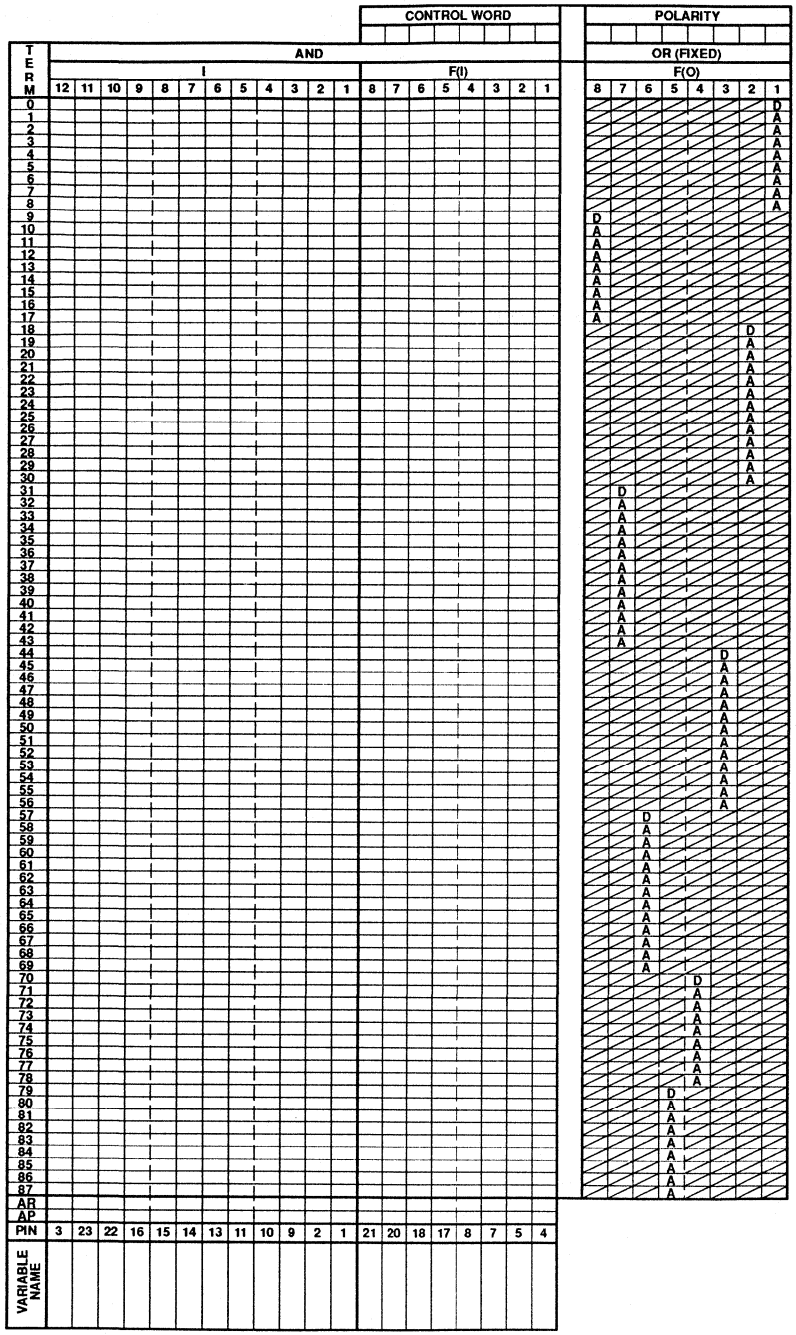
OUTPUT MACROCELL CONFIGURATIONS

OUTPUT MACROCELL CONFIGURATION	CONTROL WORD FUSE	POLARITY FUSE
Registered Output, Active–HIGH	D	H
Registered Output, Active–LOW	D[1]	L[1]
Combinatorial I/O, Active–HIGH	B	H
Combinatorial I/O, Acitve–LOW	B	L

NOTES:
1. This is the initial (unprogrammed) state of the device.

ECL Programmable Array Logic 10H20EV8/10020EV8

PROGRAM TABLE



Section 9
Package Outlines

INDEX

Data Information 655
Soldering Recommendation 656

Package Outlines and Soldering Recommendations

ECL Products

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions are shown in metric units (Millimeters) and English units (Inches).
2. Thermal resistance values are determined by temperature–sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. The substrate diode of a bipolar technology device is generally the diode used in these tests. Die size and test environment have significant effects on thermal resistance values.

Plastic DIP

3. Lead material: Copper Alloy, solder (63% Sn/37% Pb) dipped.
4. Body material: Plastic (Epoxy).
5. Index on top denotes lead No. 1 for Plastic Dual–in–Line packages.
6. Body dimensions do not include molding flash.

PLCC and Plastic SO

7. Lead material: Copper alloy, solder (90% Sn/10% Pb) plated.
8. Body material: Plastic (Epoxy).
9. Index in top center denotes lead No. 1 for PLCC.
10. Body dimensions do not include molding flash.

Ceramic DIP and Flat Pack

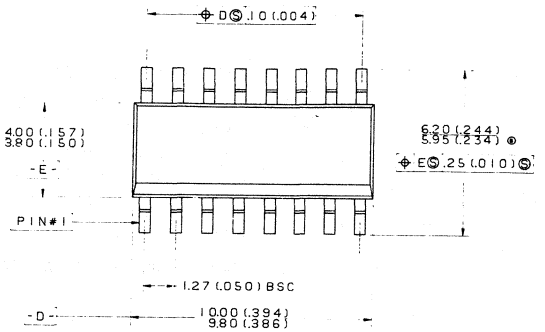
11. Lead material: Alloy 42, Tin–plated or solder (60% Sn/40% Pb) dipped.
12. Body material: Alumina with glass seal at leads.
13. Lid material: Alumina, glass seal.

ECL PACKAGES

PKG TYPE	NUMBER OF LEADS	PKG WIDTH	PKG ORDER CODE	PKG OUTLINE CODE	THERMAL RESISTANCE θ_{JA}/θ_C (°C/W)	DIE SIZE (SQUARE MILS)	TEST CONDITIONS	
							TEST AMBIENT	TEST FIXTURE
Plastic DIP	16–pin	0.300", lead row centers	N	NJ1	83/39	5,000	Still air at room temp.	Device in Textool ZIF socket with 0.040" stand–off. Accuracy: ±15%
	24–pin	0.600", lead row centers	N	NN3	56/28	8,000		
PLCC	28–pin	0.453", body width	A	AQ1	64/27	14,500	Still air at room temp.	Device soldered to Philips glass epoxy test board (2.24" X 2.24" X 0.062") with 0.005" – 0.015" stand–off. Accuracy: ±15%
Plastic SO	16–pin	0.150", body width	D	DJ1	167/36	2,500	Still air at room temp.	Device soldered to Philips glass epoxy test board (1.12" X 0.75" X 0.059") with 0.008" – 0.009" stand–off. Accuracy: ±15%
Ceramic DIP	16–pin	0.300" lead row centers	F	FJ1	98/15	6,000	Still air at room temp.	Device in Textool ZIF socket with 0.040" stand–off. Accuracy: ±15%
	24–pin		F	FN1	62/6	26,000		
	24–pin	0.400", lead row centers	F	FN2	66/10	9,000		
	24–pin	0.600", lead row centers	F	FN3	59/11	8,000		
Ceramic-Flat pack	24–pin	0.375" body width	Y	YN1	To be determined	9,000	Still air at room temp.	Device in Textool socket with plastic carrier. Accuracy: ±15%

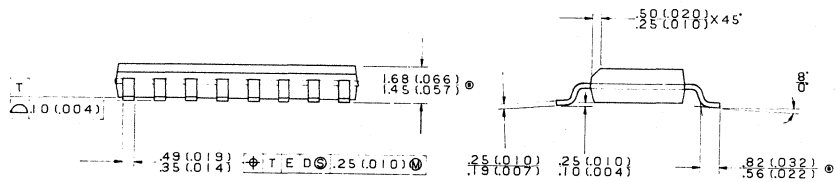
Package Outlines and Soldering Recommendation

16–PIN PLASTIC SMALL OUTLINE (SO)



NOTES

1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-012-AC FOR STANDARD SMALL OUTLINE (SO) PACKAGE. 16 LEADS. 3.75MM (.150") BODY WIDTH (ISSUE A. JUNE 1985).
2. CONTROLLING DIMENSIONS ARE MM. INCH DIMENSIONS IN PARENTHESES.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T", "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15MM (.006") ON ANY SIDE.
5. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#16 WHEN VIEWED FROM TOP.
6. SIGNETICS ORDERING CODE FOR A PRODUCT PACKAGED IN A PLASTIC SMALL OUTLINE (SO) PACKAGE IS THE SUFFIX D AFTER THE PRODUCT NUMBER.

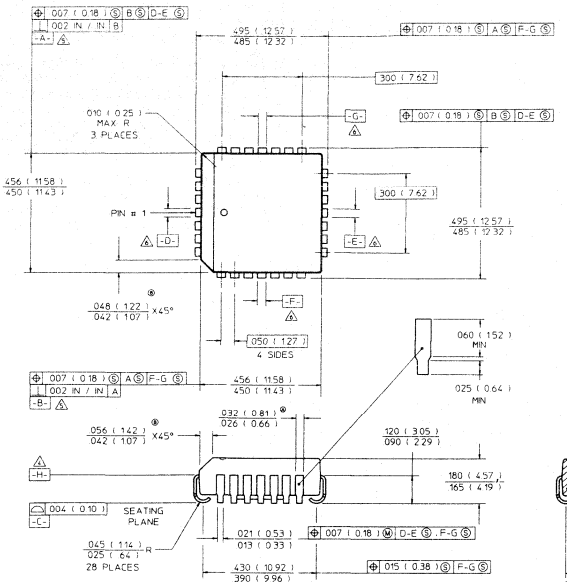


853-0005 91504

DJ1

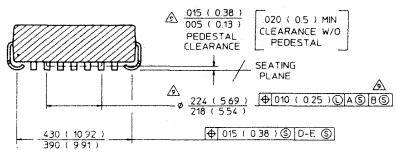
Package Outlines and Soldering Recommendation

28–PIN PLASTIC LEADED CHIP CARRIER (PLCC)



NOTES:

1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MO-047-AB FOR PLASTIC LEADED CHIP CARRIER 28 LEADS, .050 INCH LEAD SPACING, SQUARE. (ISSUE A, 10/31/84)
2. CONTROLLING DIMENSIONS: INCHES. METRIC DIMENSIONS (IN mm) ARE SHOWN IN PARENTHESES.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
4. DATUM PLANE -H- LOCATED AT THE TOP OF MOLD PARTING LINE AND COINCIDENT WITH TOP OF LEAD, WHERE LEAD EXITS PLASTIC BODY.
5. LOCATION TO DATUM -A- AND -B- TO BE DETERMINED AT PLANE -H-. THESE DATUMS DO NOT INCLUDE MOLD FLASH. MOLD FLASH PROTRUSION SHALL NOT EXCEED .006" (0.15 mm) ON ANY SIDE.
6. DATUM D-E AND F-G ARE DETERMINED WHERE THESE CENTER LEADS EXIT FROM THE BODY AT PLANE -H-.
7. PIN NUMBERS CONTINUE COUNTERCLOCKWISE TO PIN 28 (TOP VIEW).
8. SIGNETICS ORDER CODE FOR PRODUCT PACKAGED IN A PLCC IS THE SUFFIX "A" AFTER THE PRODUCT NUMBER.
9. APPLICABLE TO PACKAGES WITH PEDESTAL ONLY.

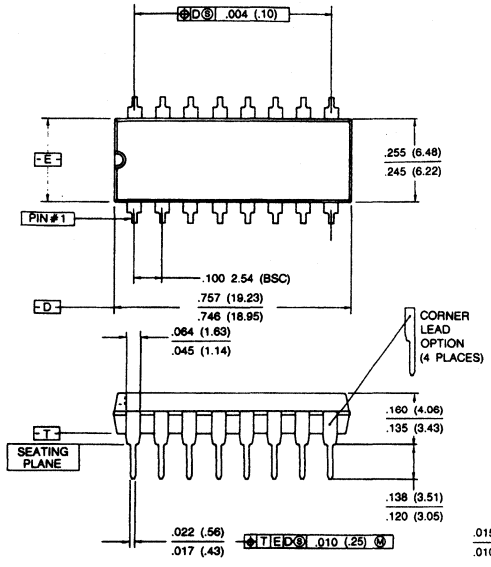


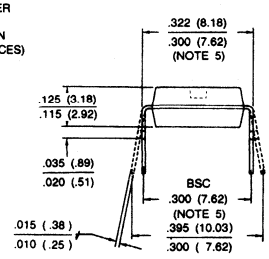
853-0401 93885

AQ1

Package Outlines and Soldering Recommendation

16–PIN PLASTIC DIP (300 MILS WIDE)





NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

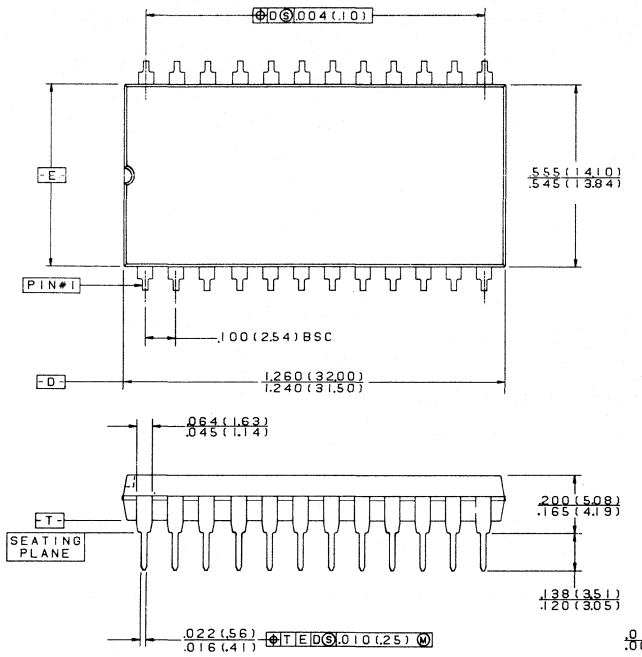
853-0406 81232

PO00280S

NJ1

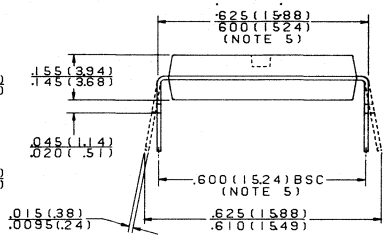
Package Outlines and Soldering Recommendation

24–PIN PLASTIC DIP (600 MILS WIDE)



NOTES

1. CONTROLLING DIMENSION: INCHES. METRIC ARE SHOWN IN PARENTHESES.
2. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-011-AA, FOR STANDARD DUAL IN-LINE (DIP) PACKAGE .600 INCH ROW SPACING (PLASTIC) 24 LEADS (ISSUE B, 7/85)
3. DIMENSION AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T", "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (.25MM) ON ANY SIDE.
5. THESE DIMENSIONS MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#24 WHEN VIEWED FROM THE TOP.
7. THIS PKG NOT PROCESSED THROUGH STANDARD SIGNETICS PROCESS. LEAD FINISH: SOLDER PLATED LEAD ANGLE : 90 DEG. BEND

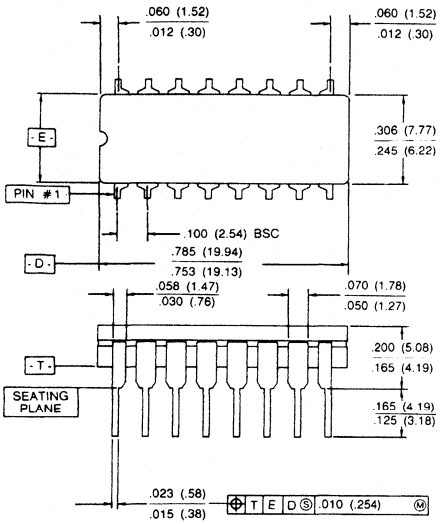


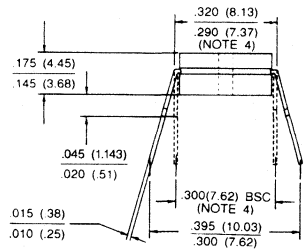
853-1202 88270

NN3

Package Outlines and Soldering Recommendation

16–PIN CERAMIC DIP (300 MILS WIDE)





NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

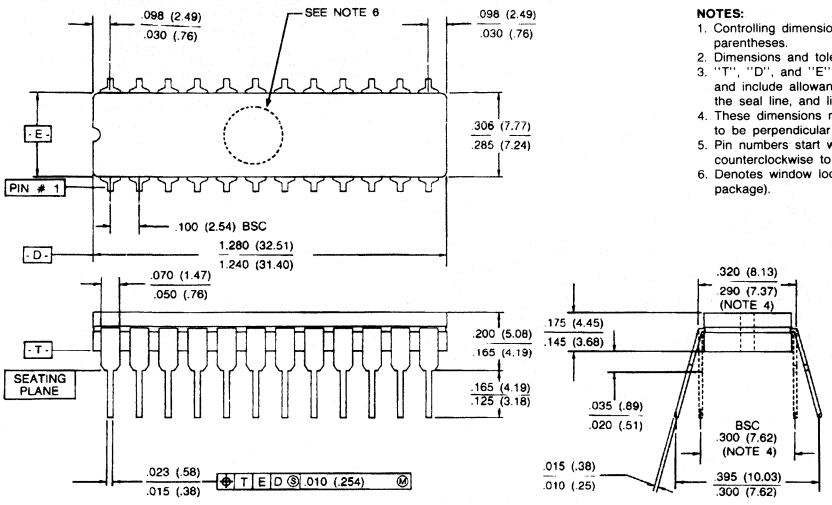
853-0582 88375

PO00491S

FJ1

Package Outlines and Soldering Recommendation

24–PIN CERAMIC DIP (300 MILS WIDE)



NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.
6. Denotes window location for EPROM products (see FA package).

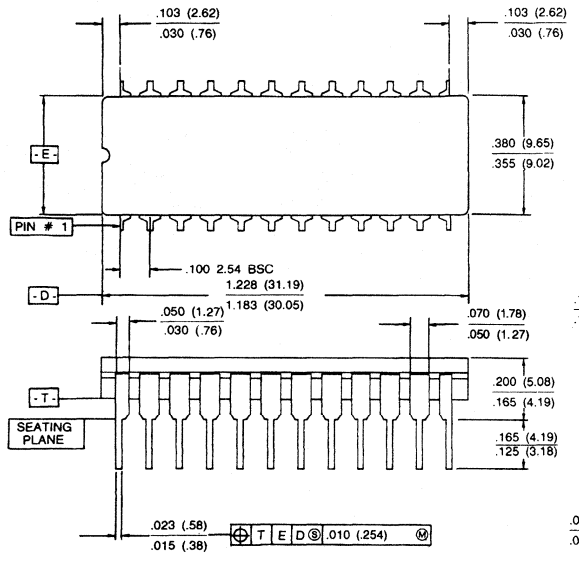
853-0586 84000

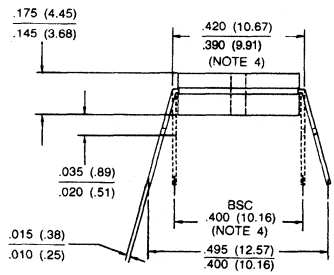
PO00402S

FN1

Package Outlines and Soldering Recommendation

24–PIN CERAMIC DIP (400 MILS WIDE)



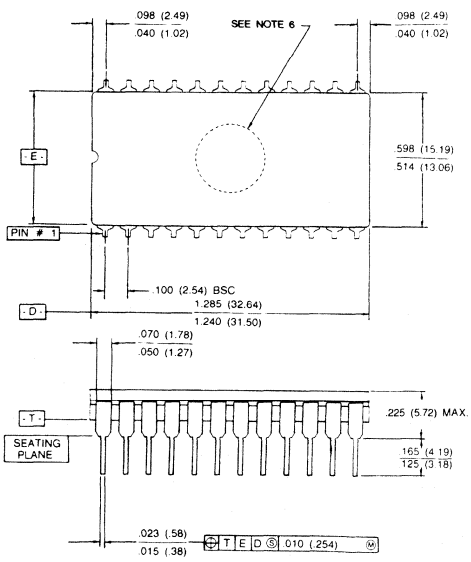


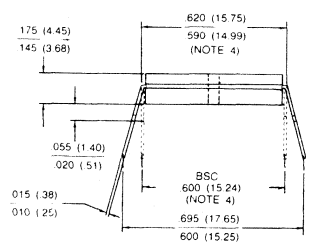
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0587 88274

FN2

24–PIN CERAMIC DIP (600 MILS WIDE)





NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.
6. Denotes window location for EPROM products.

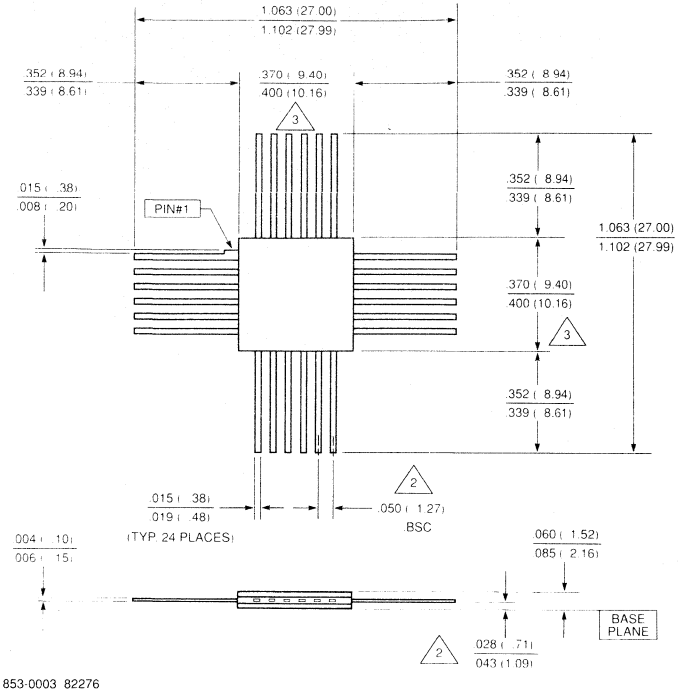
853-0588 84221

PD004645

FN3

Package Outlines and Soldering Recommendation

24–PIN CERAMIC QUAD FLAT PACK (375 MILS SQUARE)



NOTES

1. CONTROLLING DIMENSIONS: INCHES. MILLIMETERS ARE SHOWN IN PARENTHESIS.
2. THIS DIMENSION SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
3. THE DIMENSION ALLOWS FOR OFF-CENTER LID, MENICUS AND GLASS OVER RUN.
4. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#24 WHEN VIEWED FROM THE TOP.

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DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of seven series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MAGNETIC PRODUCTS*

LIQUID CRYSTAL DISPLAYS

The contents of each series are listed on pages III to IX

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

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* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

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IC05	**Advanced Low-power Schottky (ALS) Logic Series**
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S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07**	**Small-signal field-effect transistors**
S6	**SC08a***	**RF bipolar transistors**
	SC08b*	**RF power transistors**
	SC09	**RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
S10	**SC14**	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**

* Not yet issued with the new code in this series of handbooks.
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C22	**PA05***	**Film capacitors**
C15	**PA06***	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08**	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

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current code	new code	handbook title
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T5	PC02*	Cathode-ray tubes
T6	PC03*	Geiger-Müller tubes
T9	PC04	Photo multipliers
T10	PC05	Plumbicon camera tubes and accessories
T11	PC06	Circulators and Isolators
T12	PC07	Vidicon and Newvicon camera tubes and deflection units
T13	PC08	Image intensifiers
T15	PC09	Dry-reed switches
C8	PC10	Variable mains transformers; annular fixed transformers
	PC11	Solid state image sensors and peripheral integrated circuits
T9	PC12*	Electron multipliers

* Not yet issued with the new code in this series of handbooks.

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current code	new code	handbook title
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C16	MA02*	**Permanent magnet materials**
C19	MA03*	**Piezoelectric ceramics**

* Not yet issued with the new code in this series of handbooks.

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current code	new code	handbook title
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